

International Journal of Innovative Research in Science, Engineering and Technology

(A High Impact Factor, Monthly, Peer Reviewed Journal)

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Vol. 8, Issue 6, June 2019

Implementation and Applications of CORDIC Algorithm in Satellite Communication

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ABSTRACT: CORDIC stands for COordinate Rotation DIgital Computer, is a algorithm, based digital signal processing has become an important tool in communications biomedical and industrial products, providing designers with significant impetus for making algorithm into architecture. In this paper, a new kind of CORDIC algorithm was presented which was based on the state machine structure and iterative operation of multilevel pipeline architecture. The algorithm has been realized in the FPGA using the multilevel pipeline architecture. At the end, by the simulation waveform and spectrum analysis results, the feasibility of the method was proved. Based on the algorithm, we also provide a digital down converter architecture using CORDIC processor to eliminate both multiplier and CORDIC scale factor.

KEYWORDS: Digital down convertor, Frequency synthesizer, Signal processing, NCO, FPGA, DDC, Satellite communication.

I. INTRODUCTION

satellite communication systems, now days going through a series of rapid changes in terms of modulation techniques and implementation. More & more DSP algorithms are used to increase the performance of the system. Thus, there is an increasing need for the efficient implementations of complex arithmetic operation require to, realize these algorithms.

Among the hardware-efficient algorithms, is a class of iterative solutions for trigonometric and transcendental functions that use only shifts and adds to perform. This algorithm is called CORDIC, was first introduced by Jack E Volder in 1959. CORDIC is an arithmetic algorithm widely used in the computation of elementary functions and digital signal processing applications, particularly where large amount of rotation operations are necessary. It calculates the trigonometric functions of sine, cosine, arctangent, magnitude and phase, to any desired precision. These transcendental functions are the core for many applications such as digital signal processing, graphics, image processing, and kinematic processing. The advances in the VLSI technology have extended the application of CORDIC algorithm recently to the field of biomedical signal processing, neural networks and wireless communications.

CORDIC works on the basis of iterative rotation of a two-dimensional vector using only add and shift operations. The DSP based communication system implementation using CORDIC is more hardware efficient than conventional as CORDIC doesn't require any multiplier and accumulator. With the digital realization of the system, we can optimize the communication system at algorithm level plus at implementation level.

The basic theory of CORDIC is explained in section II. Section deals with the error analysis and data width requirements in CORDIC implementation followed by in depth analysis of CORDIC based DDFS. In section V, issues related to FPGA implementation of CORDIC based DDFS and results of real time testing are described. The use of CORDIC based DDFS in other system is dealt in section VI. Section VII explains about CORDIC based DDC, its

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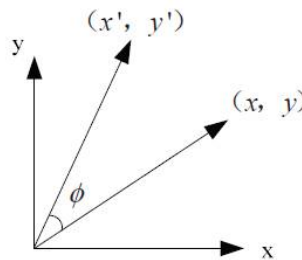
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implementation and real time spectrum followed by conclusion at the end.

II. CORDIC THEORY

The CORDIC algorithm approaches the target angle by several iterations.



As is showed in the Figure 1, the CORDIC algorithm means transforming a vector (x,y) into a new vector (x' y'). The basic circular iteration functions of CORDIC algorithm can be seen in formula (1).

$$\begin{aligned} x' &= x \cos \phi - y \sin \phi \\ y' &= y \cos \phi + x \sin \phi \end{aligned} \quad (1)$$

From formula (1) the formula (2) can be derived.

$$\begin{aligned} x' &= \cos \phi [x - y \tan \phi] \\ y' &= \cos \phi [y + x \tan \phi] \end{aligned} \quad (2)$$

If we made the $\tan(2^{-i})$ where i is the current iterative times from 0 to N, then the iterative equation can write:

$$\begin{aligned} x_{i+1} &= K_i [x_i - y_i \cdot d_i \cdot 2^{-i}] \\ y_{i+1} &= K_i [y_i + x_i \cdot d_i \cdot 2^{-i}] \end{aligned} \quad (3)$$

where $d_i = \pm 1$,

K_i will be equal to 0.6073 almost when sufficient iteration steps were computed. So the iteration equation should multiply a gain which computed by the equation (4).

$$A_n = \sum_{i=1}^N \sqrt{1 + 2^{-2i}} \quad (4)$$

The effective model of the rotation iterative which was used by the CORDIC algorithm is shown in equation (5).

$$\begin{aligned} x_{i+1} &= x_i - y_i \cdot d_i \cdot 2^{-i} \\ y_{i+1} &= y_i + x_i \cdot d_i \cdot 2^{-i} \\ z_{i+1} &= z_i - d_i \cdot \tan^{-1}(2^{-i}) \end{aligned} \quad (5)$$

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For every step of the rotation i d is computed as a sign of the z_i :

$$d_i = \begin{cases} -1 & \text{if } z_i < 0 \\ 1 & \text{if } z_i > 0 \end{cases} \quad (6)$$

Then the result is

$$\begin{aligned} x_n &= A_n [x_0 \cos z_0 - y_0 \sin z_0] \\ y_n &= A_n [y_0 \cos z_0 + x_0 \sin z_0] \\ z_n &= 0 \\ A_n &= \sum_{i=1}^N \sqrt{1 + 2^{-2i}} \end{aligned} \quad (7)$$

The result is shown in the equation (8) when the initial vector $y_0 = 0$.

$$\begin{aligned} x_n &= A_n x_0 \cos z_0 \\ y_n &= A_n x_0 \sin z_0 \end{aligned} \quad (8)$$

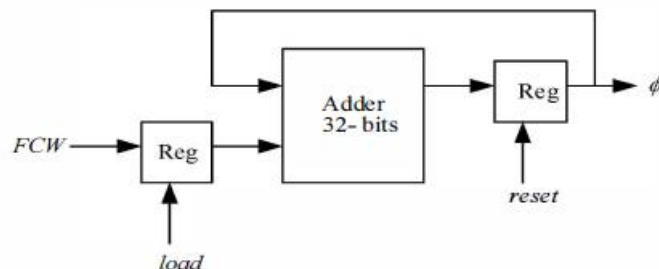
If X_0 is input data of the digital down converter (DDC), the X_n and Y_n computed by the NCO are the results of the mixing. When we do not use the multipliers, we can obtain the mixing data, which can reduce the hardware resources

III. IMPLEMENTATION IN FPGA

Figure 1 shows the General Block Diagram of CORDIC algorithm based DDFS. It contains following:

PHASE ACCUMULATOR:

It is used as an index into a waveform lookup table to provide a corresponding amplitude sample.



By the iterative sequence: 0, 1, 2, ... , N-1, for different N proposed by J. S. Walther [1], we can achieve the largest iterative angle[5], which is shown in TABLE 1

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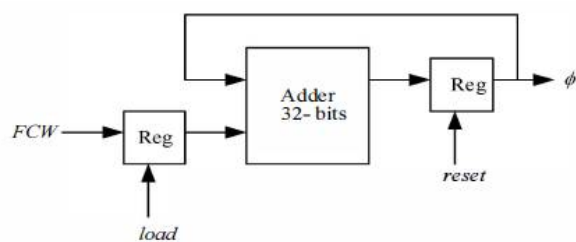


Figure 1:Phase Accumulator

i	X	Y	Z	d	$\tan^{-1}(2^i)$	$\tan^{-1}(y/x)$
0	70.00000	19.00000	30.00000	1	45.00000	15.19
1	51.00000	89.00000	-15.00000	-1	26.56505	60.19
2	95.50000	63.50000	11.56505	1	14.03624	33.62
3	79.62500	87.37500	-2.47119	-1	7.12502	47.66
4	90.54688	77.42188	4.65382	1	3.57633	40.53
5	85.70801	83.08105	1.07749	1	1.78991	44.11
6	83.11172	85.75943	-0.71242	-1	0.89517	45.90
7	84.45172	84.46081	0.18275	1	0.44761	45.00
8	83.79187	85.12059	-0.26486	-1	0.22381	45.45
9	84.12437	84.79328	-0.04105	-1	0.11191	45.23
10	84.28998	84.62897	0.07085	1	0.05595	45.11
11	84.20733	84.71129	0.01490	1	0.02798	45.17
12	84.16597	84.75240	-0.01307	-1	0.01399	45.20
13	84.18666	84.73185	0.00091	1	0.00699	45.18
14	84.17632	84.74213	-0.00608	-1	0.00350	45.19
15	84.18149	84.73699	-0.00258	-1	0.00175	45.19
Descaled:	84.1/An = 51.11	84.7/An = 51.45				

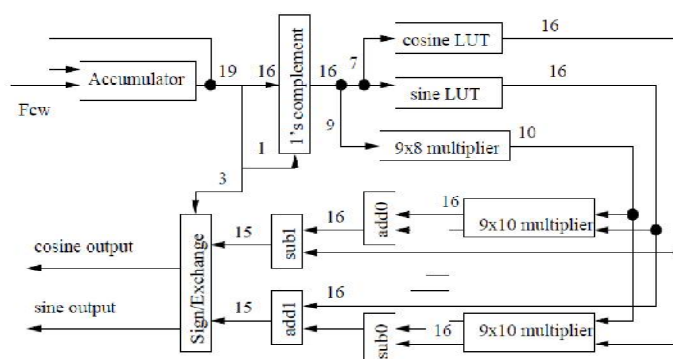


Figure 2: FPGA Implementation

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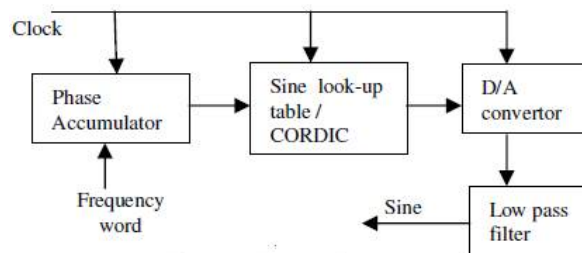


Figure 3: System Block Diagram

The DDFS is one of the requirements in digital modem design.

Particular to our satellite system, we are using BPSK modulation technique, so at transmitter end DDFS can be used in BPSK modulator as shown in fig.6. Input data is used to select the phase and that is added with the phase of the carrier. Finally phase information is converted in to amplitude by CORDIC. D/A is used to get the analog output. The system

can be upgraded to MPSK by suitable selection of phases. At receiver the CORDIC based DDFS finds application in Costas loop demodulator & Bit synchronizer as shown in fig. 4 & 5.

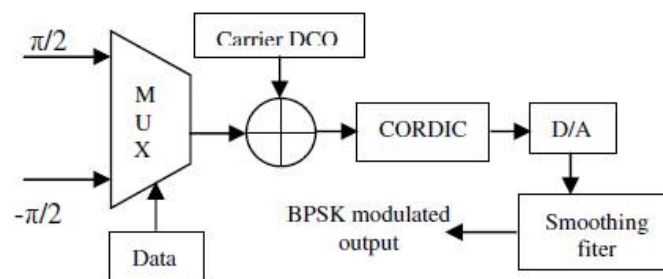


Figure 4: Digital BPSK Modulator

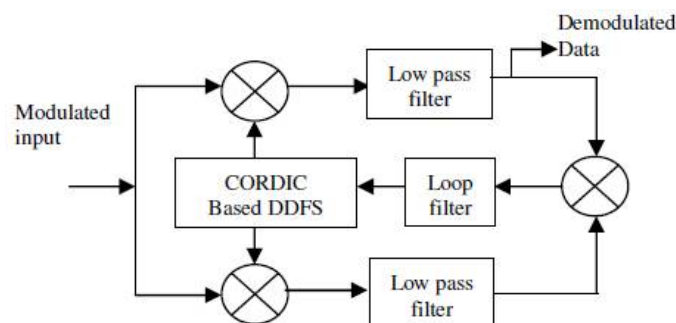


Figure 5: Costas Loop Demodulator

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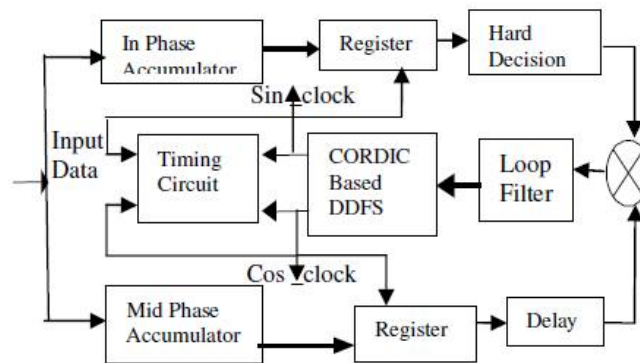


Figure 6: In phase / Mid phase bit synchronizer

IV. CORDIC BASED DDC FOR SATELLITE RECEIVER

DDC is one of the important modules of the any receiver system. There are various algorithm to down convert the RF input to any low IF frequency. One of the simple methods is the use of multiplier. For I-Q demodulation we require two multiplier and a DDFS as shown in fig.9.

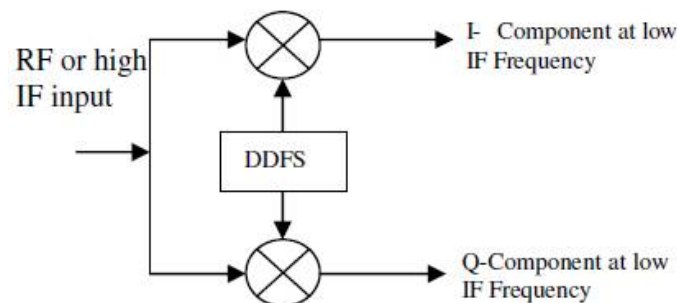


Figure 6: Multiplier based down conversion

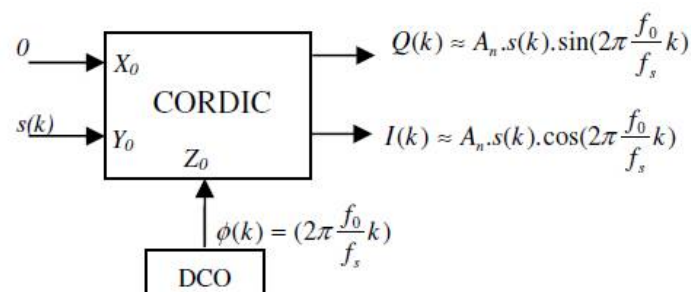


Figure 7: CORDIC based down conversion

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V. EXPERIMENT RESULTS AND CONCLUSION

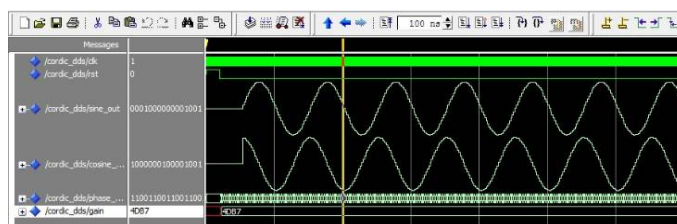


Figure 8: Sin Cos wave simulation results

The simulation result is shown in the above Figure.

VI. CONCLUSION

In this paper a CORDIC-based method for digital down conversion was proposed which overcomes the drawback of the common DDC of requiring a very large ROM table to achieve high resolution. Therefore, it helps to save chip area, power consumption, and costs. Since this CORDIC-DDC can easily be implemented on a pipelined architecture, it is suitable for high speed applications as required for the task of digital down-conversion in software radio terminals. The

CORDICDDC can realize any oscillator frequency by simply feeding it with the appropriate saw-tooth input signal. No coefficients must be changed. Thus, it empowers the software radio concept. An analytically derived worst case quantization error bound was presented which allows an efficient design of CORDIC-based DDC.

ACKNOWLEDGMENT

The authors wish to thank A, B, C. This work was supported in part by a grant from XYZ.

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