

Review Paper on Multi-level DWT using Scaling Accumulator based on Distributed Arithmetic Technique

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ABSTRACT: Discrete Wavelet Transform (DWT) is a mathematical technique that provides a new method for signal processing. Due to various useful features like adaptive time-frequency window, lower aliasing distortion and efficient computational complexity, it is widely used in many signal and image processing applications. The DWT is highly computation intensive and many of its application need real-time processing to deliver better performance. In this paper the studied of 9/7 filter coefficient based DWT. The DWT is consisting of distributive arithmetic (DA) technique. DA technique is a multiplier-less technique to provide less time and area compared to multiplier based technique. The mathematical calculation of DA technique is present in this paper.

KEYWORDS: - 1-D Discrete Wavelet Transform (DWT), DA, Low Pass Filter, High Pass Filter, Xilinx Simulation.

I. INTRODUCTION

The Wavelet Transform (WT) provides the time-frequency representation of the signal or image. To overcome the shortcoming of the Fourier Transform (FT) on constant resolution at all frequencies, the multiresolution based wavelet transform is used [1]. Here different frequencies are analyzed with different resolutions. Similar to FT, the signal is multiplied with a wavelet function which is a short oscillating function and the transform is computed for each segment. In the WT, time information is obtained by shifting the wavelet over the signal, while the frequencies are changed by contraction and dilation of the wavelet function. Continuous Wavelet Transform (CWT) retrieves the time-frequency content of the signal, DWT decomposes a discrete signal in the time domain by using dilated / contracted and translated version of a single basis function is named as wavelet. The one dimensional (1-D) and two dimensional (2-D) are applied in various application such as signal analysis, image coding.

The computation in DWT is carried out using low pass and high pass filters. The sub bands are obtained by decomposing the input signal through low pass and high pass filters. The low pass and high pass filter pair forms a Quadrature Mirror Filter (QMF) for perfect signal reconstruction. They are short length Finite Impulse Response (FIR) filter. The computation block diagram of 1-D DWT is shown in Figure 1.

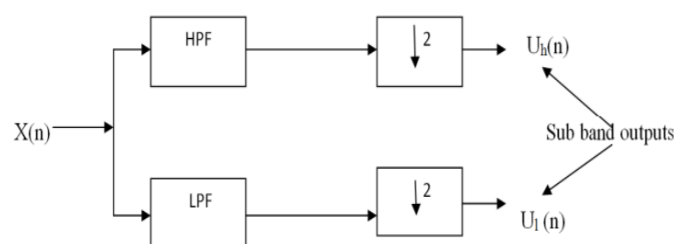


Figure 1: Computation block diagram of 1-D DWT

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Filtering unit consists of low pass and high pass filters and down sampling units. The low pass filter output is down sampled to obtain the low pass sub band output $u_l(n)$. Similarly, the high pass filter output is down sampled to obtain the high pass sub band output $u_h(n)$. This is equivalent to a two channel down sampled FIR filter computation. So, the computational unit comprises the Low Pass Filter (LPF), High Pass Filter (HPF) and a pair of down samplers. Multi resolution representations are very effective for analyzing the information content of the images. It is based on the wavelets theory which provides the details of signal between successive levels of scale or resolution.

II. LITERATURE REVIEW

Maurizio Martina et al. [1], presented a novel memory efficient high throughput scalable architecture for multi-level 2-D DWT. The authors propose a novel parallel stripe-based scanning method based on the analysis of the dependency graph of the lifting scheme. With the new scanning method for multi-level 2-D DWT, a memory efficient scalable parallel pipelined architecture is developed. The proposed architecture requires no frame memory and temporal memory, only for the 3-level DWT decomposition with an image size of 32 pixels processed concurrently. The elimination of frame memory and the small temporal memory lead to significant reduction in overall size. The presented architecture has a regular structure and achieves 100% hardware utilization.

R. Praisline Jasmi et al. [2], proposed a pipeline based architecture to perform 1-D DWT. The design focuses on the reduction of number of clock cycles. The intra and inter stage parallelism is enhanced by optimizing the computation overload at different decomposition level. The reported work mainly focuses on reducing the number and period of clock cycles for the DWT computation with little or no overhead on the hardware resources by maximizing the intra-inter stage parallelisms of the pipeline. The inter stage parallelism is enhanced by optimally mapping the computational load as associated with the various DWT decomposition levels to the stages of the pipeline and by synchronizing their operations. The intra stage parallelism is enhanced by decomposing the filtering operation equally into two subtasks that can be performed independently in parallel and by optimally organizing the bitwise operations for performing each subtask so that the delay of the critical data path from a partial-product bit to a bit of the output sample for the filtering operation is minimized. It is shown that an architecture designed based on the presented scheme requires a smaller number of clock cycles compared to that of the architectures employing comparable hardware resources.

Ms. Rashmi Patil et al. [3], this paper provides an implementation of 1-D Discrete wavelet transform DWT the usage of systolic array structure. It plays calculations of low skip and excessive pass coefficients by the use of best one multiplier. This architecture has been carried out and simulated using VLSI. The systolic nature of this architecture corresponds to a clock velocity of 19.27MHz for Coiflets1 wavelet and occasional electricity of 88.9mW for Haar wavelet. It has advantage for optimizing region and time. The structure is modular and cascable for one or multi-dimensional DWT.

S.G. Mallat et al. [4], developed a methodology generic, scalable architectures for biorthogonal wavelet transform systems. The presented architectures offer efficient hardware utilization, significant reduction in area and better performance by combining the linear phase property of biorthogonal filters with decimation and interpolation. Wavelet, word lengths for data and coefficients are parameterized in this design. The method used to design the orthonormal, bi-orthogonal wavelet. It has the advantage that it reduces the partitioning and more flexible too. Significant reduction in terms of area requirements and increased throughput performance are achieved when compared to other filter banks based on DA, convolution or the lifting scheme. The improvement in speed was achieved by rearranging the matrix element into a two-dimensional array of processing elements interconnected as a mesh. The edges of each row and column were interconnected in torus structure, facilitating simultaneous implementation of several multiplications. The reported methodology ensures substantial reduction in propagation delay compared with the conventional algorithm, systolic array and Pseudo Number Theoretic Transformation (PNTT)-based implementation

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III. DISTRIBUTED ARITHMETRIC (DA)

Let us consider the following sum of products [4]:

$$R = \sum_{k=1}^L X_k \times Y_k \tag{1}$$

Where X_k are fixed coefficients and they Y_k are the input data words. Equation (1) can be expressed in the form of a matrix product as:

$$R = [X_1 \quad X_2 \quad \dots \quad X_L] \begin{bmatrix} Y_1 \\ Y_2 \\ \vdots \\ Y_L \end{bmatrix} \tag{2}$$

Both X_k and Y_k are in two's complement format. The two's complement representation of X_k may be expressed as

$$X_k = -X_k^M 2^M + \sum_{i=N}^{M-1} X_k^i 2^i \tag{3}$$

Where $X_k^i = 0$ or 1 , and $i = N, N+1, \dots, M$ and X_k^M is the sign bit and X_k^N is the least significant bit (LSB). Equation (3) can be expressed in matrix form as:

$$X_k = [2^N \quad 2^{N+1} \quad \dots \quad 2^M] \begin{bmatrix} X_k^N \\ X_k^{N+1} \\ \vdots \\ -X_k^M \end{bmatrix} \tag{4}$$

Similarly Y_k can be represented in two's complemented format as:

$$Y_k = -Y_k^X 2^X + \sum_{i=W}^{X-1} Y_k^i 2^i \tag{5}$$

Where $Y_k^i = 0$ or 1 , and $i = W, W+1, \dots, X$ and Y_k^X is the sign bit and Y_k^W is the least significant bit (LSB). Now on combining equations (1) and (3), we get-

$$R = -(R^M \cdot 2^M) + \sum_{i=N}^{M-1} (R^i \cdot 2^i) \tag{6}$$

Where

$$R^i = \sum_{k=1}^L X_k^i Y_k, \quad i = N, N+1, \dots, M$$

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IV. PROPOSED ARCHITECTURE

In this paper, we have proposed a high speed area efficient multiplier-less 1-D 9/7 wavelet filters based DA technique. 9/7 wavelet filters coefficient i.e. 9 low-pass and 7 high-pass wavelet filters coefficient are given in table1. We multiply the filter coefficients by 128 for simplification. The mathematical calculation for 1-D high pass filter output is explained by an example.

Table 1: Show high-pass and low-pass wavelet filters coefficient.

	Wavelet filters coefficients	Multiplied by 128	7 bit binary representation
h_0	0.60294901823	77	1001101
h_1	0.26686441184	34	0100010
h_2	0.07822326652	10	0001010
h_3	0.01686411844	2	0000010
h_4	0.026748757410	3	0000011
g_0	0.55754352622	71	1000111
g_1	0.29563588155	38	0100110
g_2	0.02877176311	4	0000100
g_3	0.045635881557	6	0000110

Where h_0, h_1, h_2, h_3, h_4 are the Low pass filter coefficients and g_0, g_1, g_2, g_3 are the High pass filter coefficients.

If we take the high pass coefficients g_0, g_1, g_2 and g_3 multiply by r_1, r_2, r_3 and r_4 then we get the High pass output Y_H of the 9/7 filter as [6]:

$$Y_H = \begin{bmatrix} g_0 & g_1 & g_2 & g_3 \end{bmatrix} \begin{bmatrix} r_1 \\ r_2 \\ r_3 \\ r_4 \end{bmatrix} \quad (7)$$

Where

$$r_1 = Y(n) + Y(n - 6)$$

$$r_2 = Y(n - 1) + Y(n - 5)$$

$$r_3 = Y(n - 2) + Y(n - 4)$$

$$r_4 = Y(n - 3)$$

Let $r_1=3, r_2=4, r_3=5, r_4=6$ then

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$$Y_H = [71 \quad 38 \quad 4 \quad 6] \begin{bmatrix} 3 \\ 4 \\ 5 \\ 6 \end{bmatrix} = 421 \quad (8)$$

Now if we implement this with DA then

$$Y_H = [1000111 \quad 0100110 \quad 0000100 \quad 0000110] \begin{bmatrix} r_1 \\ r_2 \\ r_3 \\ r_4 \end{bmatrix} \quad (9)$$

Now we can make the DA matrix by the filter coefficients as

$$[B_k] = \begin{bmatrix} 1 & 0 & 0 & 0 \\ 1 & 1 & 0 & 1 \\ 1 & 1 & 1 & 1 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 1 & 0 & 0 & 0 \end{bmatrix} \quad (10)$$

$$Y_H = \begin{bmatrix} 1 & 0 & 0 & 0 \\ 1 & 1 & 0 & 1 \\ 1 & 1 & 1 & 1 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 1 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} r_1 \\ r_2 \\ r_3 \\ r_4 \end{bmatrix} = \begin{bmatrix} r_1 \\ r_1 + r_2 + r_4 \\ r_1 + r_2 + r_3 + r_4 \\ 0 \\ 0 \\ r_2 \\ r_1 \end{bmatrix} \quad (11)$$

All the DA matrix output is shift and add, get the final output. The filter coefficients are pre stored in the LUT. The value thus accessed by the incoming address shall be added with the previous values to find the product of input and the coefficient values. The scaling accumulator is used for creating the delay in the product generation. The added values of the successive inputs are stored in D-flip-flop before the final product is obtained at Y(n).

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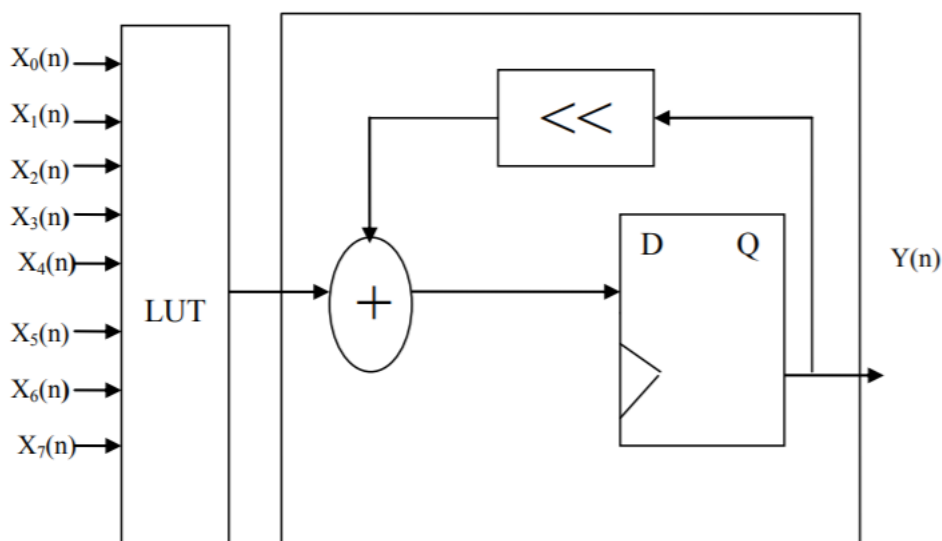


Figure 2: Scaling Accumulator

V. CONCLUSION

The processor core architecture is used to achieve high degree of parallelism, capable of handling multiple blocks of inputs to implement the convolution based DWT. The implemented results show that the architecture achieves a high speed with a lower accessing time and reaches a speed performance suitable for real time low power embedded multimedia applications. The DA based DWT architecture will implemented Xilinx software and compared to previous paper shown in final paper.

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