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An Improved SEPIC Converter and NPC Inverter for the Suppression of Torque Ripple in PMSM Using PWM

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ABSTRACT: Permanent Magnet Synchronous Motor drives are widely used in high performance applications where torque smoothness is essential, suffers from severe torque ripples. For PMSM motors, torque ripple is an important origin of acoustic noise, vibration and speed fluctuation. This paper presents a new power converter topology to suppress the torque ripple due to the phase current commutation of a permanent magnet synchronous motor drive system. A combination of a 5-level DCMLI, a modified single-ended primary-inductor converter, and a dc-bus voltage, PWM logics are employed in the proposed torque ripple suppression circuit. For efficient suppression of torque pulsation, Using modified SEPIC converter during the commutation interval. In order to further mitigate the torque ripple pulsation, the 5-level DCMLI is used in the proposed circuit. The theoretical analysis and computer simulation, using MATLAB/Simulink environment, are given to illustrate the proposed method and the performance is compared with conventional system.

KEYWORDS: PMSM, Sepic converter, 5 level diode clamped inverter, PWM controller, Torque ripple, DC link voltage control.

I. INTRODUCTION

Permanent magnet synchronous Motor (PMSM), has been widely used in industries that require high reliability and precise control due to its simple structure, high power density and wide speed range [1]. Torque ripple, which occurs during commutation period, has always been one major factor in preventing BLDCM from achieving high performance. Two general approaches have been proposed to reduce the torque ripple. The first approach is to improve the motor's geometrical structure [2]. The second approach is to control the winding currents to overcome the disturbances [3]. More studies are being done to identify the sources, characteristics and minimization of torque ripple [3]- [5]. A new approach to optimize current waveform based on d-q frame, which results in minimum torque ripple and maximum efficiency of PMSM drives is proposed in [6]. DTC is applied to PMSM drives to achieve instantaneous torque control and reduced torque ripple is described in [7]. The commutation torque ripple and its compensation technique have been analyzed theoretically in [8] - [10].

Researchers introduced some special topology of a circuit to PMSM drives to control its input voltage in [11]- [13]. In [11], the current slopes of the incoming and outgoing phases in the commutation period are equalized. In [12], a buck converter is used, and commutation torque ripple is greatly reduced at low speed. In [13], a super lift Luo converter is placed at the front of the inverter to produce desired DC link voltage and the commutation to required ripple is reduced at high speed. Those methods suffer from slow voltage adjustment and can achieve torque pulsation reduction only in low or high speed regions. A new approach of minimizing commutation torque ripple for PMSM

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based on Single ended primary inductor converter (SEPIC) is presented in[14].But the conventional SEPIC has pulsating output current similar to buck boost converters. In addition, the SEPIC converter transfers all its energy via the series capacitor so a capacitor with high capacitance and current handling capability is required. In [15], an average torque control method using one-cycle control (ATC-OCC) has been proposed using dc-bus voltage and current measurements, without using back-EMF and accurate rotor position information. In order to suppress the torque ripple for PMSM, a current optimization technique has been proposed in both conduction mode and commutation mode using integral variable structure control [16]. A direct adaptive controller has been proposed to improve inverter current regulation during large back-EMF operation, which results in significant torque ripple suppression [17]. A novel current control algorithm has been reported for torque ripple suppression of PMSM drive using Fourier series coefficients [18]. In [19], a 5-level CHB inverter has been proposed for harmonics and torque ripple suppression of PMSM drive with current and speed closed loop control. This converter needs galvanic isolated dc source for each of the H-bridge. In recent years, the MOSFET-based 3-level DCMLIs are preferred to drive PMSM for low and medium power applications, which produce low current THD in the stator windings, smaller voltage steps, reduced switching loss under high switching frequency and lower common mode voltage amplitude than conventional 2-level inverter [20], [21].

In this paper, a Modified SEPIC (MSEPIC) converter is proposed as a step-up and step -down converter having high power conversion efficiency, minimized voltage and current stress than the classical SEPIC topology. The idea of this proposed work is to drive the phase currents to increase and decrease the identical slope, resulting in the reduction of pulsated commutation torque ripple. Simulation results prove that the torque ripple is reduced when compared with the conventional method.

II. COMMUTATION TORQUE RIPPLE IN PMSM

Ideally, the current drawn by the PMSM, with trapezoidal back EMF, takes the form of rectangular waveform as shown in Fig. 1. This kind of current waveform will produce a constant torque.

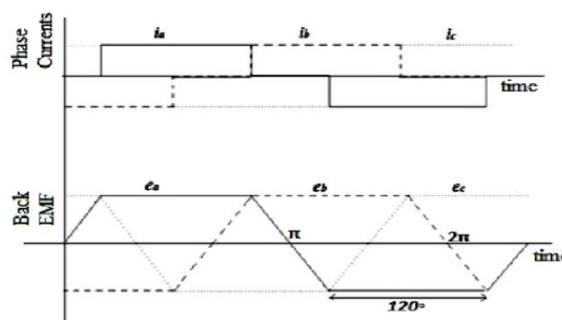


Fig. 1. Ideal Current and back emf waveform

Practically, the smoothness in torque waveform is not observed and torque ripple is prevalent. Various non-linearity in the machine will result in the disruption of the ideal rectangular current waveform thereby resulting in torque ripple. The excitation current waveforms do not change instantaneously and / a variable commutation time for different speeds is observed as shown in Fig. 2.

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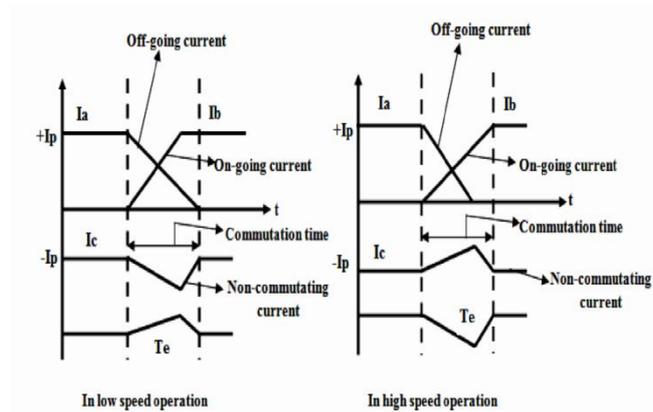


Fig. 2. Commutation Currents and Torques

During this commutation time, Torque ripple occurs due to the difference between the time taken by the ongoing phase ‘b’ current to reach the saturation value and the time taken by the off going phase ‘a’ current decay to zero. In order to eliminate the dip in the Torque waveform, the difference in the commutation time for ongoing and off going phase currents should be made zero as shown in Fig. 3. This torque dips can be reduced by suitable dc link voltage control method during the commutation time. This can be achieved by using proposed MSEPIC in PMSM drives.

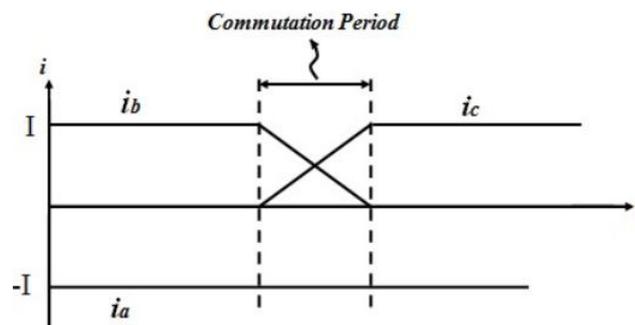


Fig. 3. Current waveform for the torque ripple compensation

The phase current behavior of 5-level DCMLI-fed PMSM with different operating speed is shown in Fig. 4. Based on the torque ripple analysis, a novel converter topology is proposed with modified SEPIC converter, which regulates the dc-bus voltage closer to $8E_m$ based on the measurement of the rotational speed of PMSM. The dc-bus voltage selector circuit applies regulated dc-bus voltage during the commutation period, which significantly diminishes the commutation torque ripple.

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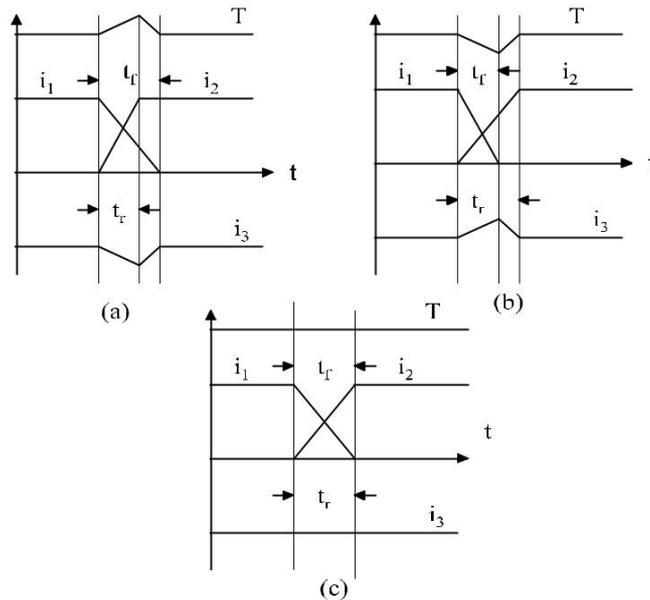


Fig. 4. Phase current behaviors at various speed conditions during commutation interval.

- (a) Phase-current dips due to an unequal slope of switching phase and switching out phase current, $\{di_1/dt < di_2/dt; V_{dc} > 8E_m\}$
- (b) Phase-current spikes due to an unequal slope of switching phase and switching out phase current, $\{di_1/dt > di_2/dt; V_{dc} < 8E_m\}$
- (c) Constant phase current due to equal slope of switching phase and switching out phase current, $\{di_1/dt = di_2/dt; V_{dc} = 8E_m\}$.

III. MODIFIED SEPIC CONVERTER

The circuit topology of the conventional SEPIC Converter is presented in Fig. 5.

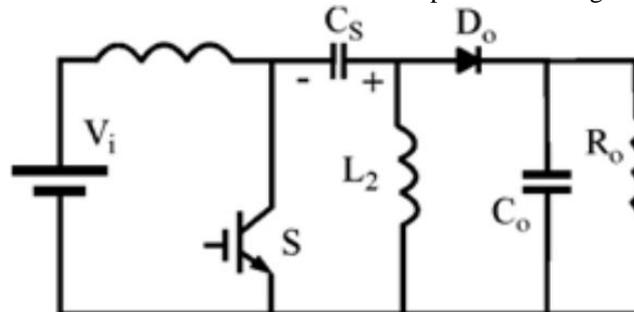


Fig. 5. Conventional SEPIC Converter

The wide range of input voltages can be realized because of the step-up and step down static gains of SEPIC converter. However, SEPIC converter suffers from higher voltage and current stress [19]. This disadvantage can be eliminated by using the proposed M-SEPIC converter circuit. Here, the modification of the SEPIC converter is accomplished by including diode D_m and capacitor C_m as shown in Fig. 6.

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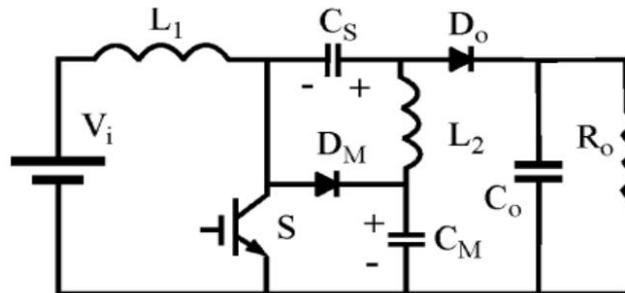
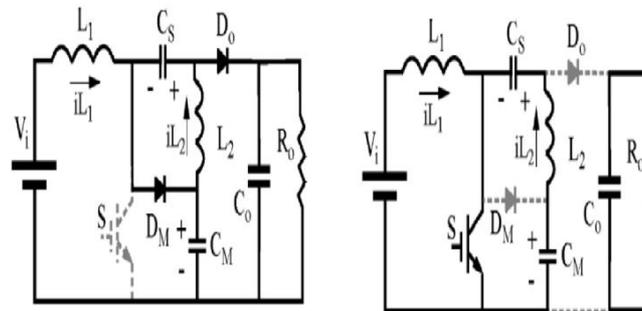


Fig. 6. Modified SEPIC Converter

A multiplier cell (C_m and D) reduces the switch stress in the proposed converter. The capacitor C_m is charged with the output voltage of the classical boost converter. Hence, the voltage applied to the inductor L_2 during conduction is higher compared with the classical SEPIC, thereby increasing the static gain.



(a) Mode 1

(b) Mode 2

Fig. 7. MSEPIC modes of operation

The continuous conduction- mode (CCM) operation of the MSEPIC converter presents the following two modes.

1) *Mode 1*: In this mode the switch S is turned-off as shown in Fig. 6(a) and the energy stored in the input inductor L_1 is transferred to the output through the capacitor C_s and output diode D_o , and also to the capacitor C_m through the diode D_m . Therefore, the switch voltage is equal to the capacitor C_m voltage. The energy stored in the inductor L_2 is transferred to the output through the diode D_o .

2) *Mode 2*: In this mode the switch S is turned-on and the diodes D_m and D_o are blocked as shown in Fig. 6(b), and the inductors L_1 and L_2 store energy. The input voltage is applied to the input inductor L_1 and the voltage $(V_{cs} - V_{cm})$ is applied to the inductor L_2 . The voltage V_{cm} is higher than the voltage V_{cs} .

The inductor L_1 current is equal to the input current and the inductor L_2 current is equal to the output current.

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IV. PROPOSED TOPOLOGY FOR PMSM DRIVE SYSTEM

A Modified SEPIC Converter with a switch over IGBT is shown in Fig.8.

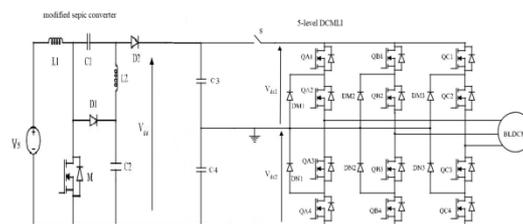


Fig. 8. Configuration of BLDCM driving system with MSEPIC Converter

In Fig. 8, M are power MOSFET s. By operating S_1 appropriately, the energy storage components L_1, L_2, C_1, C_2, C_3 and C_4 of the M-SEPIC can be adjusted to get the desired voltage. power MOSFETs used for choosing between the inputs of the inverter V_s and the output voltage of the MSEPIC V_o . V_o can be calculated as

$$V_o = \frac{1 + D}{1 - D} * V_s \quad (1)$$

Where, D is the Duty ratio.

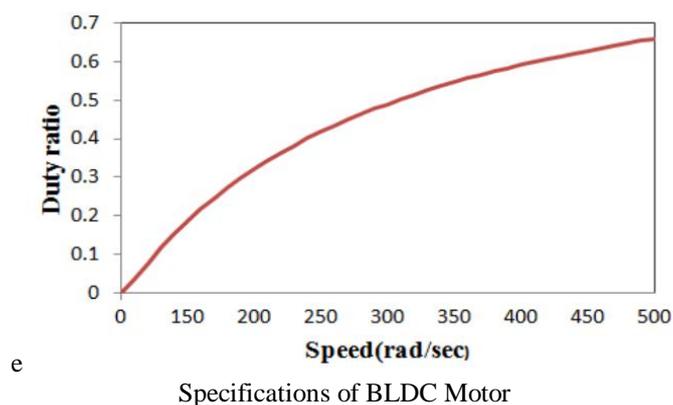
E_m is proportional to speed, i.e.,

$$E_m \propto K_e \omega \quad (2)$$

Where K_e is the back EMF co-efficient and ω is the speed of the machine. Then the duty ratio of S_1 for satisfying $V_o = 4E_m$ from can be calculated by

$$D = \frac{4K_e \omega - V_s}{V_s - 4K_e \omega}$$

According to above equation, the duty ratio of S_1 corresponding to the desired dc link voltage can be estimated by measuring the motor speed. The relationship between the duty ratio and speed is shown in Fig. 9. The duty ratio calculations are done by assuming the input voltage V_s as 200V.



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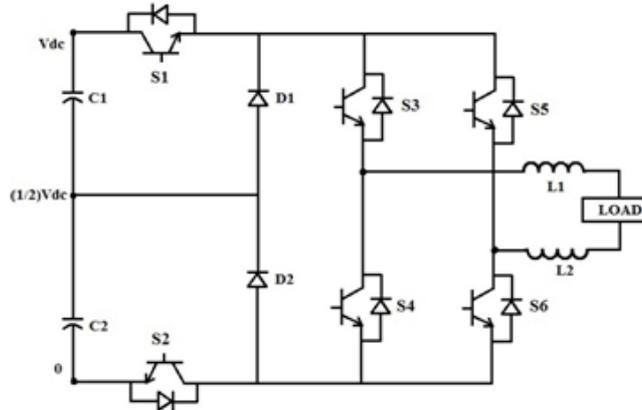
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Rated Voltage (V)	200
Rated Power (W)	518
Rated Speed (r/min)	6000
Rated Torque (N.m)	0.825
Pole Pairs	4
Phase Resistance (Ω)	3.10
Phase Inductance (mH)	3.09
Back-EMF Coefficient (V/(rad/s))	0.227

VOLTAGE SOURCE INVERTER

The inverter circuit which creates an ac voltage (and current) from a dc voltage source is called a voltage source inverter (VSI). Power-circuit topologies of a single-phase and a three-phase voltage source inverter respectively. These topologies require only a single dc source and for medium output power applications the preferred devices are n-channel IGBTs. 'Vdc' is the input dc supply and a large dc link capacitor is put across the supply terminals. There are operation can be five level mode is obtained. circuit diagram for five level operations



S1, S2, S3, S4, S5, S6, S7, S7, S8, S9, S10, S11, S12 are fast and controllable switches. D1, D2, D3, D4, D5, D6, D7, D8, D9, D10, D11, D12 are fast recovery diodes connected in anti-parallel with the switches. 'A', 'B', 'C' is output terminals of the inverter that get connected to the ac load. Capacitors and switches are connected to minimize the stray inductance between the capacitor and the inverter switches. Positive and negative line buses are also important for stray inductances limit. A three-phase inverter has three load-phase terminals and a single-phase inverter has only one pair of load terminals. The current supplied by the dc bus to the inverter switches is referred as dc link current provide. When current flow to a operation is the may be a normal open to a switch S1 and another switching operation will be closed, they will be current flow to a operation then only can be is used to the running to a switch S1 operation. Due to inverter switches are turned on and off the magnitude of dc link current often changes in step.

For n-channel MOSFET and IGBT switches, when gate to source voltage is more than threshold voltage for turn-on, the switch turns on and when it is less than threshold voltage the switch turns off. It is t remembered that the two switches of an inverter-leg are controlled and the gate control signals are low voltage signals referred of the switch. When the switch is 'on' its emitter and collector terminals are shorted. When upper switch is 'ON', the emitter of the upper switch is at positive dc bus potential. Similarly with lower switch 'ON', the emitter of upper switch of that leg is at the negative dc bus potential. Emitters of all the lower switches are solidly connected to the negative line of the dc

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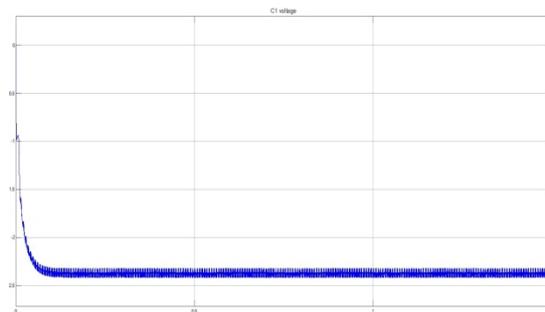
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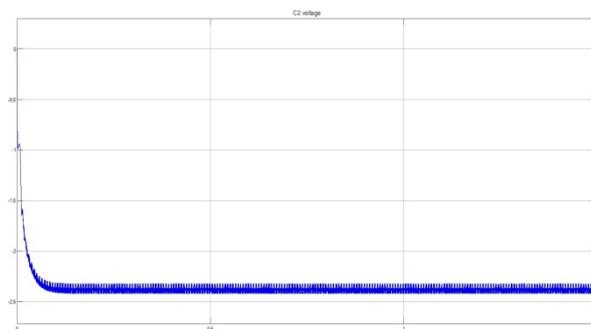
bus. Only the emitters of lower switches of all the legs are at the same potential and hence the gate control signals of lower switches need not be isolated among themselves. The step changes in instantaneous dc link current occurs even when the ac load at the inverter output is drawn a steady power. However the average magnitude of dc link current remains positive even if net power-flow is from dc bus to ac load. The net power-flows in reverse direction if the ac load connected to the inverter is regenerating. Its operation will be used to the 12MOSFET and 12diodes are parallel connected to operation for the load. The MOSFET and diode act as a switch. This type can be obtained for the level of charging and discharging.

Here the switches operation were connected to the supplies of deterioration of output voltage quality. It may be occurs to the switching operation and the level switching function. Here the switch S1 open to the conduct level operation. At regeneration mode, the mean magnitude of dc link current is negative. For an ideal input supply, with no series impedance, the dc link capacitor does not have any role. However a practical voltage supply have a considerable amount of output impedance. This may result in a cause malfunction of the inverter switches as the bus voltage appears across the non-conducting switches of the inverter. Without dc link capacitor, the series inductance of the supply line will prevent quick build up or fall of current through it. The circuit behaves differently from the ideal Voltage source inverter where the dc voltage is supposed to allow rise and fall in current as per the demand of inverter circuit.

V. SIMULATION RESULTS



Capacitor (C1) voltage



Capacitor (C2) voltage

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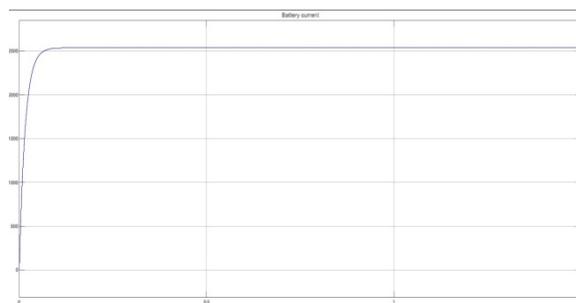
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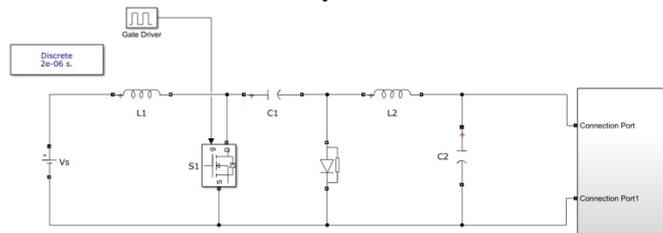
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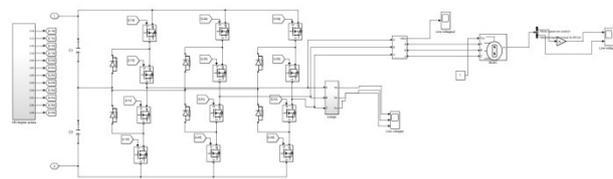
Battery voltage



Battery Current



SEPIC CONVERTER



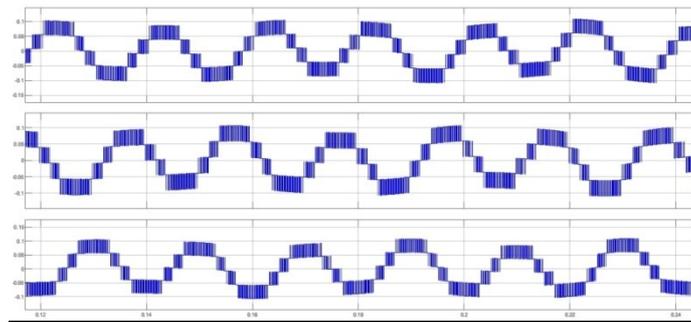
TWELVE SWITCH INVERTER

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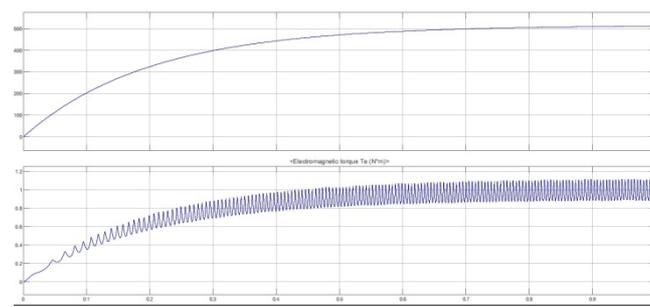
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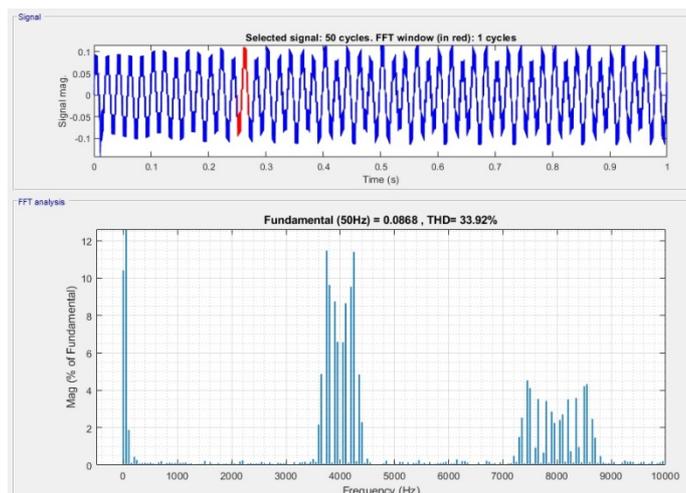
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FIVE LEVEL INVERTER OUTPUT



SPEED AND TORQUE OUTPUT



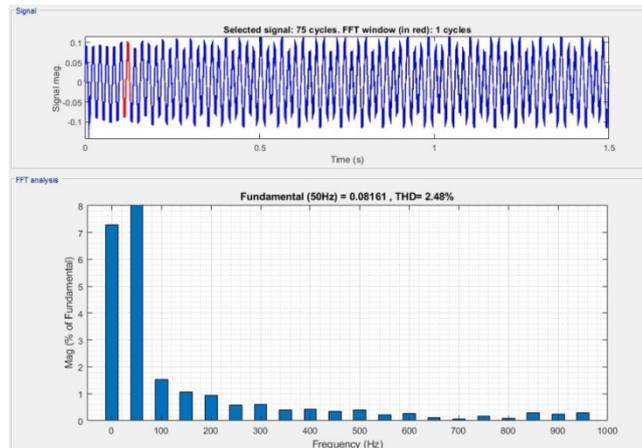
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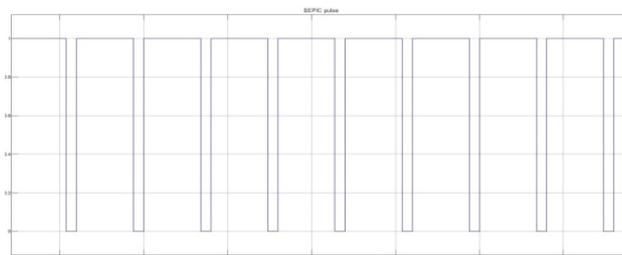
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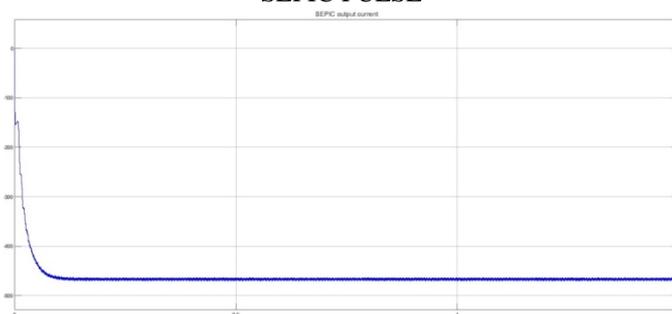
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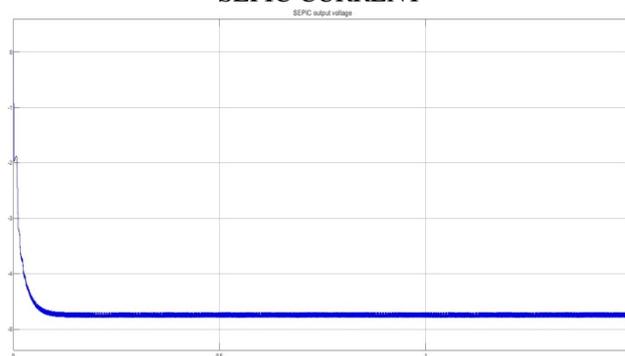
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SEPIC PULSE



SEPIC CURRENT



SEPIC VOLTAGE

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VI. CONCLUSION

The DC voltage bus control strategy is more effective in torque ripple reduction in the commutation interval. The proposed topology accomplishes the successful reduction of torque ripple in the commutation period and experimental results are presented to compare the performance of the proposed control technique with the conventional 2-level inverter, 3-level DCMLI, 2-level inverter with SEPIC converter and the switch selection circuit-fed PMSM Modified SEPIC converter is analyzed for reducing commutation torque ripple in PMSM drives. The reduction in voltage and current stress of the main switches are the main advantage of this topology. Simulation is implemented for wide range of speed and the results is apparent that the torque ripple is effectively reduced. Hardware implementation of PMSM drive with conventional control is done using FPGA. The close correlation between simulation and hardware results illustrate the relevance of the topology for torque ripple minimization.

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