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# A Research on Low-Power Explicit Pulse Tigger Flip-Flop Desing Based On a Signal Feed through Scheme

Mr.Muzaffar Husain AB Khaliq<sup>1</sup>, Prof.U.B.Pagare<sup>2</sup>,

M.E. (E&TC) Gangamai College of Engineering Nagaon Tal Dist Dhule MH, India<sup>1</sup>

Assistant Professor in NES Gangamai College of Engineering Nagaon Tal Dist Dhule MH, India<sup>2</sup>

**ABSTRACT:** In this brief, Proposed Explicit Pulse-triggered FF(P-FF) is more precious than the conventional transmission gate (TG) & master-slave based F-F. P-type f-f contains latch & separate clock pulse generator circuits. It is use in high-speed processors in electronics areas. Besides the speed advantage, its circuit simplicity lowers the power consumption of the clock tree system, & clock distribution, clock gating & clock network in H, The low-power flip-flop (FF) design featuring an explicit type pulse triggered and to change in normal power, average power by clock latch based on a signal feed through scheme is available. The proposed design successfully solves the long discharging path problem, reduce area, It avoid four sinusoidal clock signal & its long time delay, malfunctioning & more area, better for digital IC & overall power dissipate problems in explicit type pulse-triggered FF (P-FF) designs and achieves better speed and power performance.

Based on post-layout simulation results using TSMC CMOS 90-nm & 45-nm CMOS technology in nano engineering, the proposed design out performs the conventional P-FF design by using only 17 transistors. The average power delay is reduced to 3.57  $\mu$ W, 0.25-micrometer of sinusoidal clock. In the mean time the performance edges on power and power- delay-product metrics are 23.7% and 28.9%, respectively.

**KEYWORDS:** Flip-Flop (FF), Low Power, Pulse Triggered.

### I. INTRODUCTION

Low power flip flop is more essential in today's electronics industry. The need for low power has caused a major ideal model shift where power dissipation has become as important a consideration as performance and area. So this Low Power Explicit Pulse Triggered Flip Flop reviews various strategies and methodologies for designing low power circuits and systems. It prescribed the many issues facing designers at architectural, logical, circuit and device levels, power level and presents some of the techniques that have been proposed to overcome these difficulties. It also solves long discharging path problems. The ff design concludes with the future VLSI challenges that must be met to design low power, high performance systems.

Flip-flops are the basic storage elements used extensively in all kinds of digital IC designs. Now a today, digital designs often desire intensive pipelining techniques and employ many FF rich modules such as register files, shift register, and first in-first out. It is also estimated that the power consumption of the clock system, which consists of clock tree distribution networks and storage elements is as high as 50% of the total system power. F-Fs thus contribute a significant portion of the chip area and power consumption to the overall system design.

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A P-FF consists of a pulse generator for strobe signals and a latch for data storage. If the triggering pulses are approximately narrow, the latch acts like an edge-triggered FF. Since only one latch, as opposed to two in the conventional master–slave configuration, is required & P-FF is simpler in circuit complexity. This promotes to a higher toggle rate for high speed operations. P-FFs also allow time to get temporary across clock cycle boundaries and feature a zero or even negative set-up time. Despite these advantages, pulse generation circuitry requires delicate pulse width control to cope with possible variations in process technology and signal distribution network. In a statistical design framework is developed to take these factors into account. To obtain balanced performance among power, delay and area design space is also a widely used technique.

In this brief, we present a novel low-power P-FF design based on a signal feed-through scheme. Observing the delay discrepancy in latching data 1 and 0 the design manages to shorten the longer delay by feeding the input signal directly to an internal node of the latch design to speed up the data transition. This mechanism is

Modify by introducing a simple pass transistor for extra signal driving. When combined with the pulse generation circuitry. It forms a new P-FF design with enhanced speed and power-delay-product (PDP) performances.

## II. CONVENTIONAL P-FF DESIGNS

PF-FFs, in terms of pulse generation, can be classified as an implicit or an explicit type. In an implicit type P-FF, the pulse generator is part of the latch design and no explicit pulse signals are generated. In an explicit type P-FF, the pulse generator and the latch are separate without generating pulse signals explicitly & implicit type P-FFs is in general more power-economical. However they suffer from a longer discharging path, which leads to internal timing properties. Explicit pulse generation, on the opposite, accept more power consumption but the logic different from the latch design gives the F-F design a unique speed advantage. Its more power consumption and the circuit complexity in cascade form can be impressive reduced if one pulse generator is shares a group of F-Fs (e.g., an n-bit register). In this brief, we will thus focus on the explicit type P-FF designs only.

### A-EP-DCO: Explicit -Data Closed To Output Flip-Flop:-

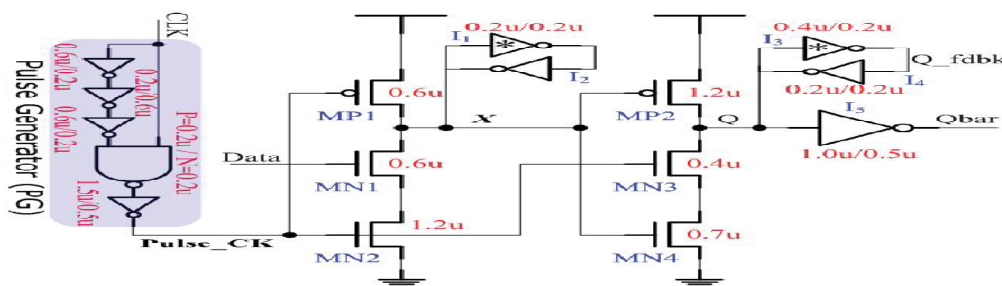


Fig.2.1 (a) EP-DCO

To provide a comparison, some existing P-FF designs are reviewed first. Fig. 2.1(a) shows explicit P-FF design, named data closet- to- output (ep-DCO). It contains a NAND-logic-based pulse generator and a semi dynamic true single-phase-clock (TSPC) structured latch design. In this P FF design, inverters I3 and I4 are used to latch data, and inverters I1 and I2 are used to hold the internal node X. The pulse width is calculated by the delay of three inverters I1, I2, I3. This design suffers from a serious disadvantages, i.e., the internal node 'X' is discharged on every rising edge of the clock in opposite of the presence of a static input one. This gives rise to large switching power dissipation in internal routes of ep-dco IC similarly noise & malfunctions may creates in this IC. To overcome this problem we use as conditional capture, conditional pre-charge conditional discharge and conditional pulse enhancement scheme have been proposed.

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### B-CDFF: conditional discharged Flip- Flop:-

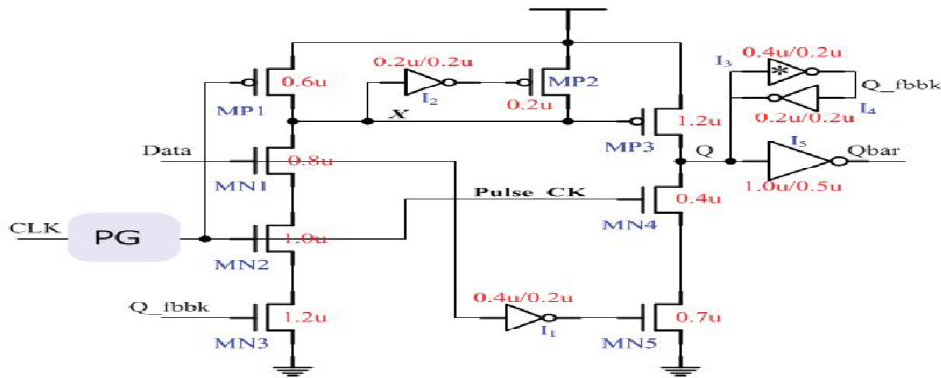


Fig.2.1 (b) CDDFF

Fig. 2.1(b) shows a conditional discharged (CD) technique. An extra nMOS type transistor MN3 controlled by the output signal Q fdbk is apply so that no discharge occurs if the input data remains “1.” In addition the keeper logic for the internal node X is simplified and depends of an inverter plus a pull-up pMOS transistor only. Now here D to Q & time delay problems is appearing. These problems avoid by using SCDDFF IC.

### C-SCDDFF: Static- conditional discharged Flip-Flop:-

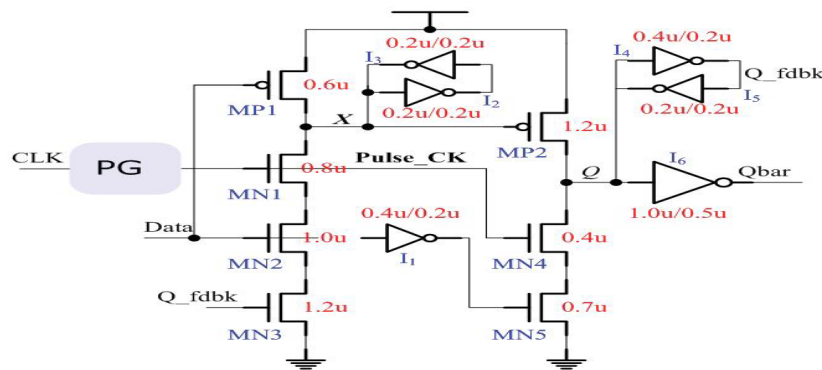


Fig.2.1(c) SCDDFF

Fig. 2.1(c) shows a similar P-FF design (SCDDFF) using a static conditional discharge technique. It has minor changes from the CDDFF design in using a static latch structure. Node X is thus extract from periodical precharges. It represents a longer data-to-Q (D-to-Q) delay than the CDDFF design. Both designs face a worst case delay caused by a discharging path providing of three stacked transistors i.e., MN1–MN3. To overcome this delay for better speed performance a powerful pull-down circuitry is required which causes extra layout area and power consumption. The modified hybrid latch flip-flop (MHLFF).

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## D-MHLFF: Modified Hybrid Latch Flip Flop:-

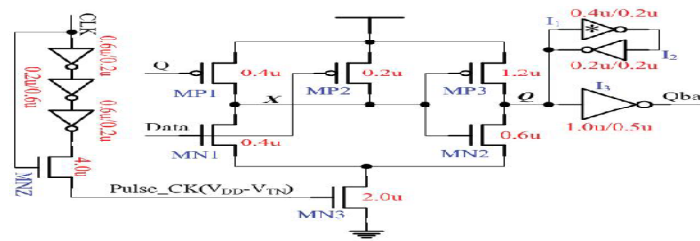


Fig.2.1 (d) MHLFF

Fig. 2.1(d) also uses a static latch such as hybrid latch, pulse latch, dual hybrid latch. The keeper logic at node X is removed. A weak pull-up transistor MP1 (P-MOS transistor) controlled by the output signal Q maintains the level of node 'X' when Q equals 0. Its circuit becomes complex, the MHLFF design encounters two drawbacks. First, since node X is not discharged firstly, a prolonged 0 to 1 delay is desired. Because a level-degraded clock pulse (deviated by one threshold voltage) is applied to the discharging transistor MN3. Second node 'X' becomes floating in certain cases and its value may increase causing extra dc power. & excess hardware material is require in MHLFF IC, Thus we can avoids this problems by using proposed design of flip-flop.

## III. PROPOSED (P-FF) DESIGNS

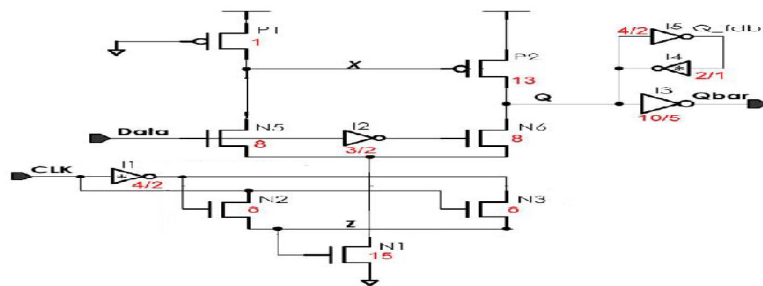


Fig.3.1 Proposed (p-FF) Design

The proposed design, as shown in Fig. 2.2, adopts two measures to overcome the problems associated with existing PFF designs. The first one is minimize the number of NMOS transistors & group of transistor in the discharging path. The second one is supporting a operations to conditionally improve the pull down strength when input data is "1." Refer to Fig. 2.2- As opposed to the transistor stacking design in Fig.2.1 (a), (b), b(c), (d) & (e), This PFF design discharging path using Pass transistor logic. Transistor N2 - in conjunction with an additional transistor -N3, forms a two-input (PTL), based AND gate to control the discharge of transistor N1. Since the two inputs to the AND logic are mostly inversely (except during the transition edges of the clock), the output node 'Z' is kept at zero most of the time. When both input signals equal to '0' (during the falling edge of the clock pulse) temporary flowing at node Z is basically harmless. At the rising edges of the clock both transistors N2 and N3 are turned ON and co-operate to pass a weak logic high to node Z, then turns on transistor N1 by a time span defined by the delay inverter I1. The switching power at node Z can be reduced due to a diminished voltage swing. Unlike the MHLFF design, where the discharge control signal is driven by a single transistor, parallel conduction of two NMOS transistors (N2 and N3) speeds up the

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operations of pulse generation. With this design measure, the number of stacked transistors along the discharging path is reduced and the sizes of transistors N1-N3 can be less.

In this design, the longest discharging path is formed when input data is “1” while the Q-bar output is “1.” It steps in when node X is discharged VTP below the VDD. This provides additional boost to node Z (from VDD-VTH to VDD). The generated pulse is taller, which enhances the pull-down strength of transistor N1.

After the rising edge of the clock, the delay inverter I1 drives node Z back to zero through transistor N3 to shut down the discharging path. This means to create a pulse with approximate width for correct data capturing & a bulky delay inverter design. Which prepare most of the power consumption in pulse generation logic, is no longer need. It should be noted that this conditional pulse enhancement technique takes effects only when the FF output Q is subject to a data change from 0 to 1. The leads to a better power performance than those schemes using an indiscriminate pulse width enhancement approach. Another profit of this conditional pulse enhancement scheme is the reduction in leakage power due to shrunk transistors in the critical discharging path and in the delay inverter.

## IV. RESULTS

The performance of the proposed P-FF design is evaluated against existing designs through post-layout simulations. The compared designs provides five explicit type P-FF designs shown in Fig-3.1, & four implicit type P-FF design named SDFF, TG latch based P-FF design ep-SFF, also two type P-FF designs as One of them is a conventional TG master-slave-based FF (TGFF) and the other one is an adaptive-coupling-configured FF design (ACFF). Conventional complementary metal oxide semiconductor NAND logic-based pulse generator design used for all P-FF designs except the MHLFF design, which has its own pulse generation circuitry as specified in Fig. 2.1(d).

The target technology is the TSMC 90-nm CMOS process. Since pulse width design is crucial to the correctness of data capture as well as the power consumption, the transistors of the pulse generator logic are sized for a design spec of 120 ps in pulse width in the transistor-transistor case. The sizing also ensures that the pulse generators can function properly in all process. With regard to the latch structures, each P-FF design is individually optimized subject to the product of power and D-to-Q delay. To minor the signal rise and fall time delays, input signals are generated through buffers. Since the p-ff design requires direct output driving from the input source to fair compare the power delay of the data input buffer (an inverter) is provides. An extra loading capacitance of 3 f/F is also placed at the output of the clock buffer. The operating condition used in simulations is 500 MHz & analysis average power of implicit & explicit type flip flop from 0%, 25%, 50% & 100% activity in microwatt, also observe PDP of both type flip flops.

Table 1:- Comparison of various P-FF designs

P-FF(Pulse Trigger Flip-Flop)	EP-DCO	SCDFF	CDFF	MHLFF	Proposed (P-FF)
No. Of Transistors	28	31	30	19	17
Avg. Power (Mw)	9.42	9.61	9.37	9.27	3.57
DELAY(Ps)	1530	711.69	853.8	615	508

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## V. CONCLUSION

In this Paper, the various Flip-flop design like, EP-DCO, MHLLF, SCDF, CDFF, TSPC based P-FF & Proposed NEW P-FF are discussed. The pulse triggered Flip Flop (P-FF) design by using two new design measures. We use D-type flip flop. The first one successfully reduces the number of transistors stacked along the discharging path by incorporating a PTL based AND logic (MOS family). The second one supports conditional enhancement to the height and width of the discharging pulse so that the size of the transistors in the pulse generation circuit can be kept minimum. These were been also designed in Cadence & Tanner Tool, synopsis', HSPICE & cosmos scope tools those result waveforms are also discussed. The comparison table also to verify the designed procedure by using CMOS 90-nm technology. With these all results Proposed PTLFF performed high speed, low power, and small area better than EP-DCO, MHLLF, SCDF, CDFF and TSPCFF designs.

In this brief, we presented a novel P-FF design by employing a modified TSPC latch structure incorporating a mixed design style consisting of pass transistor and pseudo-nMOS logic. Due to a signal feed through from input source to the internal node X of the latch & which would facilitate extra driving to shorten the transition time ( $T_s$ ) and enhance both power and speed performance. We cover VLSI integral challenges in pulse trigger flip flop. The design is intelligently achieved by employing a simple pass transistor, & reduce areas. We also observe power dissipate per gate in MOS family. Extensive simulations were conducted and the results did support the VLSI challenges to low power dissipate IC of the proposed design in various performance aspects.

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