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Adaptive DC-Link Voltage Regulation of Split Capacitor DSTATCOM

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ABSTRACT:The goal of this project is to address issues with power quality in the distribution system, such as unbalanced current and harmonic distortion. When the DC voltage is maintained at a constant level while under a light load or reduced load condition, voltage stress across switching devices increases. Under low or light load conditions, maintaining a constant dc voltage causes avoidable voltage stress across the switching device. By optimising the DC voltage, a dynamic DC voltage regulation lowers the voltage stress across the switching device. The three-phase two-level split-capacitor DSTATCOM was the subject of simulation studies for the projected process, which included reactive power compensation, load balancing, and harmonic mitigation.

KEYWORDS:Distribution Static Compensator (DSTATCOM), Voltage Source Inverter (VSI), Hysteresis Current Controller (HCC)

I. INTRODUCTION

The rise of non-linear masses due to the proliferation of strength electronic gadgets and inductive masses in a three-section 4-core (3p4w) supply device consequences in energy pleasant issues consisting of present day harmonics, poor voltage law, load unbalancing and immoderate neutral cutting-edge. A distribution static compensator (DSTATCOM) is certainly one of appropriate answers to atone for the above distribution device problems. In the 3p4w deliver gadget, three character unmarried-section DSTATCOMs, 4-leg DSTATCOM and break up-capacitor DSTATCOM topologies are generally used for harmonic mitigation, reactive power compensation, and cargo balancing and impartial cutting-edge compensation. The first topologies require extra range of switching gadgets. This leads to excessive switching losses and increases the cost. The break up-capacitor DSTATCOM topology be afflicted by dc capacitor voltage unbalancing due to dc masses. However, there are a few strategies proposed within the works to overcome the capacitor voltage unbalancing problem. In overall, the dc voltage in any topology is maintained at two times the height of factor of not unusual coupling (PCC) voltage. In reimbursement overall performance changed into taken into consideration by way of various the dc voltage and interfacing inductance; it's been concluded from the empirical relation and the logical expression that, the required dc voltage is 1.6 times the peak of PCC voltage. A gold standard dc voltage for a lively filter is defined primarily based on vector trajectories through theoretical analysis, however it's far taken into consideration best harmonic reimbursement.

In a transformer-less hybrid series active filter became proposed to enhance the power fine with decreased dc voltage. This topology does not require an isolation transformer. However, it requires three H-bridges with isolated dc sources fed from auxiliary energy deliver. In dc-link voltage changed into decreased via connecting an AC capacitor in collection with the DSTATCOM, in order that the ac capacitor voltage was introduced to ac voltage of the DSTATCOM and ends in reduction in the dc voltage requirement. Further, hybrid filter topologies are proposed to lessen the dc voltage with the combination of lively and passive filters. In the above mentioned DSTATCOM topologies, the dc voltage is constant and its value is chosen based on rated reactive load. In well known, the gadget won't always function at rated load condition, below this condition, the specified dc voltage is less while as compared to dc voltage requirement at rated or complete load condition. However, inside the above-mentioned DSTATCOM

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strategies, even the system is working beneath decreased or mild load situations; the voltage stress across switching devices may be similar to that of rated load situation. .

The objective of this project deals with overcoming of power quality problems such unbalance current, harmonics distortion in the distribution system. When the DC voltage is kept constant under light load or reduced load condition leads to increasing of voltage stress across switching devices. A dynamic DC voltage regulation reduction reduces the voltage stress across the switching device by optimizing the DC voltage based on lookup table.

II. PROPOSED SYSTEM

The electricity quality inside the distribution gadget can be stepped forward by the usage of the proposed configuration as proven in Fig.1. Here v_{sa} , v_{sb} and v_{sc} are supply voltages in a, b and c stages, respectively. The three-phase source currents are represented through i_{sa} , i_{sb} and i_{sc} , load currents by using i_{la} , i_{lb} and i_{lc} , respectively. The load draws reactive, unbalanced and non-linear currents. The phrases i_{ln} , i_{sn} and i_{fn} represent the burden neutral present day, supply neutral contemporary and clear out neutral cutting-edge, respectively. The inductance and resistance of interfacing filter are represented by L_f and R_f , respectively. This topology has two DC-hyperlink capacitors and a total DC-hyperlink voltage of 2Vdc is maintained across them using DC-link voltage controller

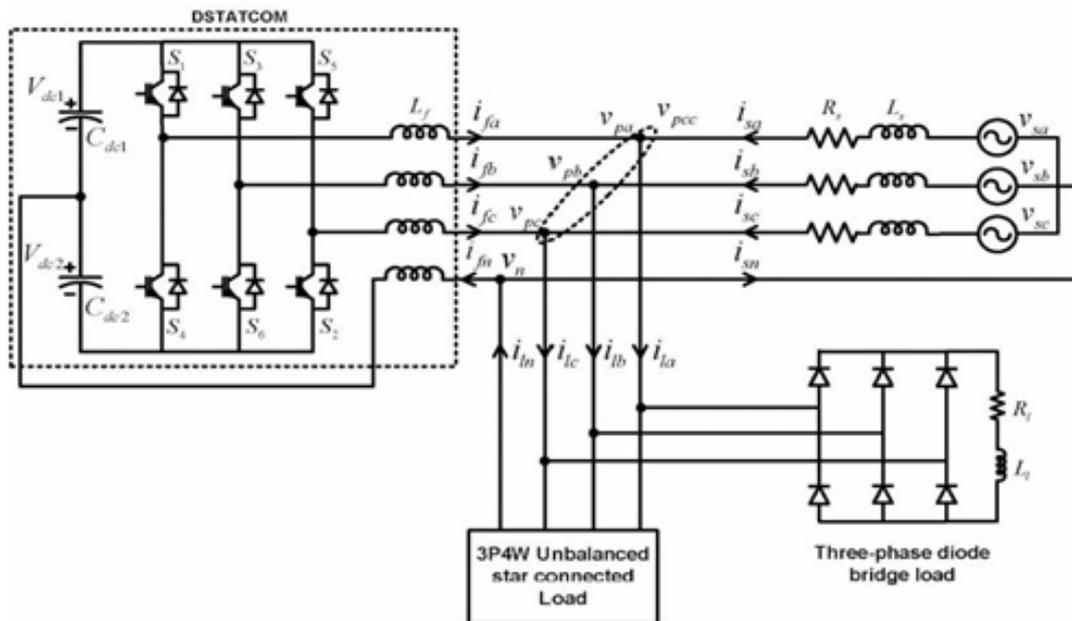


Fig. 1: Schematic diagram of distribution system with DSTATCOM

III. DESIGN OF PROPOSED ADAPTIVE DC LINK VOLTAGE SYSTEM

(i) Design of DC link capacitor (C_{dc})

The main aim of the dc link capacitor is to provide dc voltage with minimum ripples to energize the VSIs connected with it. It also have the capacity to supply reactive as well as

harmonic power of the load. The energy balance equation of the dc link capacitor is given by the equation,

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$$\Delta E = (2X - X/2) nT \quad (1)$$

Where X is the KVA of the system. The assumption is made that the DSTATCOM is working with half (X/2) twice (2X) KVA handling capacity for n cycles. T is the time period of voltage or current waveform.

The dc capacitor voltage can be allowed to vary between the values of 3.4V_m to 3.0V_m. By using the equation (1)

$$\frac{1}{2} C_{dc} [(3.4V_m)^2 - (3.0V_m)^2] = (2X - X/2) nT \quad (2)$$

$$C_{dc} = \frac{2 (2X - X/2) nT}{(3.4V_m)^2 - (3.0V_m)^2} \quad (3)$$

(ii) Design of neutral capacitor (C_n)

The neutral current to be compensated must be known to design the value of neutral capacitor. In order to design the neutral capacitor, the imaginary parts of 'a' phase Inv₁ current is equated to the 'a' phase load current.

The 'a' phase filter current of Inv₁ is given as,

$$I_{f1a} = \frac{V_1 - V_{ta1}}{R_{f1} + j(X_{f1} - \frac{X_{cn}}{\alpha})} \quad (4)$$

Where V₁ is given by,

$$V_1 = \frac{m_a V_{dc}}{\sqrt{2}} = \frac{V_{dc}}{2\sqrt{2}} \quad (5)$$

m_a represents the amplitude modulation index. In the analysis, its value is taken as 0.5.

The phase 'a' load current of Inv₁ is given as,

$$I_{la1} = \frac{\alpha V_{ta1}}{R_{la} + jX_{la}} \quad (6)$$

Equating the imaginary parts of equation (4) and (6), we get

$$\frac{\alpha V_{ta1} X_{la}}{R_{la}^2 + X_{la}^2} = \frac{V_1 - V_{ta1}}{R_{f1}^2 + (R_{f1}^2 + (X_{f1} - \frac{X_{cn}}{\alpha})^2)} \left(X_{f1} - \frac{X_{cn}}{\alpha} \right) \quad (7)$$

In order to find out the value of C_n, the equation (7) must be solved by substituting the known values in it so that the value of X_{cn} can be calculated. From X_{cn}, we can able to find out the value of C_n.

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IV. CONTROL ALGORITHM

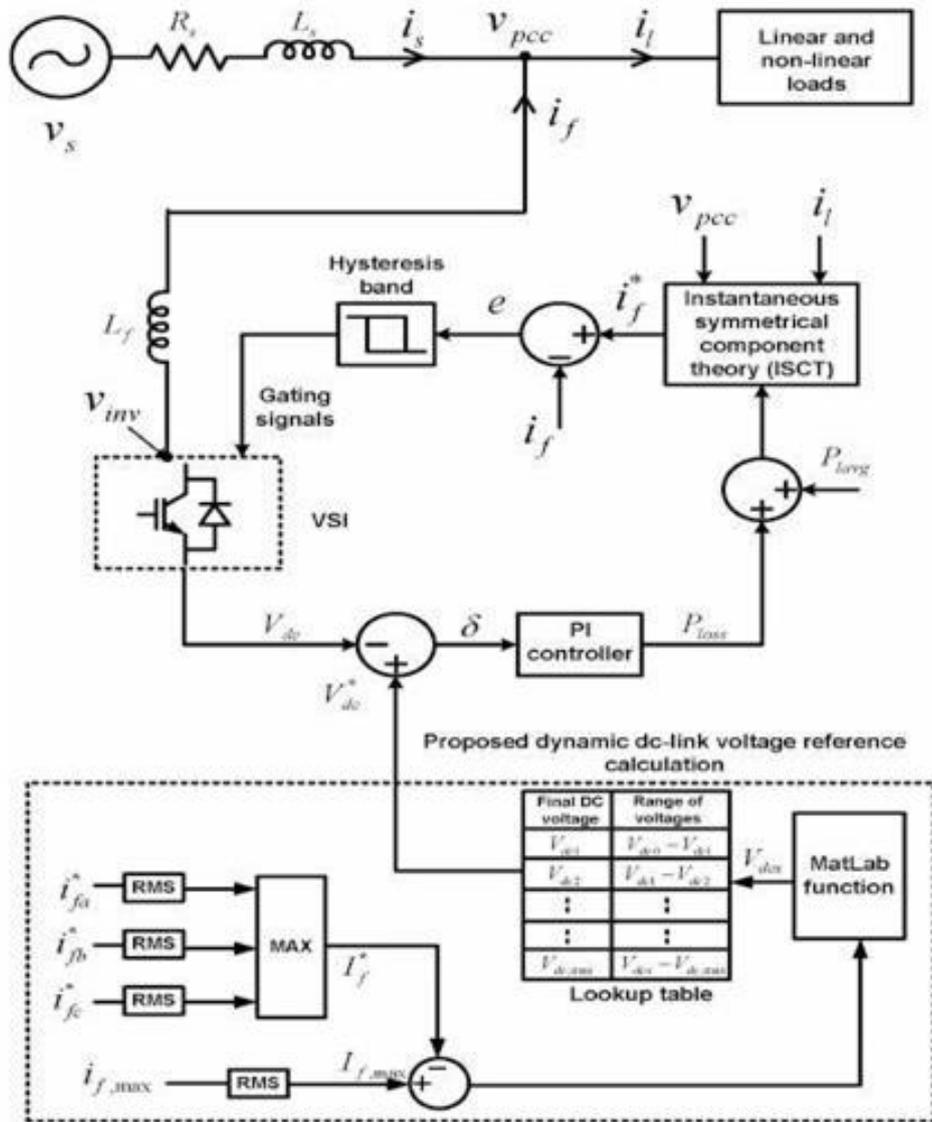


Figure 2 single-line diagram and control algorithm of proposed method

This control technique requires defining upper hysteresis band limit and lower hysteresis band limit. In open loop control strategy, the variation in output DC voltage is common problem if load is variable, but we can get steady output if close loop strategy is used. In close loop control, output current signal is compared with reference current signal which is given. Which decrease the error in output and gives desired output. The generated gate pulses can be controlled by PI or PID controllers. The steps to be followed are,

- (i) Generate the reference filter currents (i_{fab}^*).

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(ii) Compare the reference filter currents (i_{fab}^*) with the actual filter currents (i_{fab}) and generate the pulses for VSI switches.

(iii) Maintain the dc link voltage (V_{dc}) at a reference value (V_{dcref}) with the help of PI controllers.

Step 1: Generate reference filter currents (i_{fab}^)*

It is generated by using Instantaneous Symmetrical Component Theory (ISCT). Since the source voltages are being distorted due to the presence of feeder impedance on the line, it cannot be used for the generation of reference currents. Hence the ISCT are built by using the sinusoidal fundamental positive sequence components of the distorted three phase source voltages. It is given as,

$$\begin{aligned} i_{fa}^* &= i_{la} - \left(\frac{v_{ta1}^* + \beta (v_{tb1}^* - v_{tc1}^*) P_1}{\sum_{j=a,b,c} v_{tj1}^{+2}} \right) \\ i_{fb}^* &= i_{lb} - \left(\frac{v_{tb1}^* + \beta (v_{tc1}^* - v_{ta1}^*) P_1}{\sum_{j=a,b,c} v_{tj1}^{+2}} \right) \\ i_{fc}^* &= i_{lc} - \left(\frac{v_{tc1}^* + \beta (v_{ta1}^* - v_{tb1}^*) P_1}{\sum_{j=a,b,c} v_{tj1}^{+2}} \right) \end{aligned} \quad (8)$$

Where, (i_{la} , i_{lb} , i_{lc}) represents the three phase load currents, (v_{ta1}^* , v_{tb1}^* , v_{tc1}^*) represents the three phase source voltages, P_1 is the average load power, P_{loss} represents the switching and ohmic losses in the actual compensator. $\beta = \frac{\tan \phi}{\sqrt{3}}$. ϕ is the desired phase angle between source voltage and current. In order to obtain unity power factor (UPF), the value of β was chosen as zero.

Average load power (P_l) is given by the equation,

$$P_l = \frac{1}{T} \int_{t_1-T}^{t_1} (V_{sa} i_{la} + V_{sb} i_{lb} + V_{sc} i_{lc}) dt \quad (9)$$

Equation (8) shows the reference filter currents. It is applicable for the compensation provided by only one DSTATCOM. Hence the ISCT equation (8) can be modified as,

$$i_{f1(abc)}^* = \alpha i_{l(abc)} - \alpha \left(\frac{v_{t(abc)1}^+}{\sum_{j=a,b,c} v_{tj1}^{+2}} \right) P_1 \quad (10)$$

Equation (11) represents the reference filter currents of Inv1.

The reference filter currents of Inv2 is given by,

$$i_{f2(abc)}^* = (1 - \alpha) i_{l(abc)} - (1 - \alpha) \left(\frac{v_{t(abc)1}^+}{\sum_{j=a,b,c} v_{tj1}^{+2}} \right) P_1 \quad (11)$$

Where α denotes the fraction of load compensation done by Inv1.

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V. SIMULATION RESULTS

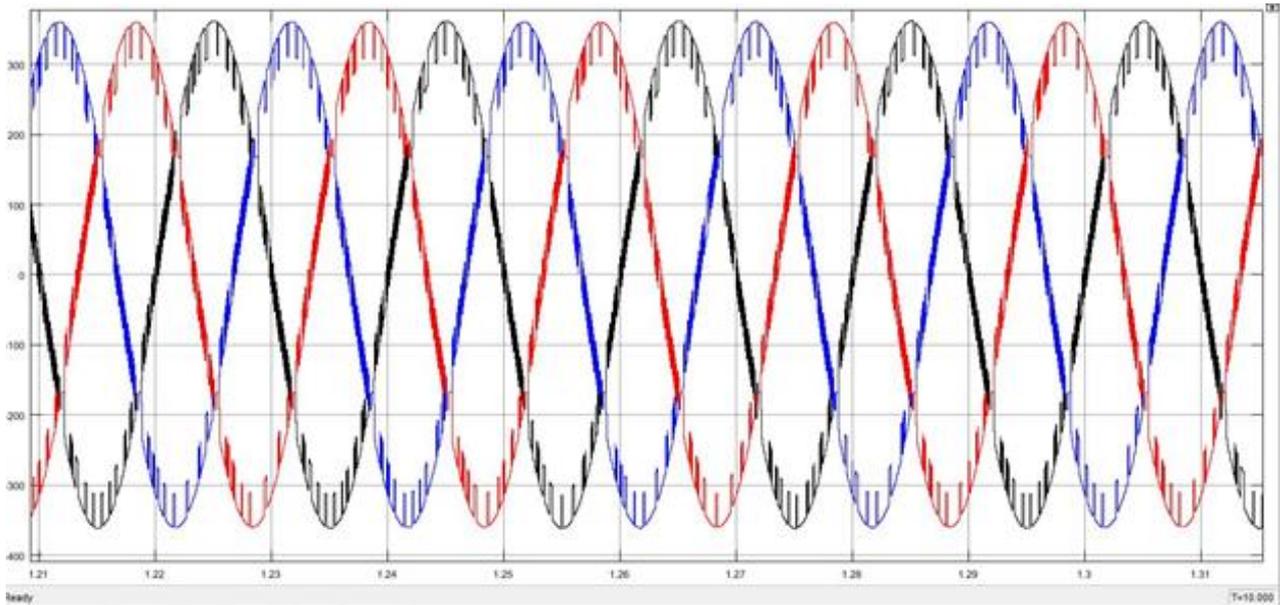


Figure 3 Three phase Supply Voltages (V_{sa} , V_{sb} , V_{sc})

Figure 3 displays the PCC voltages in positive order. The distorted PCC voltage cannot generate the reference filter current. The distorted PCC voltages are consequently converted into sinusoidal PCC voltages with equal magnitude and phase difference using transformation techniques.

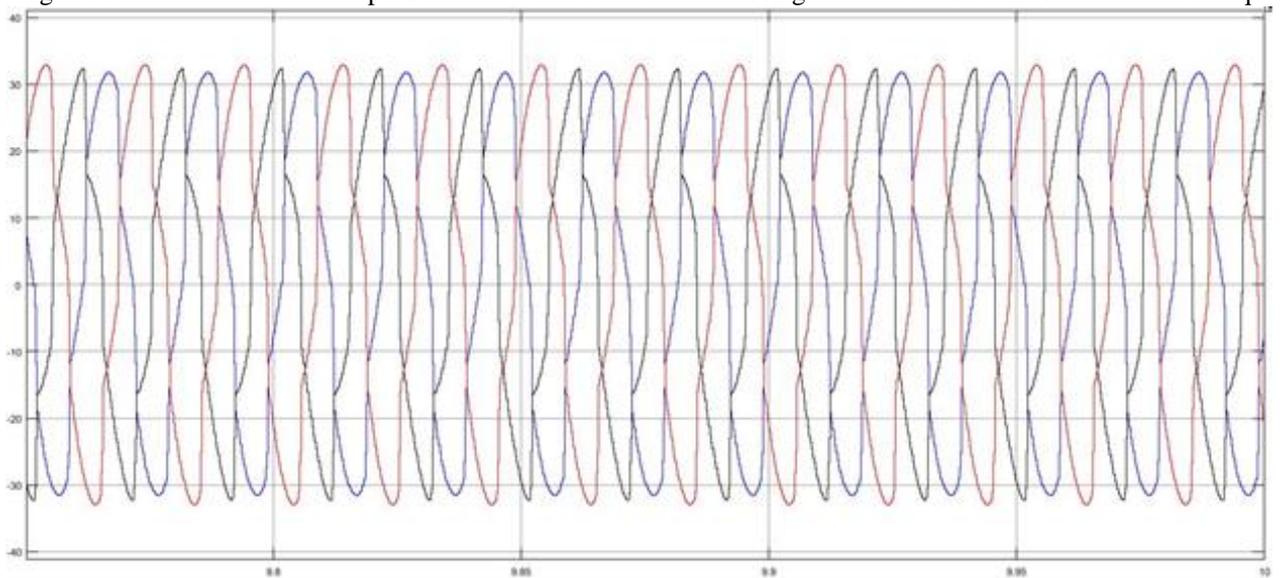


Figure 4 Three phase Source currents before compensation (I_{sa} , I_{sb} , I_{sc})

Figure 4 displays the distorted three phase source currents (I_{sa} , I_{sb} , and I_{sc}) before any compensation methods are used. The imbalance in the three phase source currents triggers the flow of the neutral source current through the

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line. So, there will be an overload on the neutral conductor. The DSTATCOM balances the distorted source current and lowers the source neutral current to zero in order to perform load balancing in the system.

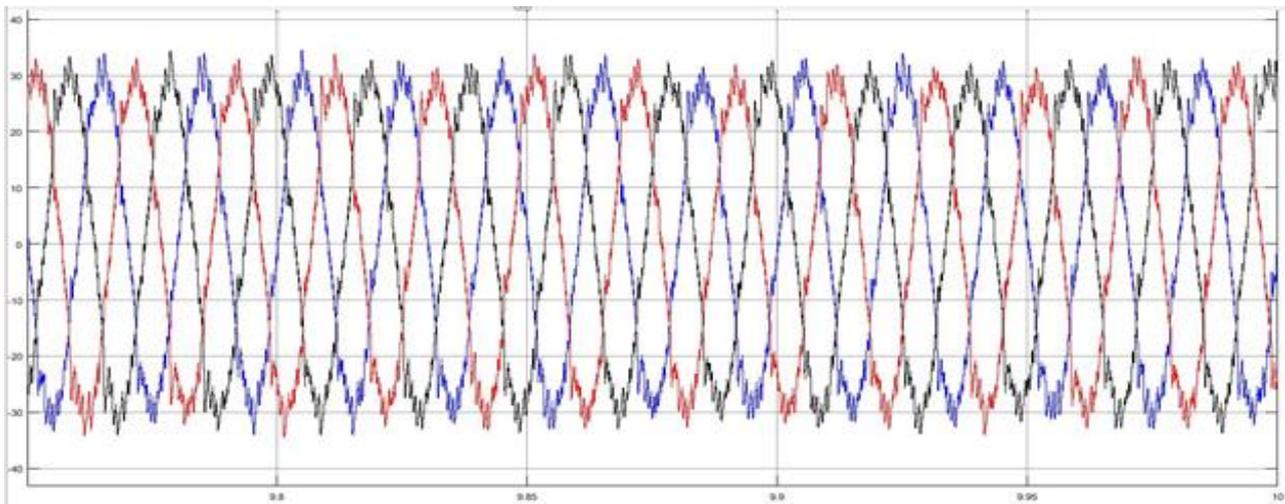


Figure 5 Three phase Source currents after compensation (I_{sa}, I_{sb}, I_{sc})

Figure 5 displays the three phase source currents (I_{sa} , I_{sb} , and I_{sc}) following DSTATCOM's compensation. The compensator source current is introduced into the line using an interfacing inductor in order to bring the source currents as balanced sinusoidal ones. After compensation, the source current has a proper phase offset and equal magnitude.

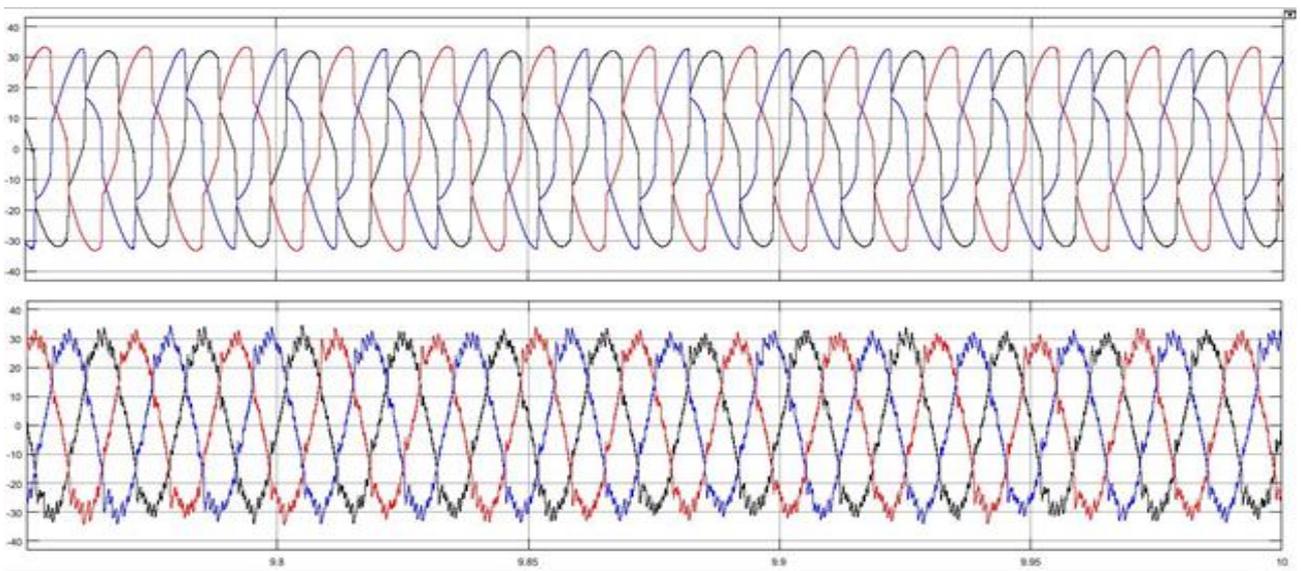


Figure 6 Three phase load currents (I_{la}, I_{lb}, I_{lc}) and Three phase Source Currents (I_{sa}, I_{sb}, I_{sc})

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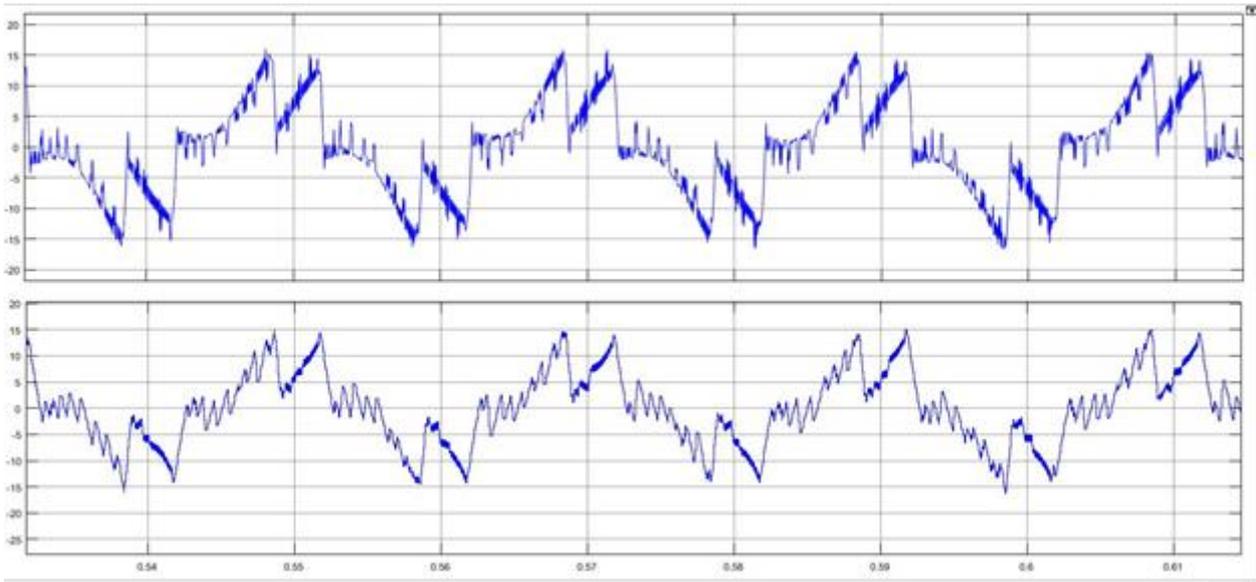


Figure 7 Reference filter current and actual filter current

Figure 7 demonstrates how the DSTATCOM injects actual filter current as well as three phase filter currents to balance out the unbalance in the three phase source currents. The control algorithm techniques provide the pulses for the DSTATCOM. Hysteresis controller error (e), which is the difference between reference filter current and actual filter current (i_{fa}), is the difference between the two.

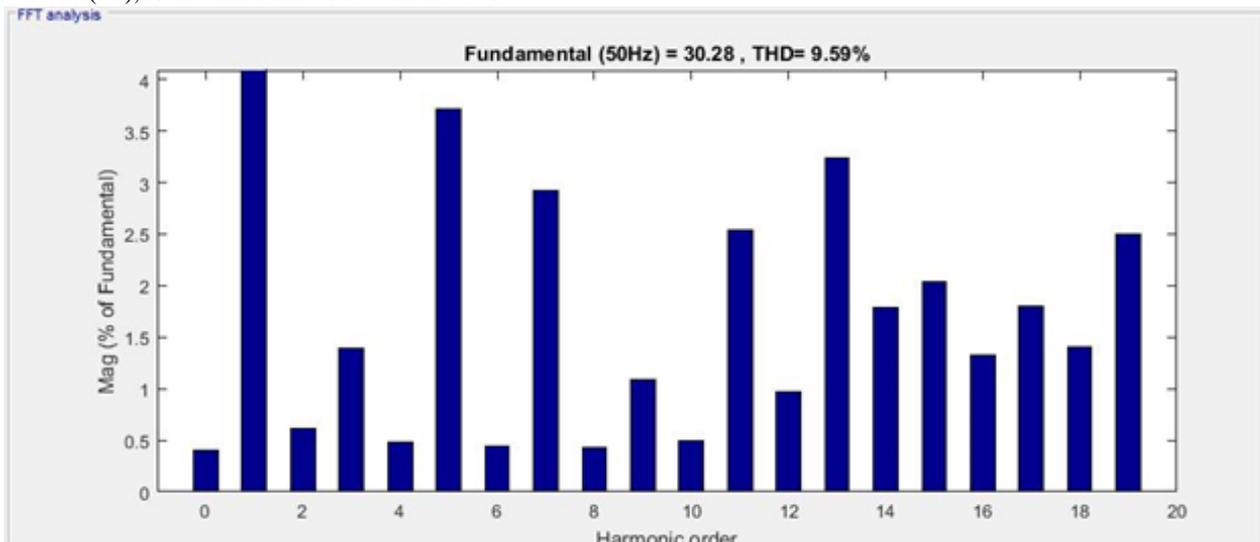


Figure 8 Harmonic Profile of Source Current (I_{sc})

VI. CONCLUSION

Results from simulations show how well the three-leg VSI-based DSATCOM topology compensates for unbalanced and non-linear loads in three-phase four-wire distribution systems. The proposed scheme's ability to share unbalanced, harmonic, and reactive powers between VSIs and to regulate the dc-link voltage and source current THDs

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is confirmed, as are the associated control algorithms. Because the DSTATCOM is utilized for compensation, the ratings of the switches, dc-link split capacitor, and stress across the VSI switches were all lowered. The suggested plan can produce comparable compensation results to leaving DSTATCOM. It also prevents the voltage unbalancing problems brought on by split capacitor VSI-based DSTATCOM topology.

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