

Design and Implementation of RBSD Technique for Various Arithmetic Circuits

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ABSTRACT: In recent years, the technological developments have increased demands for arithmetic circuits with faster computation. The emergence of signed digit representation has revolutionized the digital world. Redundant binary (RB) number system is the largely used approach for indicating a signed digit number. This Number system is designed to perform high-speed operations in image processing and in DSP applications. It gives the addition without carry generation which contract the addition time of two binary numbers. The contemplated 4-bit,8-bit and 16-bit RBSD circuits are designed using VHDL and simulated using Xilinx ISE 12.3i.

KEYWORDS: RBSD adder, carry free addition, VHDL

I. INTRODUCTION

Adder is the basic building block of all arithmetic operations like subtraction, multiplication, division and square root, etc. The current technological development in the field of integrated circuits with various arithmetic circuits with fast computing and carry free addition have been proposed. The Redundant binary signed digit adder (RBSD) has a greater advantages over other conventional circuits by eliminating more propagation time delay, high power consumption and complexity in operations due to carry free addition.

Mostly, fast adders are designed using ripple carry adder and carry select adder. In ripple carry adder, the propagation of carry results in critical delay. Carry select adders use of fast adders but it increases the length of the bit in the adder and high complexity of the circuit. The introduction of Redundant binary signed digit (RBSD) number system in designing fast adders helps to attain high-speed processing due to their ability of the technique called carry free addition. If the performance of the adder in the circuit is increased then simultaneously, the overall performance of the circuit also gets improved.

II. RELATED WORK

The most fundamental element of all the arithmetic circuits are adders. RBSD adders are immensely used to perform high speed logical operations. The RBSD number system has become more prominent due to the characteristics of carry free addition. It eliminates carry propagation chain which diminishes the processing time and improves the speed of the machine [4]. This adder is firstly fast and secondarily productive in terms of power utilization and chip area.

Shantanu Thakre, Viprav Mahajan, Shailesh Shukla proposed a system for Implementation of Fast Adder Using Redundant Binary Signed Digit. In this paper, the construction of ALU uses the technique of redundant binary signed digit (RBSD). The working of proposed ALU is broadly discussed.

Rakesh Kumar Saxena, Member IACSIT, Neelam Sharma designed the RBSD adder and multiplier circuits to execute high speed mathematical operations. In this, adder is re-modified to lower the intricacy of the circuit and the number of gates. As we know, the process of multiplication is the constant addition, it achieves less time for executing the circuit design. Thus, the proposed RBSD adder using NOR and NAND gates will enhance the speed of digital machines [6].

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T.N.Rajashekhara and O.Kalreported about fast multiplier design using Redundant Signed Digit numbers. In this, the less delay multiplier design is presented internally. The proposed multiplier has a multiplication time of range $O(\log_2 x)$ and area-time complexity of range $O(x^2 \log_2 x)$ for a word length of $x[7]$.

III. PROPOSED SYSTEM

RBSD number representation systems has the sufficient redundancy to permit the destruction of carryor borrow and hence the output is fast, carry free addition and subtraction. It is a signed digit representation and with digit set $\{-1, 0, 1\}$. The redundant binary representation (RBR) is a numeral system that uses A signed digit number is represented by $m+n+1$ digits x^i ($i=-n, -n+1, \dots, -1, 0, 1, \dots, m$) having algebraic value as;

Where the value of r and x' are such that the following conditions satisfied:

- The 'r' radix is a positive integer
- Algebraic value $xv = 0$ has unique representation
- Totally shunt addition and subtraction is probable for all digits in interrelated position of two's representation.

RBSD ADDITION TECHNIQUE

This type of adder takes a finite amount of time to generate the addition result because the carry can propagate at most one position. RBSD adder structure with a digit set $(-1, 0, 1)$ per addition operation by "Two Transfer Addition Technique" which is computed in three stages [3] i.e.:

$$x_i + y_i = 2 \cdot t'_{i+1} + w'_i$$

$$w'_i + t''_i = 2 \cdot t'_{i+1} + w''_i$$

$$s_i = w''_i + t''_i$$

Where x_i and $y_i = (-1, 0, 1)$

t'' and t' = intermediate carry

w'' and w' = intermediate sums

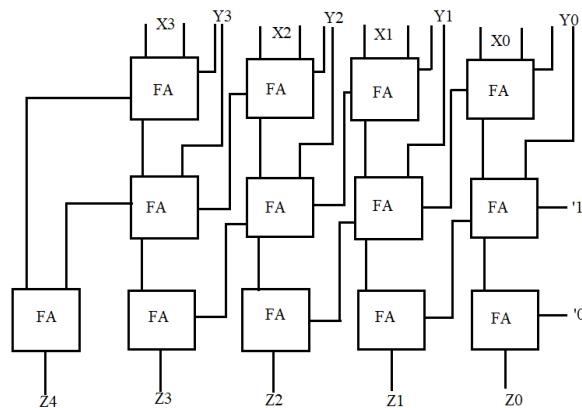


Figure 1 4-Bit RBSD Adder

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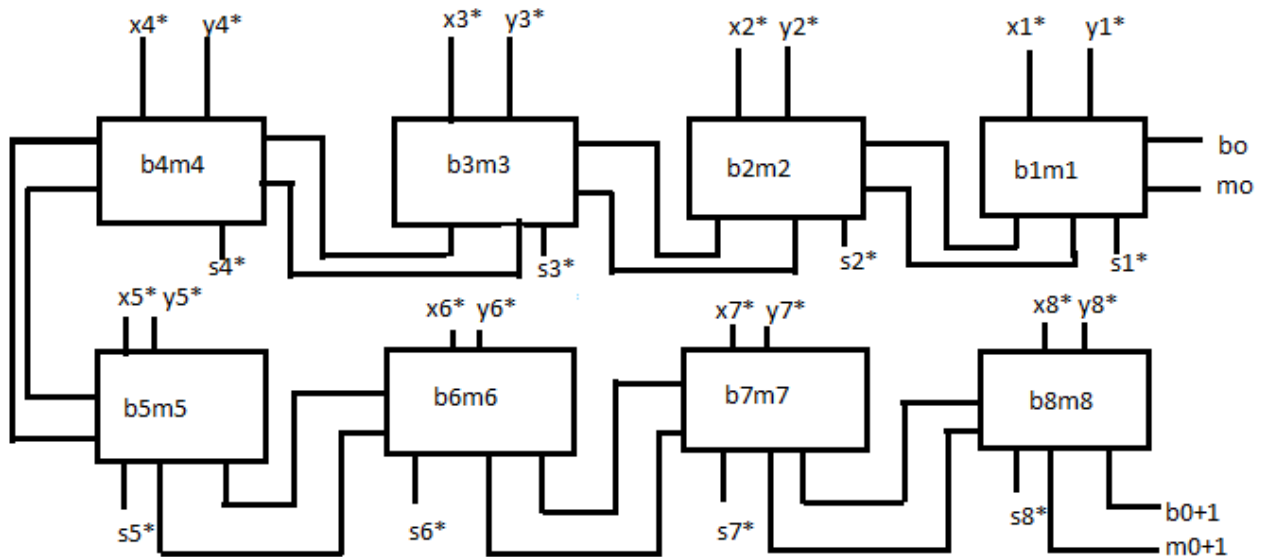


Figure 2 8-Bit RBSD Adder

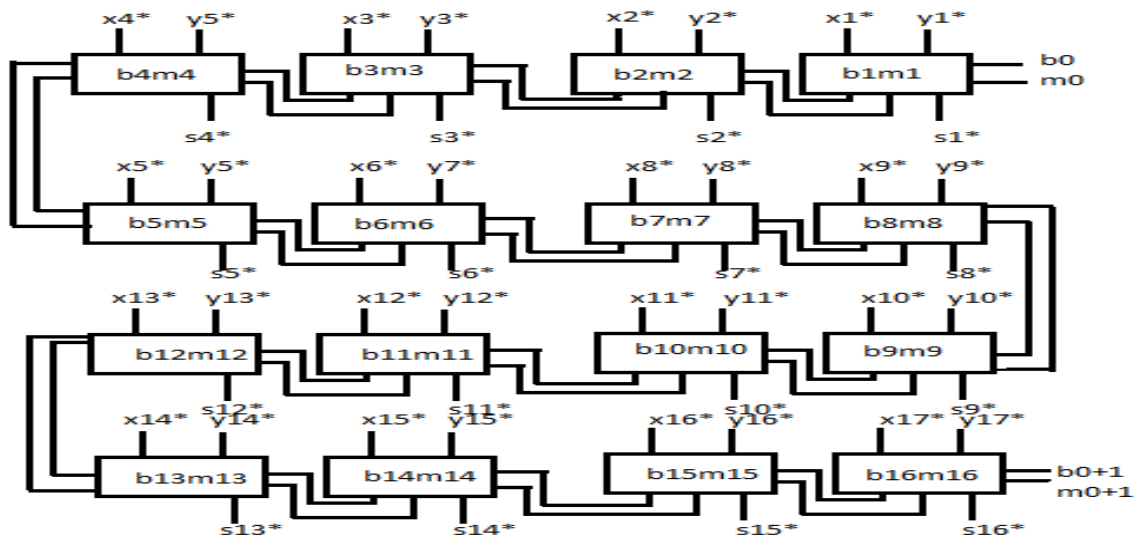


Fig 3 16-Bit RBSD Adder

IV. EXPERIMENTAL RESULTS

The proposed RBSD circuits are designed using VHDL and simulated using Xilinx ISE 12.3i and the simulation results of 4-bit,8-bit,16-bit Redundant Binary Signed Digit Adders are given below.

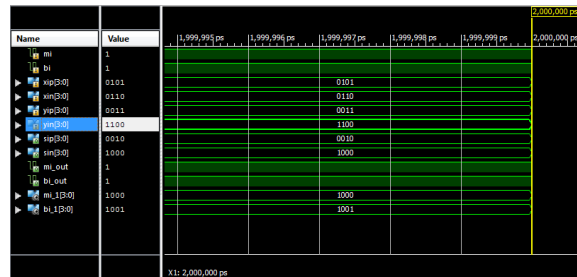


Figure 4-4-Bit RBSD Adder Output

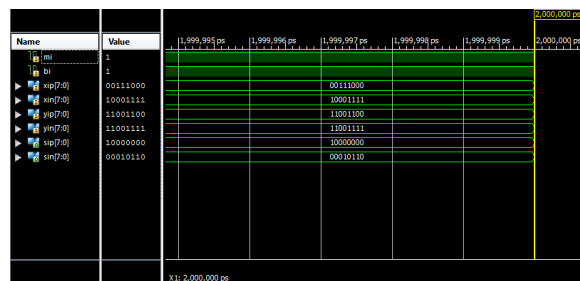


Figure 5-8-Bit RBSD Adder Output

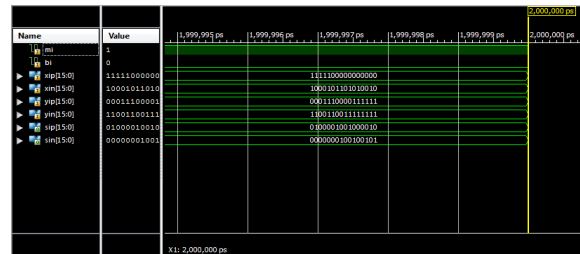


Figure 6-16-Bit RBSD Adder Output

V. CONCLUSION

The RBSD adder has a greater advantage of constant time delay, higher speed and less complexity of the circuit. When the bit length of the inputs increased, simultaneously the efficiency of the RBSD adder will also get boosted. Therefore addition is the primary operation for all the arithmetic circuits and the fast arithmetic processors with higher bit length can be designed using RBSD architecture.

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