

Analysis and Implementation of Multimode Interleaver for Wireless Communication

N. Nagaraju¹, R. Sahana², N. S. Sharika³, M. Shilpa⁴, R. Tamil Selvi⁵

Assistant Professor, Department of ECE, Adhiyamaan College of Engineering, Hosur, Tamilnadu, India¹

UG Student, Department of ECE, Adhiyamaan College of Engineering, Hosur, Tamilnadu, India^{2,3,4,5}

ABSTRACT: In today's modern world Wireless communication is one of the most vibrant research areas in communication field. WiMAX and WLAN are emerging standards in wireless broadband communication system. The channel interleaver employed in the WiMAX transceiver plays a major role in minimizing the effect of burst error. Interleaving is a technique for making forward error correction more robust with respect to burst errors and to achieve more flexibility in the multimode interleaver address generator, an efficient matrix circuit are proposed to compute MOD function for Row and Column counter values in order to replace the memory. The proposed circuit is designed and synthesized using XILINX 12.3 ISE.

KEYWORDS: Wireless systems, Interleaver, error correction, address generator.

I. INTRODUCTION

Broadband wireless access (BWA) systems have developed as the solution for the persistent demand of these multimedia services [10]. It provides improvement in multimedia data services. It supports synchronous voice, data and multimedia services for more users without the need for digital subscriber line (DSL) or cable modem. IEEE has developed standards (IEEE 802.11a/g) which are popularly known as wireless local area network (WLAN) and (IEEE 802.16e) known as mobile WiMAX [11]. The forward error correction (FEC) block uses more silicon due to addressing/permutation tables used in the conventional approaches for interleaver and de interleaver. To support the rapid development in wireless technology, the interleaver address generator hardware needs to convert to the interleaving standards.

The channel interleaver is a necessary block in the PHY of 802.11a/g and 802.16e based transmitter. In digital communication burst error occur, a number of random error correction codes have been succeed. ECC is not effective in combating bursts of errors. The paper is described as follows: Related works for WIMAX interleaver address generator is discussed in section 2. Section 3 explains the performance of the WiMAX transceiver system. In section 4 Interleaving in WIMAX system is explained. In Section 5 describes proposed architecture of mod circuits for interleaver address generator and its mathematical expression. Section 6 describe the simulation and synthesis result. Finally, this work is concluded in Section 7.

II. RELATED WORKS

Very few works interconnected to hardware implementation of the interleaver/deinterleaver used in a WiMAX system is available in the literature. The authors have explained a finite-state machine (FSM)-based address generator of the similar interleaver for all allowable code rates and modulation schemes in [3].

The channel interleaver is a necessary block in the PHY of 802.11a/g and 802.16e based transmitter. A channel interleaver for multistandard SDR has to support multiple interleaving operations thus, interleaving plays a vital

role in improving the performance of FEC codes in terms of bit error rate. The basic function of Interleaver block is to extend the encoded data into a random one. In the conventional approach, the received data is to be stored row-wise in the memory and read column-wise after applying certain permutations. To achieve more adaptability in the multimode interleaver, an address generator has to be developed using specialised blocks with reconfigurable ability and Upadhyaya et al have implemented the conventional interleaver on field programmable gate array (FPGA) with decrease in area in [5]. An address generating circuit, for 802.11 interleaver based on the conventional look up table (LUT) method is proposed in [8]. The author presented a high speed block interleaver/deinterleaver to give arbitrary column wise permutation by adopting a low-power first in first out bank structure and a simple finite state machine (FSM) in [6].

III. WiMAX TRANSRECEIVER

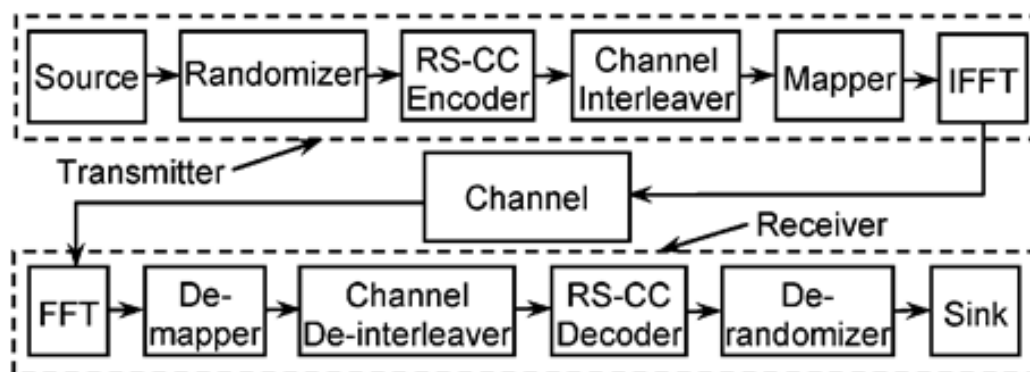


Fig 1 Block diagram of the WiMAX transceiver.

The system level overview of IEEE 802.16e based WiMAX system is shown in Fig.1. Pseudo Random Binary Sequence (PRBS) is utilized in which randomization is done by modulo 2 addition of the data with the output of the PRBS itself [3]. The randomized data bits are encoded using Reed Solomon (RS) encoder followed by Convolutional Coder (CC). The former is acceptable for correction of burst type of error whereas the latter is for random error.

IV. INTERLEAVING IN WIMAX SYSTEM

The channel interleaving is a process of rearranging code Symbols to decrease the effect of burst error. It processes one block of encoded bits at a time with block size equal to one OFDM symbol depending on the modulation design for a specific code rate. It consists of an address generator and two RAMs of the similar size. Both the memories are directed by the sel signal, generated from the address generator in such a way that when one memory block is being written, the other one is read, and vice versa. When sel = 'HIGH', the input data stream written in M1 relative to the write address as WE is active. z The read/write operation of memory blocks are moved out according to the interleaver depth. If it reaches the specified depth, then the status of sel signal is altered to swap the read/ write operation.

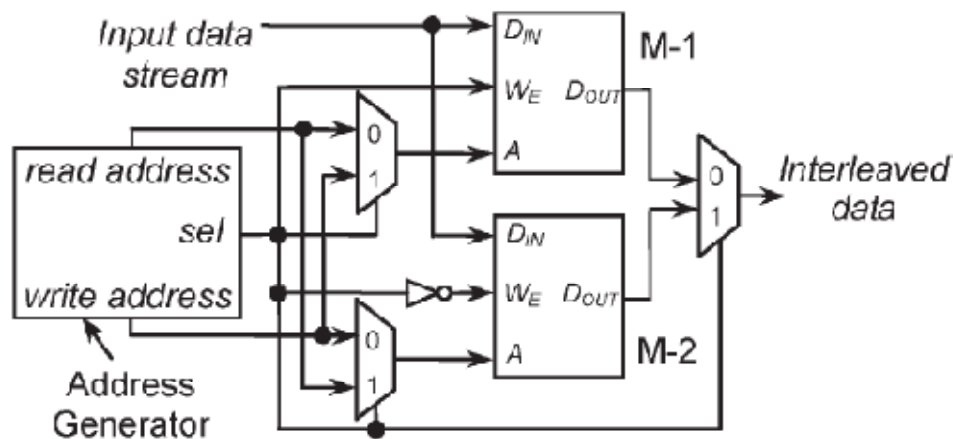


Fig 2 Block diagram of interleaver

After RS-CC encoding all encoded data bits will be interleaved by a block interleaver. As soon memory is completely filled, the bits are read Column by column manner [3].

In the block interleaver of WiMAX system, data is written in the memory in a limited Manner based on certain arrangement and read in a sequential manner. After interleaving, data send through the mapper block in which modulation takes place. The resulting data symbols are used to construct one OFDM symbol by execute Inverse Fast Fourier Transform (IFFT). Cyclic Prefix (CP) is used to decrease ISI.

V. PROPOSED MOD FUNCTION CIRCUIT

In this section, the architectural details of mod row and mod column for the multimode interleaver address generator is proposed. It incorporates row counter, column counter, selection unit, multiplier and an adder. The output of column counter is compared with d to produce a fixed count value between 0 to $d - 1$. Whereas, the row counter is a changeable one, which counts different levels between 0 to $(N_{cbps}/d) - 1$ based on particular block size selected by multiplexers (MUXs) M6 and M7. The addresses of 16-QAM and 64-QAM are not equally spaced.

Therefore, the address generator has to produce two cumulative patterns for 16-QAM and three for the 64-QAM modulation scheme. Thus, the design process adapted for QPSK can be extended to 16-QAM and 64-QAM with additional components such as incrementer, decremter and a separate MOD circuit for row and column counter respectively. To ensure adaptability in generating address for different modulation schemes, MUX based logic is perceived to select incremented/ decremented values of row counter based on specific mod_type , MOD_row and MOD_column values.

The requirement of MOD functions for column and row count values in the address generation of 16-QAM and 64-QAM are contented by the proposed MOD_column and MOD_row circuits as shown in Figs. 3 and 4 respectively. The proposed mod column and mod_ row circuit using carry save adder reduces the propagation delay compared to existing mod circuit

A. OPERATION OF MOD_COLUMN

As, the number of column (d) is chosen as 16, the column counter values moves between 0 to $(d - 1)$, that is, maximum value of 15. Hence, a 4-bit MOD_column circuit is proposed to determine the MOD value of column counter as shown in Fig. 3 With the 4-bit input as C_3, C_2, C_1 and C_0 from MSB to LSB. The final MOD2 or MOD3 value for the column counter is obtained by performing the consecutive steps as shown in Table 1.

1). LOGICAL EXPRESSION FOR MOD_COLUMN

The four bit inputs (C3, C2, C1, C0) grouped into two 2-bit numbers. To obtain the Boolean expression of the sum (s1, s0) and carry (c0) of the first 2-bit adder in Fig. 3, the variables (B1, B0, A1, A0) in (11), (12) and (13) are substituted with (C3, C2, C1, C0).

$$s_1 = C_3 \cdot C_2 \cdot C_1 + C_3 \cdot C_1 \cdot C_0 + C_3 \cdot C_2 \cdot C_1 \cdot C_0 + C_3 \cdot C_2 \cdot C_1 \cdot C_0$$

$$s_0 = C_2 \cdot C_0 + C_2 \cdot C_0 \quad (15)$$

$$c_0 = C_2 \cdot C_1 \cdot C_0 + C_3 \cdot C_1 + C_3 \cdot C_2 \cdot C_0$$

Similarly, the Boolean expression of sum (s3, s2) of the second 2-bit adder in Fig. 3, can be obtained by replacing the values of (s1, s0, 0, c0) in the place of (B1, B0, A1, A0) in (11), (12) and (13).

$$s_3 = C_3 \cdot C_2 \cdot C_1 \cdot C_0 + C_3 \cdot C_2 \cdot C_1 + C_2 \cdot C_1 \cdot C_0 + C_3 \cdot C_2 \cdot C_1 + C_3 \cdot C_1 \cdot C_0 + C_1 \cdot C_3 \cdot C_0$$

$$s_2 = C_3 \cdot C_2 \cdot C_1 \cdot C_0 + C_3 \cdot C_2 \cdot C_0 + C_3 \cdot C_2 \cdot C_0 + C_2 \cdot C_1 \cdot C_0 + C_2 \cdot C_1 \cdot C_0 + C_3 \cdot C_1 \cdot C_0$$

From the Table 1, it is noted that the sum value (s3, s2) correspond with the MOD3 (modulo 3) of the 4-bit inputs, except for the case of sum value is 3 ('11'). Where, the necessary MOD3 value is 0 ('00'), that is, complement. The key point is, if the sum value goes to '3' we have to bring into '0'. Hence, we introduced a MUX for choosing either the direct value of sum (s3, s2) or its complement value ($\sim s_3, \sim s_2$) with the control signal (sel) generated by performing AND operation of the mux.

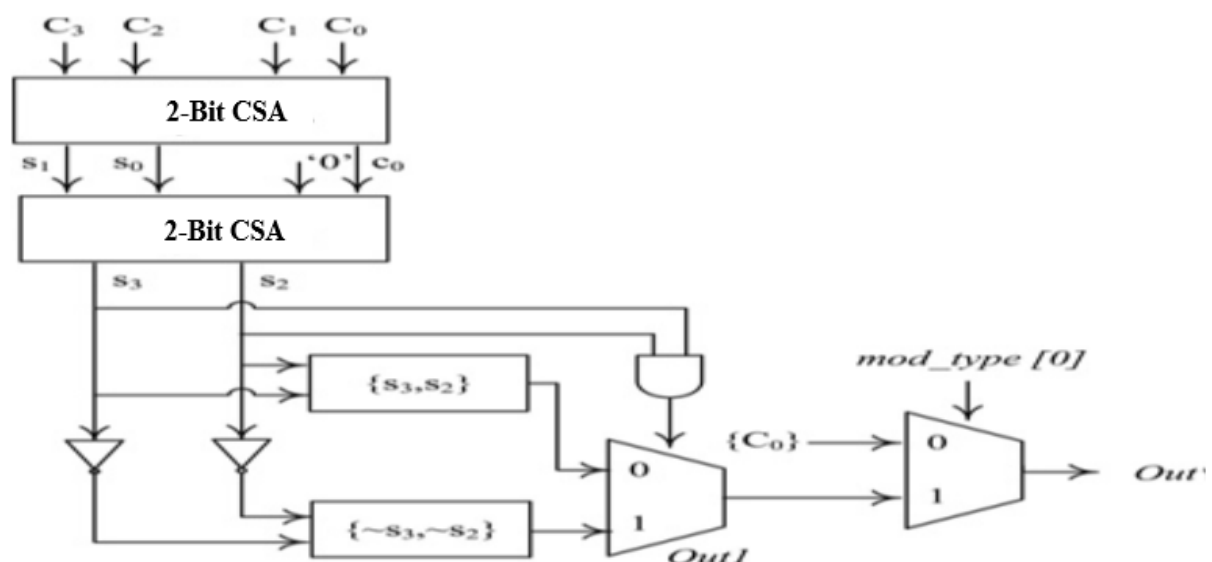


Fig 3 Proposed architecture of MOD_column circuit with 4-bit input

Finally, the output of the MOD_column is obtained by selecting either MOD2 (C0) or MOD3 (Out1) with selection signal as mod type[0].

Table 1 Working of proposed MOD_column circuit

| STEP | For the count value of 12. | Output | Operation |
|------|--------------------------------------------------------------|------------------------------------------|---------------------------------------------|
| 1 | 12 = '1100' as 11 00 | $C_1C_0 = 00$ $C_3C_2 = 11$ | Group in to two bits each |
| 2 | $C_1C_0 = 00$ $+ C_3C_2 = 11$ 0) 11 | $s_1s_0 = 11$ (sum) $c_0 = 0$ (carry) | 2-bit ripple carry addition |
| 3 | $s_1s_0 = 11$ $+ 0 c_0 = 00$ 0) 11 | MSB is fixed to '0' $s_3s_2 = 11$ (sum) | 2-bit ripple carry addition |
| 4 | If $s_3s_2 = 11$, complement each bit; Else, pass the same. | $Out1 = 00$, that is, MOD3 value | Complement |
| 5 | C_0 represents MOD2 value | $C_0 = 0$, that is, MOD2 value | |
| 6 | Final MUX with the selection line as $mod_type[0]^a$ | $mod_type[0] = 0$ for 64-QAM | MOD_column Output, that is, $Out = C_0 = 0$ |

Table 2 Truth table for the MOD_column circuit

| C_3 | C_2 | C_1 | C_0 | s_1 | s_0 | '0' | c_0 | s_3 | s_2 | sel | MOD3 | MOD2 |
|-------|-------|-------|-------|-------|-------|-----|-------|-------|-------|-----|------|------|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 |
| 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 |
| 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 1 |
| 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 |
| 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 |
| 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 1 |
| 1 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 0 |
| 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 0 |
| 1 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 0 |
| 1 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 1 |

B. OPERATION OF MOD_ROW

The maximum block size (Ncbps) for IEEE 802.11a/g and IEEE 802.16 interleaver is 576. Therefore, the row counter counts maximum value of $(Ncbps/d) - 1 = 35$. In binary form can be represented with 6-bit as '100011'. Hence, a MOD row circuit is proposed to compute MOD function for 6-bit input named as R5, R4, R3, R2, R1, R0 from MSB to LSB as shown in Fig. 4.

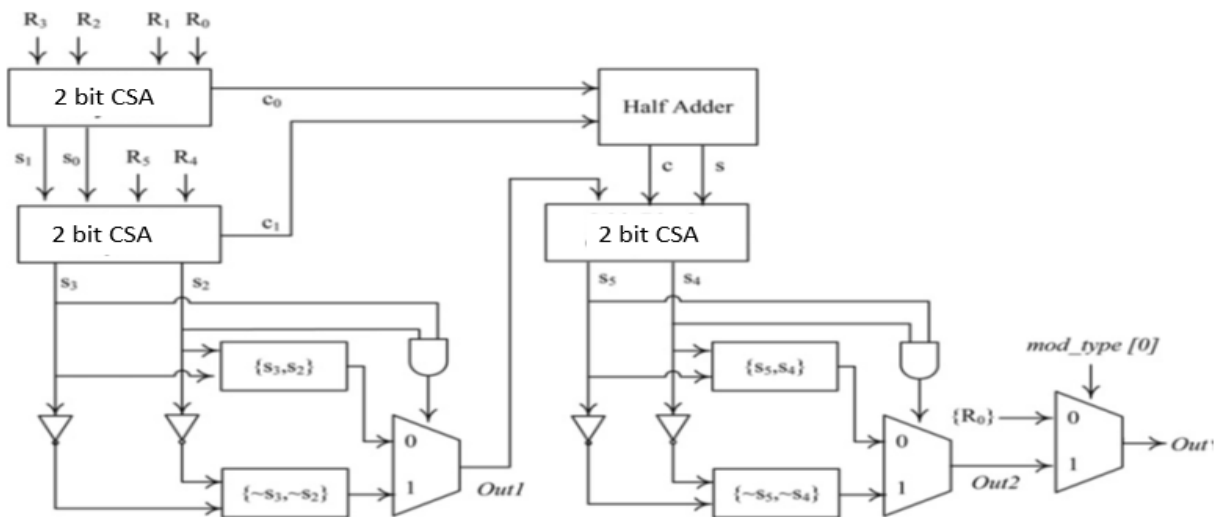


Fig 4 Proposed architecture of MOD row circuit with 6-bit input

The final MOD2 or MOD3 for the row counter is obtained by performing the successive steps as shown in Table 7. The Boolean expression for the MOD row circuit can be derived in the same manner as MOD column. The MUX selects either the direct value of sum (s5, s4) or its complement value ($\sim s5, \sim s4$) with the selection signal (sel) obtained by performing AND operation of the sum bit s5 and s4 as given in Fig. 4.

Finally, the output of the MOD row (Out) is generated by selecting either MOD2 values (R0) or the MOD3 value (Out2) with the selection signal as mod type [0].

The proposed MOD circuit for row and column, eliminates the need for two ROMs of dimension 16×3 -bit and 64×3 -bit in to store the MOD values for 16-QAM and 64-QAM respectively, which yields a large amount of reduction in resources and improvement in performance.

Table 3 Working of proposed MOD row circuit

| STEP | For the count value of 35. | Output | Operation |
|------|---------------------------------------------------------------|-------------------------------------------|---------------------------------------------|
| 1 | 35 = '100011' as 10 00 11 | $R_1R_0 = 11$ $R_3R_2 = 00$ $R_5R_4 = 10$ | Group in to two bits each |
| 2 | $R_1R_0 = 11$ + $R_3R_2 = 00$ 0) 11 | $s_1s_0 = 11$ (sum) $c_0 = 0$ (carry) | 2-bit ripple carry addition |
| 3 | $s_1s_0 = 11$ + $R_5R_4 = 10$ 1) 01 | $s_3s_2 = 01$ (sum) $c_1 = 1$ (carry) | 2-bit ripple carry addition |
| 4 | If $s_3s_2 = 11$, complement each bit; Else, pass the same. | Out1 = 01 | No Complement |
| 5 | $c_0 = 0$ + $c_1 = 1$ 0) 1 | $s = 1$ (sum) $c = 0$ (carry) | Half adder |
| 6 | $c s = 01$ + Out1 = 01 0) 10 | $s_5s_4 = 10$ (sum) | 2-bit ripple carry addition |
| 7 | If $s_5s_4 = 11$, complement each bit; Else, pass the same. | Out2 = 10, that is, MOD3 value | No Complement |
| 8 | R_0 represents MOD2 value | $R_0 = 0$, that is, MOD2 value | |
| 9 | Final MUX with the selection line as mod_type[0] ^a | $mod_type[0] = 1$ for QPSK | MOD_column Output, that is, Out = '10' = 2. |

VI.SIMULATION RESULT

In this section, the performance analysis of the proposed MOD function circuit using carry save adder are discussed. In [2], Butler & et al have developed two methodologies for computing $x \text{ mod } z$ with z fixed as 3, where x is the n -bit input and z is the MOD value. First perspective is based on combinational circuits and the second design uses cascade of LUTs. The proposed MOD circuit is much faster, consumes fewer resources and it reduces the propagation delay than the first approach in [2].

From the results, it is concluded that for higher input bit width, the proposed circuit extends further reduction in resource utilization and improvement in operating speed. Compared with the second design using LUTs, our proposed design consumes less logic resources.

Table 4 Comparison of mod function circuit using different adder

| ADDERS | RIPPLE CARRY ADDER | | CARRY SELECT ADDER | | CARRY LOOK AHEAD ADDER | | CARRY SAVE ADDER(PROPOSED) | |
|---------------------|--------------------|---------|--------------------|---------|------------------------|---------|----------------------------|---------|
| | MOD COLUMN | MOD ROW | MOD COLUMN | MOD ROW | MOD COLUMN | MOD ROW | MOD COLUMN | MOD ROW |
| No. of slices | 1 | 4 | 3 | 8 | 5 | 7 | 1 | 3 |
| No. of LUTS | 2 | 7 | 5 | 14 | 9 | 13 | 2 | 6 |
| No. of bonded IOB's | 8 | 10 | 8 | 11 | 9 | 11 | 9 | 12 |
| No. of GCLK's | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

The comparison table for mod function circuit are given in table 4. Since, the LUT approach adapts LUT in each stage rather than combinational logic, the design able to operate at high speed with increase in latency. Mod circuit using carry save adder increase the speed and efficiency by reducing the number of slices. The design is simulated on Xilinx 12.3 ISE to have a better comparison of the proposed work with the existing approaches in [1].

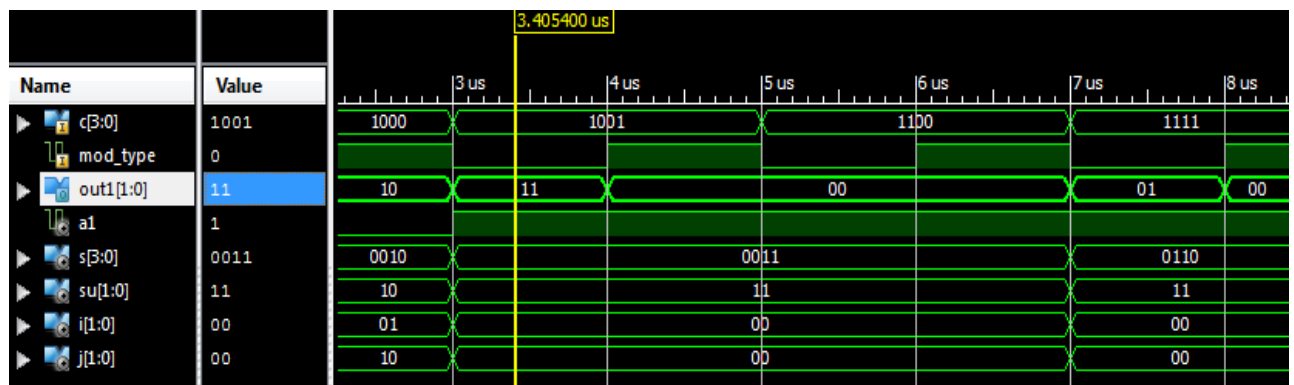


Fig 5 Simulation result for mod column circuit

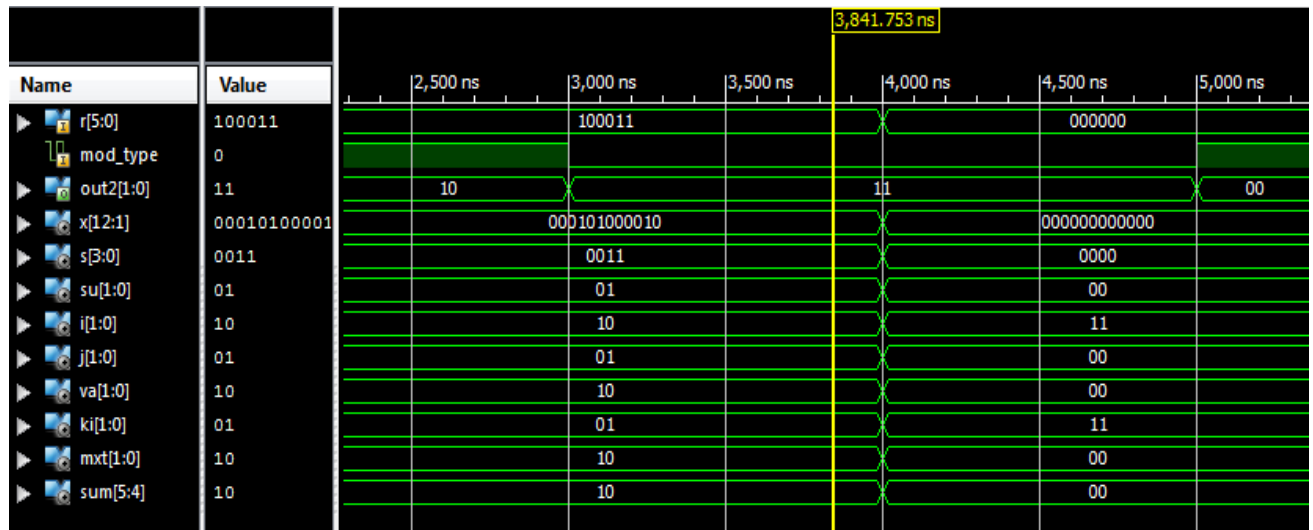


Fig 6 Simulation result for mod row circuit

VII. CONCLUSION

In this paper, an efficient mod function circuit for reconfigurable address generator architecture of multimode interleaver for IEEE 802.11a/g and 802.16e wireless standards supporting all possible code rates and modulation schemes has been presented. An efficient MOD row and a MOD column circuits were proposed to compute MOD function for row and column counter values. The synthesis results of the proposed MOD circuit using carry save adder shows significant reduction in resource utilization, improvement in operating speed compared with existing modulo algorithms and reduces the propagation delay.

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