

Performance Improvement of Low Power and Fast Full Adder by Exploring New XOR and XNOR Gates

M.loga Lakshmi, S.Jeya Anusuya M.E,(Ph.D), S.V.Sathyah

Department of Electronics and Communication Engineering, T.J.S Engineering College, Peruvoyal, India

HOD, Department of Electronics and Communication Engineering, T.J.S Engineering College, Peruvoyal, India

Assistant Professor, Department of Electronics and Communication Engineering, T.J.S Engineering College,
Peruvoyal, India

ABSTRACT: Adders are the main component in digital devices. In this work circuit for XOR/XNOR gates are used. The design of full adder using XOR/XNOR gates is used. This circuit design is highly optimized in terms of power and delay. This circuit is designed by using 65nm technology. So we designed a new circuit by using GDI technique. The design of full adder using GDI technique also reduces the transistor sizing, thereby it also reduces the power and speed. It is designed by using 18nm technology. Our observation shows the comparison of both techniques in tanner platform.

KEYWORDS: Full adder, GDI, XOR/XNOR, particle swarm optimization algorithm, transistor sizing.

I. INTRODUCTION

The electronic systems are inseparable part of every life. Recently, the industries are demand for low power, less area and high speed for designing the circuits. With improvement in technology and the enlargement of embedded system used electronic devices such as mobile, laptops, TV applications, power consumption, which is one of the limits in both high & low performance system, has become a primary focus in VLSI digital design. Due to increasing interest in low power ICs for portable measurement instrumentation, laptop computers cellular communications, etc., design choices which take into consideration low power features along with other circuit features are of the utmost importance. In our daily life, electronic systems are an inseparable part of everyday life. Digital circuits, microprocessors, digital communication devices, and digital signal processors, comprise a large part of electronic systems. As the scale of integration increases, the usability of circuits is restricted by the augmenting amounts of power and area consumption. Therefore, with the growing popularity and demand for the battery-operated portable devices such as mobile phones, tablets, and laptops, the designers try to reduce power consumption and area of such systems while preserving their speed. The analysis and comparison developed here have been carried out in terms of speed, power consumption and power-delay product (PDP). The investigation, which also includes the most interesting recently proposed one-bit full adders, has been based on simulation runs on a tanner environment.

GDI method is based on the use of a simple cell as shown in Fig. At a first glance the basic cell reminds the standard CMOS inverter, but there are some important differences: GDI cell contains 3 inputs - G (common gate input of NMOS and PMOS), P (input to the source/drain of PMOS) and N (input to the source/drain of NMOS).

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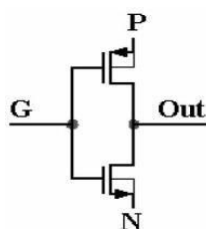


Fig: 1 GDI cell

II. LOGICS IN DESIGN OF LOW POWER

A) *CPL Logic (complementary pass transistor logic)* Every CPL has two output wires, both the positive signal and the complementary signal, eliminating the need for inverters. Complementary pass transistor logic or differential pass transistor logic refers to a logic family which is designed for certain advantage.

B) *Transmission Gate (TG) Logic*

A transmission gate is similar to a relay that can conduct in both directions or block by a control signal with almost any voltage potential.

It is a CMOS based switch, in which PMOS passes a strong 1 but poor 0, and NMOS passes strong 0 but poor 1. both PMOS and NMOS work simultaneously.

C) *DPL Logic (Double pass transistor logic)*

Double pass transistor logic (DPL) is a modified version of complementary pass transistor logic (CPL) that meets the requirement of reduced supply voltage designs. In DPL circuits full swing operation is achieved by simply adding PMOS transistors in parallel with the NMOS transistors.

D) *PTL Logic (Pass transistor logic)*

In electronics, pass transistor logic describes several logic families used in the design of integrated circuits. It reduces the count of transistors used to make different logic gates, by eliminating redundant transistors.

E) *PSO Algorithm*

The PSO algorithm maintains multiple potential solutions at one time. During each iteration of the algorithm, each solution is evaluated by an objective function to determine its fitness. Each solution is represented by a particle in the fitness landscape (search space). The particle "Fly" or "swarm" through the search space to find the maximum value returned by objective function.

III. DESIGN OF FULL ADDER USING XOR/XNOR

Six new hybrid 1-bit full-adder (FA) circuits based on the novel full-swing XOR–XNOR or XOR/XNOR gates and novel circuits for XOR/XNOR and simultaneous XOR– XNOR functions are introduced. Hybrid FAs are made of two modules, including 2-input XOR/XNOR (or simultaneous XOR–XNOR) gate and 2-to-1 multiplexer (2-1-MUX) gate.

A) REVIEW OF XOR/XNOR GATES

Hybrid FAs are made of two modules, including 2-input XOR/XNOR (or simultaneous XOR–XNOR) gate and 2-to-1 multiplexer (2-1-MUX) gate. The XOR/XNOR gate is the major consumer of power in the FA cell. Therefore, the power consumption of the FA cell can be reduced by optimum designing of the XOR/XNOR gate. The XOR/XNOR gate has also many applications in digital circuits design. Many circuits have been proposed to implement XOR/XNOR gate, which a few examples of the most efficient ones are shown in Fig. 3.1. It shows the full-swing XOR/XNOR gate circuit designed by double pass-transistor logic (DPL) style. This structure has eight transistors. The main problem of this circuit is using two high power consumption NOT gates on the critical path of the circuit, because the NOT gates must drive the output capacitance. Therefore, the size of the transistors in the NOT gates should be increased to obtain lower critical path delay. Furthermore, it causes the creation of an intermediate node with a large capacitance. Of course, this means that the NOT gates drives the output of circuit through, for example, pass transistor or TG.

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Therefore, the short-circuit power and, thus, the total power dissipation of this circuit are widely Increased. Moreover, in the optimum PDP situation, the critical path delay will also be increased slightly.

One of the most important issues in VLSI design is power consumption. With continuously increasing chip complexity and number of transistors in a chip, circuit's power consumption is growing as well. Higher power consumption raises chip temperature and directly affects battery life in portable devices as it causes more current to be withdrawn from the power supply. High temperature afflicts circuit operation and reliability.

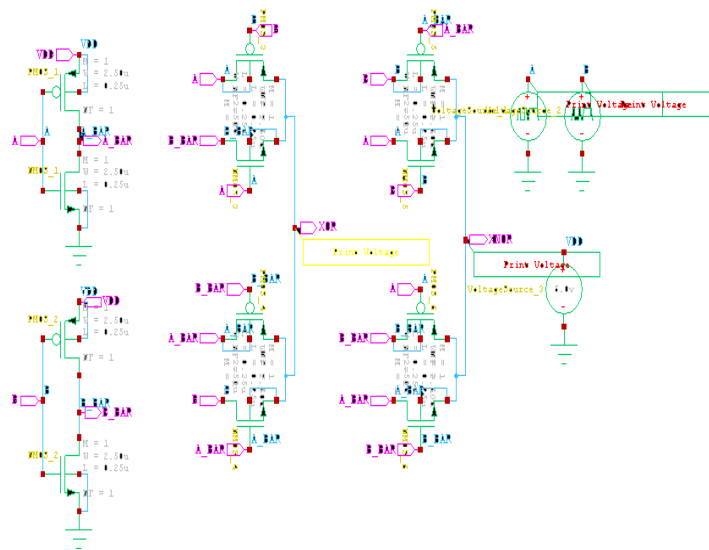


Fig 2(a) Full swing XOR/XNOR circuits (DPL logic)

The PTL logic of the full-swing XOR/XNOR gate shows that, each made of six transistors. This circuit is based on the PTL logic style, whose delay and power consumption are better than the circuit depicted in Fig. 3.1. The only problem of this structure is using a NOT gates on the critical path of the circuit. The XOR circuit of Fig. 3.2 has the lower delay than its XNOR circuit, because the critical path of XOR circuit is comprised of a NOT gates.

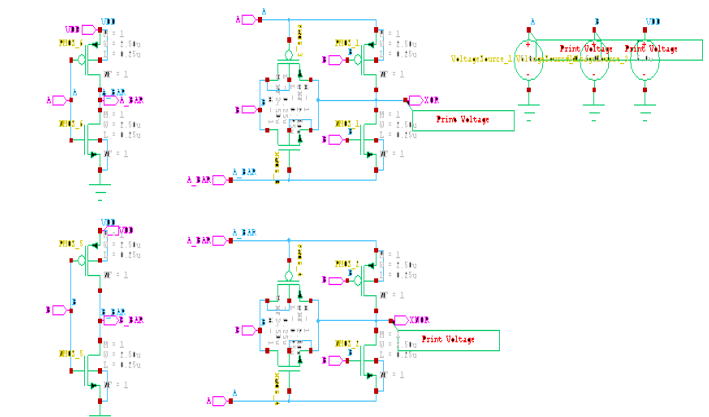


Fig 2(b) Full swing XOR/XNOR circuits (PTL logic)

The simultaneous XOR–XNOR circuit is widely used in hybrid FA structures. Commonly, in the hybrid FAs, the XOR–XNOR signals are connected to the inputs of 2-1-MUX as select lines. Therefore, two simultaneous signals with

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the same delay are necessary to avoid glitches in the output nodes of the FA. Fig. 3.3 shows an example of the simultaneous XOR–XNOR circuit. This circuit is based on the CPL logic style that has been designed by using ten transistors. In this structure, the outputs have been driven only by NMOS transistor, and thus, two PMOS transistors are connected to outputs (XOR and XNOR) as cross coupled to recover the output-level voltages. One problem of this XOR–XNOR circuit is to have the feedback (cross-coupled structure) on the outputs, which increases the delay and short-circuit power of this structure. Therefore, to mitigate the imposed delay, the size of transistors should be increased. Another disadvantage of this structure is the existence of two NOT gates in the critical path.

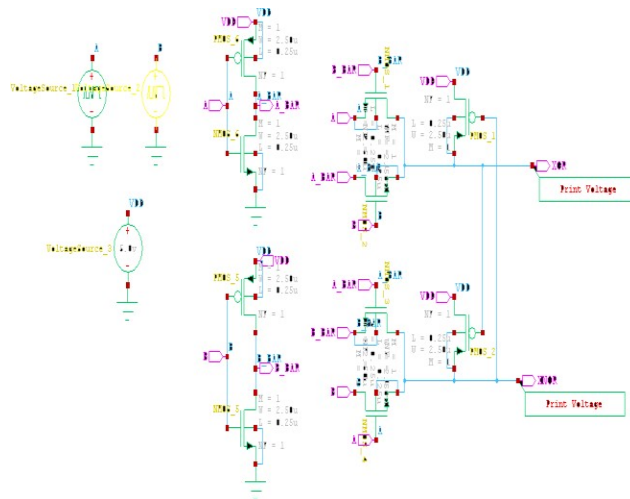


Fig 2(c) XOR/XNOR circuits (CPL logic)

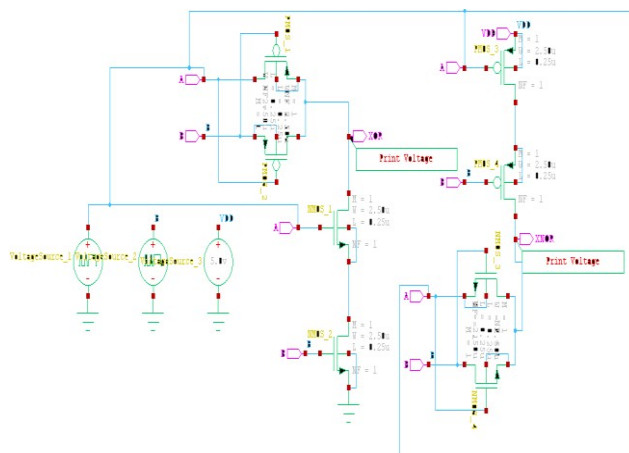


Fig 2(d) Non full-swing XOR/XNOR gates

The advantages of this structure are good driving capability, full swing output, and robustness against transistor sizing and supply voltage scaling. The main problem of this circuit is the structure of feedback that imposes extra parasitic capacitance to the XOR and XNOR output nodes. Thus, the delay and power consumption significantly increase.

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Combination of two XOR and XNOR circuits of Fig. 3.1 and 3.2 will result in two simultaneous XOR–XNOR gates. These new structures will have all advantages and disadvantages of their XOR/XNOR circuits. But, when the inputs change from AB=10 to AB=11, according to figures, we have

$$kN2 = WN2/W_{min}, kN3 = WN3/W_{min} \dots kP3 = WP3/W_{min}$$

$$RN2 = R_{min}/kN2, RN3 = R_{min}/kN3,$$

$$a = kN4 + kP2 + kP3$$

$$CX = C_{min} \times kN2 + C_{dmin} \times kN3 = C_{dmin}(kN2 + kN3) \quad C_{OUT} = C_{dN4} + C_{dP2} + C_{dP3} + C_{dmin} \times kN2$$

$$C_{OUT} = a \times C_{dmin} + C_{dmin} \times kN2 = C_{dmin}(a + kN2)$$

Where W_{min} is the minimum transistor width, R_{min} is the resistance,

C_{dmin} is the diffusion capacitance of transistor, A is the total size of transistor P2, P3 and N4.

The Elmore delay ($T_{dmin}=10 \rightarrow 11$) is $T_{dAB=10 \rightarrow 11} = C_{OUT} (R_{min}/kN2) + (R_{min}/kN3) + CX (R_{min}/kN3)$

$= C_{dmin} R_{min} [a (1/kN2) + (1/kN3) + 2(1 + kN2/kN3)]$ By calculating power,

$$P_{AB=10 \rightarrow 11} = C_{TOTAL} V^2 = [C_{dmin}(kN2 + kN3) + C_{dmin}(a + kN2) + kN3 C_{gmin} + kP2 C_{dmin} + kP3 C_{gmin} + kN4 C_{dmin}] V^2$$

$$+ kP2 C_{dmin} + kP3 C_{gmin} + kN4 C_{dmin}] V^2$$

$$+ kP2 C_{dmin} + kP3 C_{gmin} + kN4 C_{dmin}] V^2 \quad DD$$

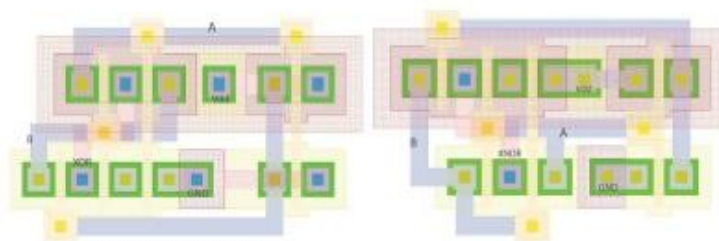


Fig 3 Circuit layout of existing XOR/XNOR. (e) Circuit layout existing XNOR

IV. SIX NEW HYBRID FULLADDER

These new full adder have been employed with hybrid logic style, and all of them are designed by using the XOR/XNOR circuits. The well-known four-transistor 2-1 MUX structure is used to implement the existing hybrid FA cells.

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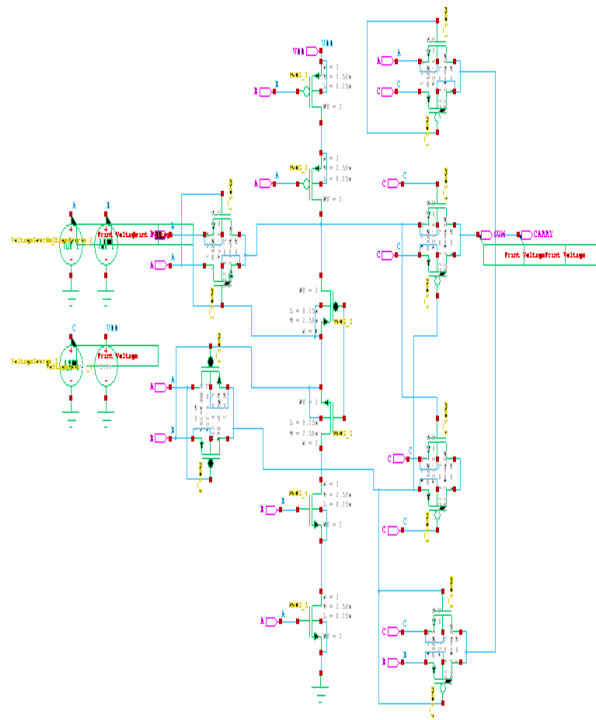


Fig 3(a) Hybrid full adder design of HFA-20T using XOR/XNOR logic

Here we are using input supply; inverter and output supply Print voltage is used to display the waveforms. This circuit is based on the combination

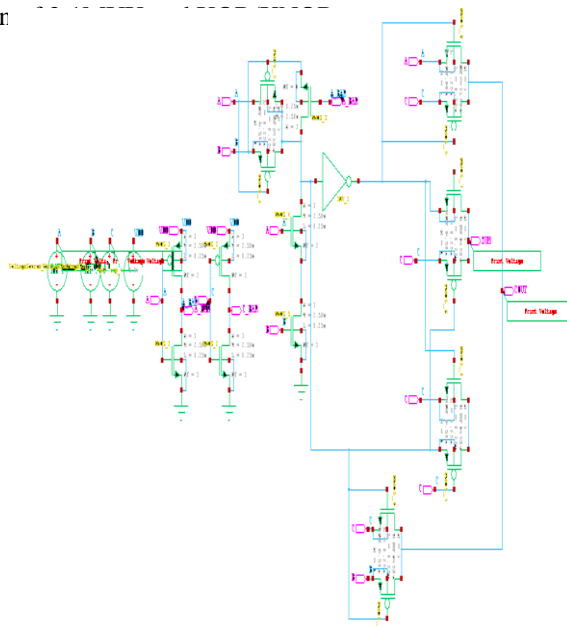


Fig 3(b) Hybrid full adder design of HFA-17T using XOR/XNOR logic

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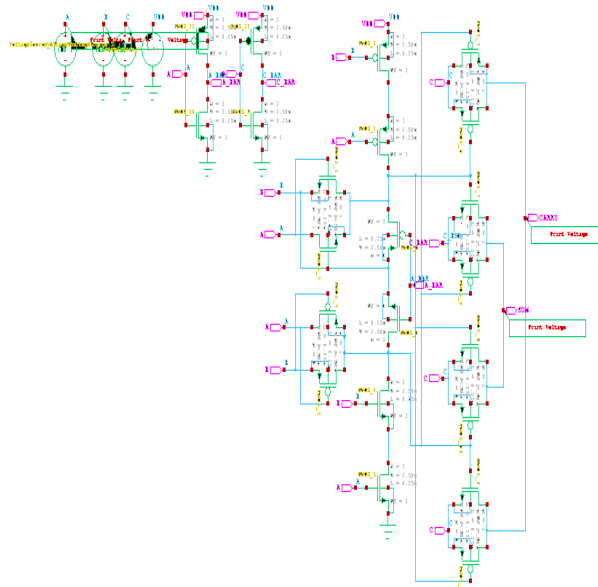


Fig 3(c) Hybrid full adder design of HFA-B-26T using XOR/XNOR logic

We are using input supply; inverter and output supply Print voltage is used to display the waveforms. This circuit is based on the combination of 2:1MUX and XOR/XNOR gates.

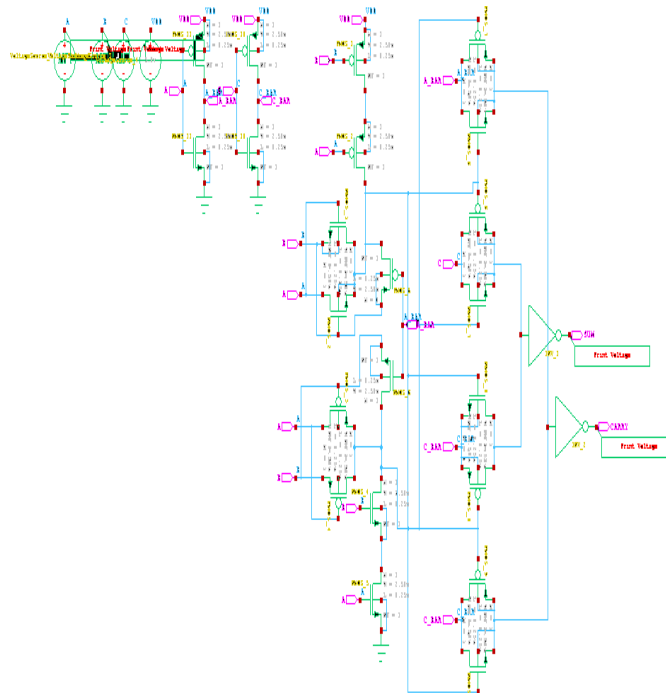


Fig 3(d) Hybrid full adder design of HFA-NB-26T using XOR/XNOR logic

This circuit is based on the combination of 2:1MUX and XOR/XNOR gates. We are using input supply; inverter and output supply. Print voltage is used to display the waveforms.

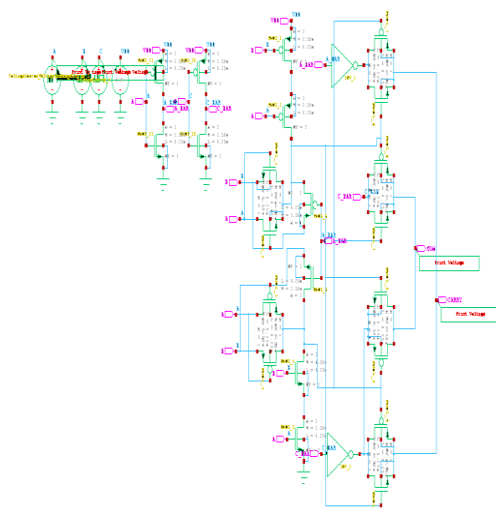


Fig 3(e) Hybrid full adder design of HFA-22T using XOR/XNOR logic

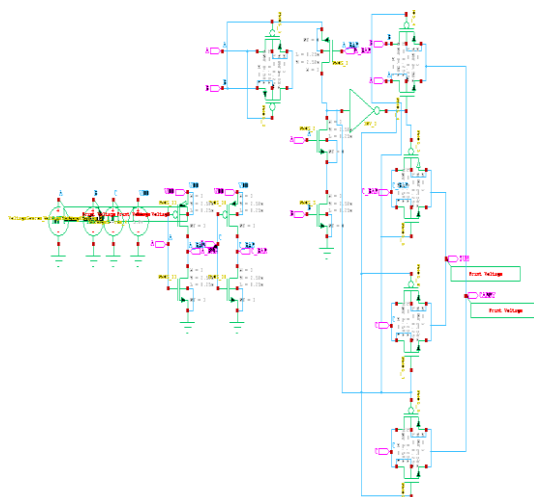


Fig: 3(f) Hybrid full adder designs of HFA-19T using XOR/XNOR logic

Due the increased count of transistor it leads to high power and also it increases the heavy delay in the circuit. Increase in transistor count increases delay and power consumption. All the above circuits have been simulated using HSPICE in the 65-nm TSMC CMOS process technology. The evaluation revealed that using the NOT gates on the critical path of a circuit is a drawback. Another disadvantage of a circuit is to have a positive feedback on the outputs of the XOR–XNOR gate for compensating the output voltage level. This feedback increases the delay, output Capacitance, and, as a result, energy consumption of the circuit.

A) Method for Transistor Sizing

The above mentioned methods do not consider the dependence of transistors and, therefore, do not have good accuracy. There are different ways to optimize a function, which one of these methods is particle swarm optimization (PSO). In computer science, the PSO algorithm is a numerical computation method that optimizes a function iteratively. The PSO

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algorithm is becoming popular due to its simplicity of implementation and ability to rapidly converge to a good solution.

B) PVT Variation Test Setup

PVT variations cause changes in the parameters of the transistor, such as threshold voltage, capacitances, and ON- and OFF-state currents. These changes will have the effect on the performance of the circuit. Therefore, the robustness of different FA cells should be investigated in unfavorable and unknown conditions. To reach this purpose, the Monte Carlo transient analysis for W , L , and V_{th} variations, as well as process corners simulation is performed.

C) Noise Immunity Test Setup

Noise in VLSI circuits is defined as any disturbance that changes the voltage of circuit nodes from their nominal value. Noise sources that have a significant impact on the performance of digital circuits consist of crosstalk, alpha particles, skin effect, electron migration, electromagnetic interference, IR drop, charge sharing, charge leakage, ground bounce, power supply noise, and so on. Digital circuits are inherently very low sensitive to noise, and they filter the noise pulses with high amplitude and adequate narrow width.

D) Performance Analysis against VDD

The delay, power, and PDP of the FA cells at supply voltage range from 0.65 to 1.5 V are shown in Fig. 3.1(a)–(c), respectively. The nominal supply voltage for the 65-nm TSMC CMOS process technology is 1.2 V. Also, the transistor sizes optimized at 1.2 V are used for the simulation at all supply voltage ranges. The simulation results confirm that the proposed designs have superior speed, power, and PDP than other FA designs. The 14T, 16T, DPL, and New- HPSC FAs, due to the threshold voltage drop problem, can only work at and above 0.95, 0.75, 0.7, and 0.7 V, respectively.

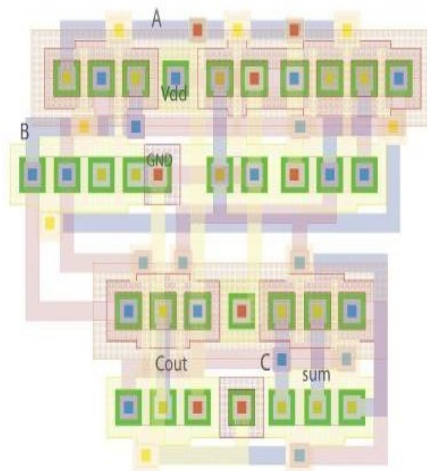


Fig. 4 Circuit layout of HFA-20T using XOR/XNOR logic

V. DISADVANTAGES

- Power consumption and delay is more due to increased transistor count.
- The power consumption gets worst with increasing the power supply.
- The power delay product is increased with supply voltage due scattering effects at higher temperatures.
- Full adder is designed in CMOS technology using XOR/XNOR logic.
- Had been simulated in 45nm technology.

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VI. DESIGN OF FULL ADDER USING GDI TECHNIQUE

A) Full swing circuit design

In this design full adder consists of two XOR gate cells and one cell of 2x1 multiplexer (MUX). The performance of the proposed design compared with the different logic style for full adders. The proposed full adder design dissipates low power, while improving delay and power delay product among all the design taken for comparison.

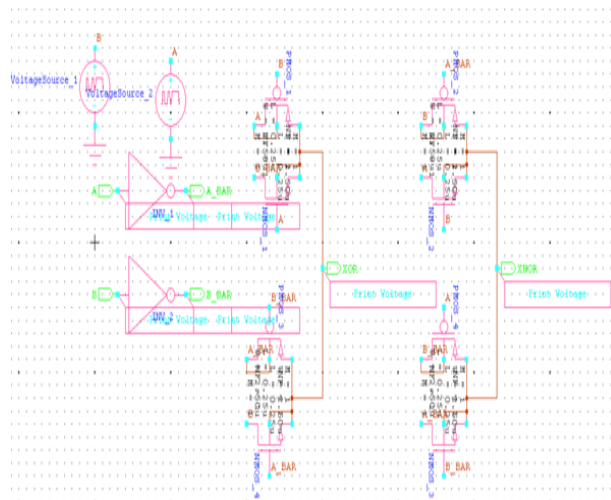
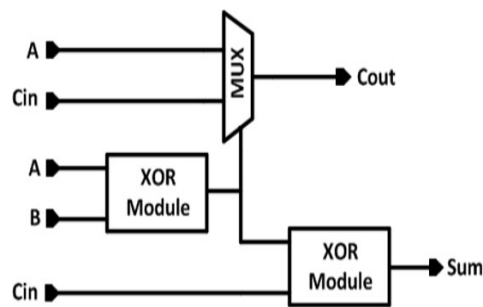


Fig: 5 Full swing 1-bit full adder circuit using GDI technique

Fig: 5(a) GDI based Full swing XOR/XNOR circuits.

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Five different non full-swing GDI full adders have been designed with transistor count of 16T, 14T, 12T, 10T and 8T. For 16T GDI full adder implemented from the Boolean expression, the sum expression is designed using 3-input XOR gate, whereas carry expression is designed using 2-input AND and 3-input OR gate.

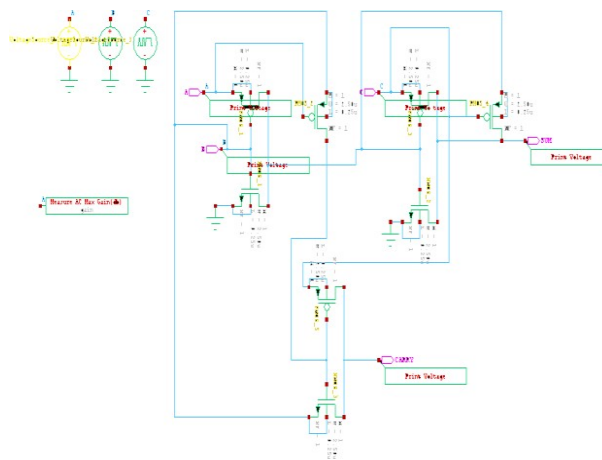


Fig 5(b) Hybrid full adder design of HFA-8T using GDI technique

Here we are using input supply; inverter and output supply Print voltage is used to display the waveforms. This circuit is based on the combination of 2:1MUX and XOR/XNOR gates.

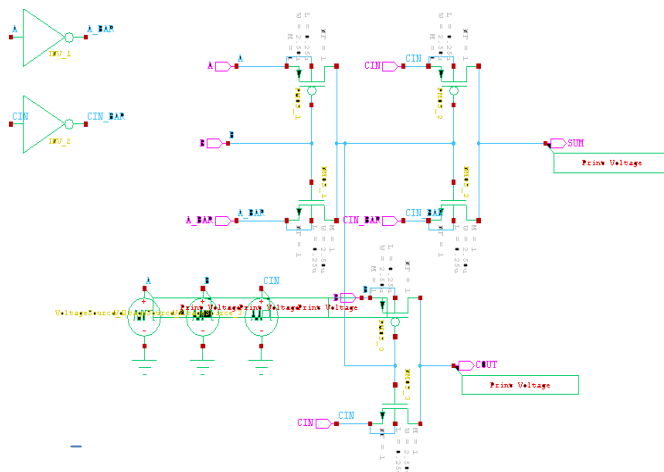


Fig 5(c) Hybrid full adder design of HFA-10T using GDI technique

This circuit is based on the combination of 2:1MUX and XOR/XNOR gates. The 10T GDI full adder from the Boolean expression, sum is designed with 2-input XOR, 2-input XNOR and 2-to-1 MUX, and carry is designed with 2-to-1 MUX. By reducing the transistor sizing using GDI technique the Power consumption is reduced, thereby delay is minimum and also the output driving capability is maximum. All the above circuits have been simulated using HSPICE in the 18- nm TSMC CMOS process technology.

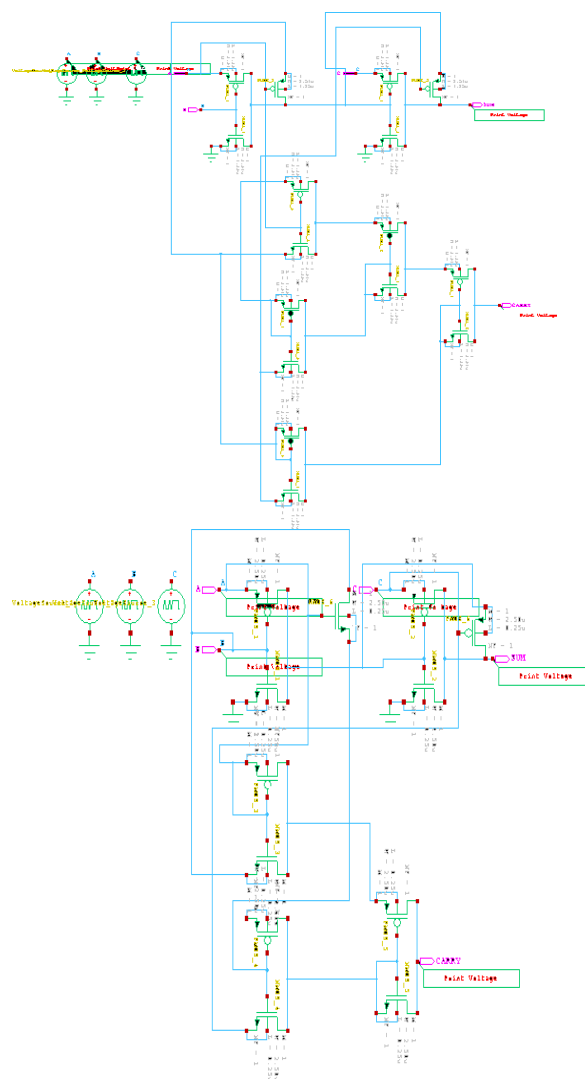


Fig 5(d) Hybrid full adder design of HFA-12T using GDI technique

For 12T GDI full adder from the expressions, sum is realized using 3-input XOR gate and carry is realized using 2-input OR and 2-input AND. By reducing the transistor sizing using GDI technique the Power consumption is reduced, thereby delay is minimum and also the output driving capability is maximum. Here the print voltage is used to display the output voltage.

These circuits have been simulated using HSPICE in the 18- nm TSMC CMOS process technology.

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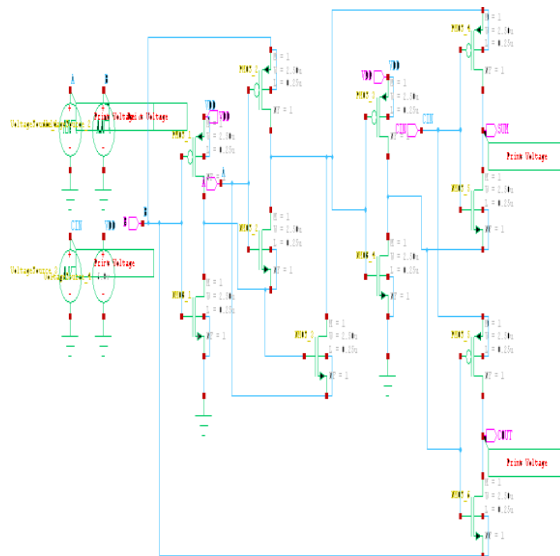


Fig 5(e) Hybrid full adder design of HFA-11T using GDI technique
Fig 5(f) Hybrid full adder design of HFA-16T using GDI technique

This circuit is based on the combination of 2:1MUX and XOR/XNOR gates. The 16T GDI full adder from the expressions, sum is designed with 2-input XOR, 2-input XNOR and 2-to-1 MUX, and carry is designed with 2-to-1 MUX. Hybrid FAs are made of two modules, including 2- input XOR/XNOR (or simultaneous XOR–XNOR) gate and 2-to-1 multiplexer (2-1-MUX) gate. The XOR/XNOR gate is the major consumer of power in the FA cell. Therefore, the power consumption of the FA cell can be reduced by optimum designing of the XOR/XNOR gate. The XOR/XNOR gate has also many applications in digital circuits design.

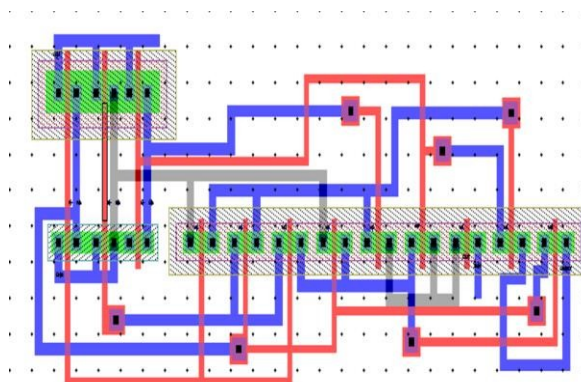


Fig: 6 Circuit layout of HFA-11T using GDI technique

VII. ADVANTAGES

- The proposed circuit can also work for wide range of inputs.
- Had been simulated in 18nm technology.

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DESIGN	DESIGN OF FULL ADDER DESIGN USING XOR/XNOR GATES			DESIGN OF FULL ADDER DESIGN USING GDI TECHNIQUE		
	POWER	DELAY	PDP	POWER	DELAY	PDP
DPL Logic	4.062×10^{-6}	1.083×10^{-8}	4.399×10^{-14}	2.633×10^{-6}	1.0825×10^{-8}	2.856×10^{-14}
PTL Logic	2.247×10^{-6}	1.092×10^{-8}	2.245×10^{-14}	1.1407×10^{-6}	1.0083×10^{-8}	1.1501×10^{-14}
HFA-17T	9.169×10^{-6}	1.132×10^{-7}	10.37×10^{-13}	8T 1.0087×10^{-6}	9.145×10^{-9}	9.2245×10^{-15}
HFA-19T	4.349×10^{-4}	1.408×10^{-8}	6.123×10^{-12}	10T 1.150×10^{-6}	1.900×10^{-8}	2.1850×10^{-14}
HFA-20T	4.454×10^{-4}	9.328×10^{-8}	37.09×10^{-12}	11T 1.180×10^{-6}	9.197×10^{-9}	10.852×10^{-14}
HFA-22T	8.876×10^{-4}	1.030×10^{-7}	9.142×10^{-11}	12T 4.43×10^{-8}	9.370×10^{-9}	41.509×10^{-17}
HFA-B-26T	8.808×10^{-4}	4.408×10^{-7}	38.82×10^{-11}	14T 1.270×10^{-8}	1.057×10^{-8}	1.3423×10^{-16}
HFA-NB-26T	4.712×10^{-4}	1.041×10^{-8}	4.909×10^{-12}	16T 6.280×10^{-4}	1.180×10^{-8}	7.4104×10^{-12}

TABLE I PERFORMANCE COMPARISON TABLE

VIII. CONCLUSION

This work presents a 1-bit Full Adder designed in 22nm TSMC process using the Full-Swing GDI technique and simulated using the Tanner EDA simulator. Simulation results showed design in terms of power consumption and transistor count, while maintaining Full-Swing Operation. The proposed design consists of 10 transistors and operates under 1V supply voltage. So far work completed in Tanner platform. Both proposed is compared with conventional work (base work).Its proving better result when compare with existing work .After base work architecture implementation the following results are achieved. We successfully achieved a much higher throughput with a lower GDI total area. A comparison with previous designs for area, speed, and power efficiency has been given achieved.

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