



e-ISSN: 2319-8753 | p-ISSN: 2320-6710

IJIRSET

International Journal of Innovative Research in
SCIENCE | ENGINEERING | TECHNOLOGY

INTERNATIONAL JOURNAL OF INNOVATIVE RESEARCH

IN SCIENCE | ENGINEERING | TECHNOLOGY

Volume 9, Issue 12, December 2020

ISSN INTERNATIONAL
STANDARD
SERIAL
NUMBER
INDIA

Impact Factor: 7.512

9940 572 462

6381 907 438

ijirset@gmail.com

www.ijirset.com

A Novel Design of Modified Asymmetric Multilevel Inverter for Power Maximization

Dr.R.Subramaniyan

Professor, Dept. of EEE, International Maritime Academy, Chennai, India

ABSTRACT: In present day industrial scenario, the demand of multilevel inverter is growing rapidly in the field of power conversion i.e. from DC/AC, AC/DC & DC/DC, conversion of frequency with varying output etc. & their applications. The main drawback of multilevel inverters is that it requires a high number of switching devices that leads to complexity in their control. Hence, the concept of reduced switch count is introduced in this paper in order to minimize the size of hardware, maximizing output power and also reducing the cost and complexity of hardware. A modified structure of asymmetric multilevel inverter topology is prescribed. It is planned with the point of lessening the quantity of switches with increased number of levels at the output. Proposed topology utilizes three asymmetrical dc voltage sources alongside, ten power semiconductor switches to accomplish thirteen levels at the output. Compared to the conventional topologies, the proposed inverter has less number of switches as well as less harmonics content. Transformer based multilevel inverter is expected to give the isolation protection. The proposed cascaded H-bridge topology has high efficiency as well as balanced power distribution quality. MATLAB/SIMULINK results have been given to prove the proposed topology.

KEYWORDS: multi level inverter, THD, CHB topology, power

I. INTRODUCTION

The idea of multilevel inverter (MLI) advanced path back in 1981 with creators of [1] proposing a topology for expanding the quantity of levels in a traditional two level inverter enhancing the power quality. These converters have a multilevel voltage with n number of steps instead of a sinusoidal waveform created from connecting few dc voltage sources symmetrically and asymmetrically under various dynamic conditions. Additionally, the inalienable issue of fast change in voltage level in the

customary two level partner which causes huge electromagnetic interference (EMI) is dealt with in the multilevel inverter that results in lower level of switching voltage [2]–[4]. The multilevel inverter is also suitable for solar application, power quality improvement using FACTS devices, grid connected system. Few MLI topologies are additionally utilized in electric vehicle for regenerative braking. The unpredictability in hardware because of generous number of switches and usage of numerous dc sources in MLI have open up ways for research to lessen them. There has been a thorough research proceeding to diminish the quantity of electronic switches and dc source utilized in MLI without bargaining with the quantity of output levels. The research attempt has been stepped comprehensively into discovering more uptodate topologies for accomplishing the above targets and contriving appropriate circuit for multilevel attenuation [5-7].

Traditional MLI incorporate diode or Neutral Point Clamped (NPC), flying capacitor (FC) and cascaded H bridge (CHB) MLI topology. The CHB topology is viewed as less complex, dependable and measured as expanding the level of output voltage requires progressively number of units increases. The CHB topology has engrossed researchers consideration due to a few deficiencies related with NPC and FC including enormous capacitor necessity, unbalancing in the dc connections and huge burden on the power switches[8-10]. CHB topology is classified as symmetrical CHB converter and asymmetrical CHB converter. Symmetrical CHB converter employs various equivalent dc voltage sources while asymmetrical CHB utilizes inconsistent voltage sources[10-12]. An asymmetrical CHB design acquires more noteworthy number of levels at the output voltage with same number of parts contrasted with the symmetrical CHB which increases the reliability of the system. A few research work has been done in writing, prominently on novel topologies for symmetrical CHB converter and asymmetrical CHB converter setup utilizing isolated dc voltage sources and the association of H-bridge circuits.

II. PROPOSED SYSTEM

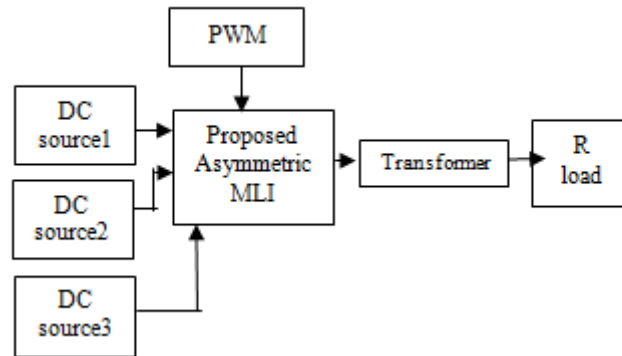


Fig 1. Block Diagram of Proposed System

In proposed system shown in figure 1 consists of three asymmetrical DC source in the ratio 1:2:3 fed to the proposed asymmetric MLI. The asymmetric MLI have the capability of producing 13 level of output voltage with the help of simple PWM control techniques. The transformer is used for the isolated protection circuit.

III. MODELS

A. Proposed asymmetric MLI

The proposed asymmetric MLI shown in figure 2 consists of dual unit structure. One unit is responsible for the generation of voltage levels and other is responsible for the generation of AC waveform by changing the polarity of current flow through the load. The switches Q1-Q5 are responsible for the 13 level output and H1-H4 are responsible positive and negative polarity waveform.

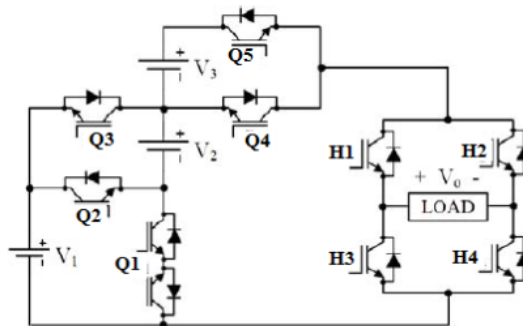


Fig 2. Circuit diagram of proposed asymmetric MLI

The circuit operation involves when switches H1&H4 are ON the positive cycle is produced likewise when the switched H2&H3 are ON the negative cycle is produced. When switches Q3&Q4 are ON the V_1 (2nd level) and $-V_1$ (8th level) are produced. Q1&Q4 are turned ON simultaneously to get the V_2 (3rd level) and $-V_2$ (9th level) are produced. Q2&Q4 are turned ON to produce the (V_1+V_2) 4th and $-(V_1+V_2)$ 10th level of output voltage. Q3&Q5 are turned ON to generate the (V_1+V_3) 5th and $-(V_1+V_3)$ 11th level. Q1&Q5 are turned ON to generate (V_2+V_3) 6th and $-(V_2+V_3)$ 12th level. The $(V_1+V_2+V_3)$ 13th& $-(V_1+V_2+V_3)$ 7th level is attained by turning ON the switches Q2&Q5. In 1st level output voltage is 0 so all the level generation switches are turned OFF during this period of level generation.



The common structure equation is given by,

$$\text{Number of switches} = \frac{1}{3}[\text{Number of levels} + 17] \quad (1)$$

$$\text{Number of sources} = \frac{1}{6}[\text{Number of levels} + 5] \quad (2)$$

The table 1 shows the switching table for the proposed asymmetric MLI switches. Figure 3 depicts the switching signals.

Table 1. Switching table

Q1	Q2	Q3	Q4	Q5	H1	H2	H3	H4	LEVEL
0	0	0	0	0	1	1	0	0	1
0	0	1	1	0	1	0	0	1	2
1	0	0	1	0	1	0	0	1	3
0	1	0	1	0	1	0	0	1	4
0	0	1	0	1	1	0	0	1	5
1	0	0	0	1	1	0	0	1	6
0	1	0	0	1	1	0	0	1	7
0	0	0	0	0	0	0	1	1	1
0	0	1	1	0	0	1	1	0	8
1	0	0	1	0	0	1	1	0	9
0	1	0	1	0	0	1	1	0	10
0	0	1	0	1	0	1	1	0	11
1	0	0	0	1	0	1	1	0	12
0	1	0	0	1	0	1	1	0	13

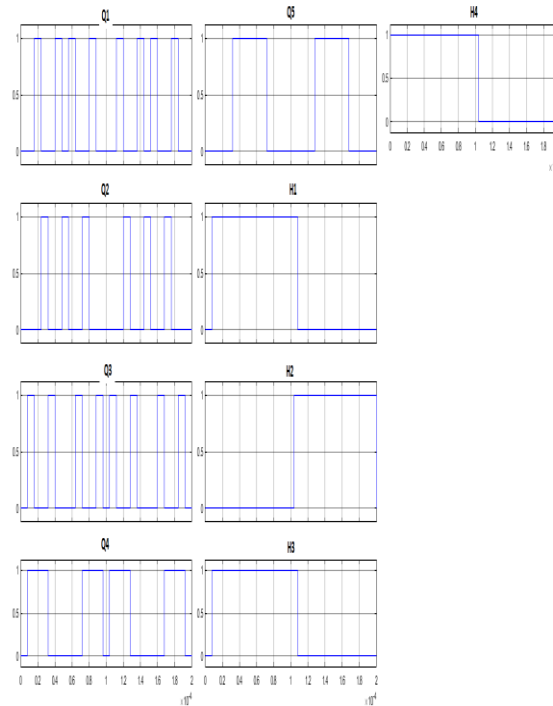


Fig 3. Switching signals for Switches

The proposed converter operated at low switching frequency of 5000Hz which reduces the stress on the switch. The simple PWM is used for the pulse generation which generates the required pulse based on the delay time period and pulse width which is specified manually in pulse generator block in MATLAB/SIMULINK. The linear transformer which has the turns ratio of 1:1 which neither step up nor step down voltage serves as isolation for protection.

IV. COMPARISON OF CONVENTIONAL AND MODIFIED MLI

Conventional	Modified
Conventional cascaded multilevel inverter consists of 28 switches	Modified MLI consists of only 9 switches
Conventional cascaded multilevel inverter consists of 7 sources	Modified mli consists of only 3 sources
Conventional inverter are symmetrical	Modified MLI are asymmetrical
Conventional inverter works on high frequency which is on khz	Modified MLI are works on low switching frequency

V. SIMULATION RESULTS

Figure 4 shows the overall simulation diagram of proposed asymmetric MLI which produces 13 level output voltage of $V_0=60V$ with three different sources of $V_1=10V$, $V_2=20V$, $V_3=30V$

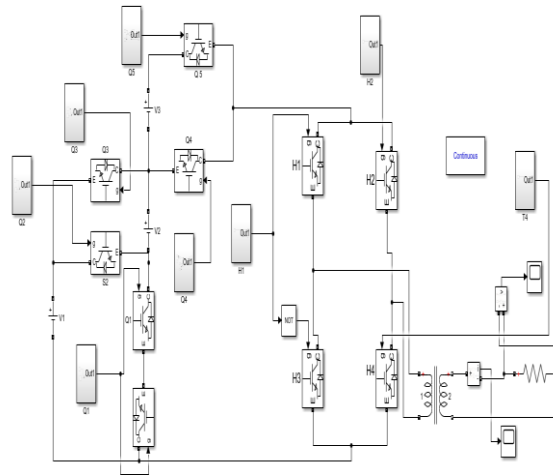


Fig 4. Overall Simulation Diagram

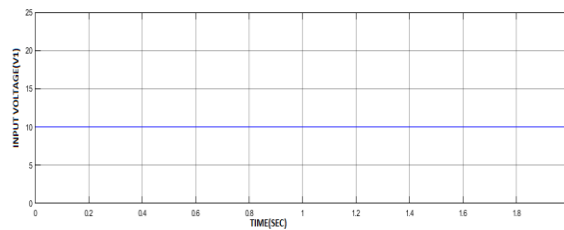


Fig 5. Input voltage1

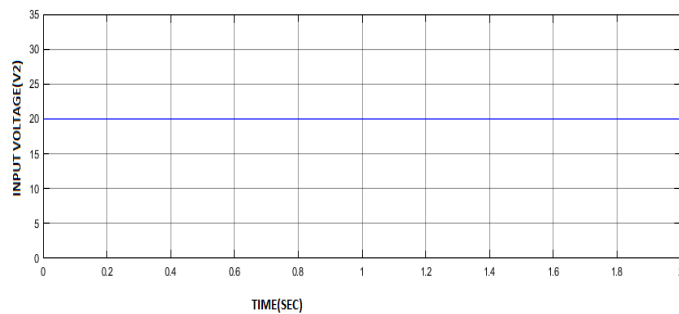


Fig 6. Input voltage2

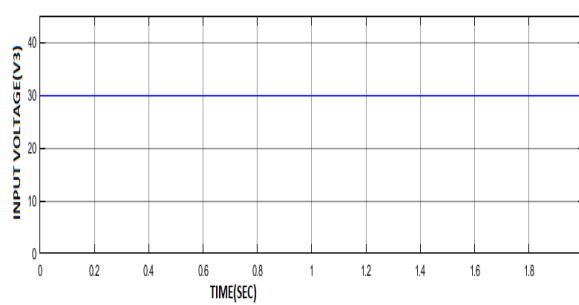


Fig 7. Input voltage3

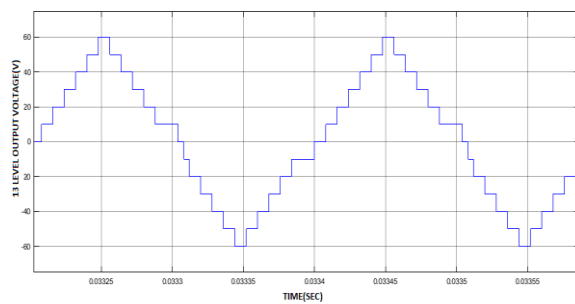


Fig 8. Level output voltage of proposed asymmetric MLI

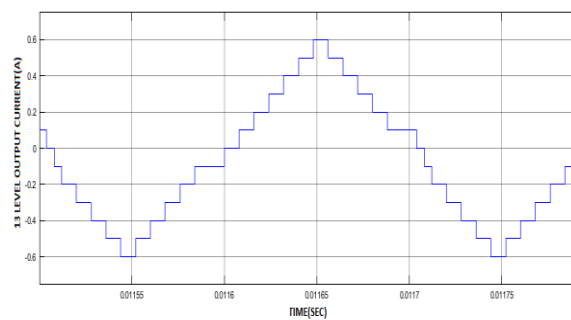


Fig 9 Level output current of proposed asymmetric MLI

Figure 5,6&7 shows the input voltage 1,2&3 respectively. Figure 8&9 shows the 13 level output voltage and output current waveform. The total harmonic distortion(THD) value shown in figure 10 is evaluated using FFT analysis which shows the value of 5.86%

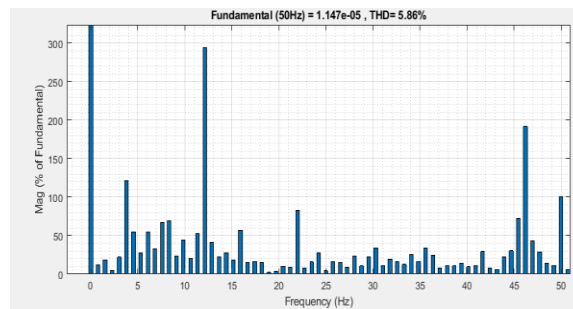


Fig 10. THD percentage

The power efficiency is calculated as,

$$\text{Input power} = v_{in} \cdot i_{in}$$

$$V_{in} = 60V$$

$$I_{in} = 0.6A$$

$$V_{in} \cdot I_{in} = 60 \cdot 0.6 = 36W$$

$$\text{Output power} = V_{out} \cdot I_{out}$$

$$V_{out} = 59.9V$$

$$I_{out} = 0.59A$$

$$V_{out} \cdot I_{out} = 59.9 \cdot 0.59 = 35.3W$$

$$\begin{aligned}\text{Power efficiency} &= (P_{out}/P_{in}) * 100 \\ &= (36/35.3) * 100 \\ &= 98\%\end{aligned}$$

The overall efficiency of the system is **98%**

VI. CONCLUSION

This paper presented a modified asymmetric MLI with isolated protection which also implemented with simple PWM control technique. The presented topology has the advantages of less reduced switch count which increases the cost effectiveness of the system. The proposed MLI exhibits the less harmonic distortion with the value of 5.86% and it can operate at low switching frequency which increases the reliability of the system. The power efficiency is also increase with balance power distribution systems.

REFERENCES

- [1] A. Nabae, I. Takahashi, and H. Akagi, "A New Neutral-Point-Clamped PWM Inverter," IEEE Trans. Ind. Appl., vol. IA-17, no.5, pp. 518–523, 1981.
- [2] H. Akagi, "Multilevel Converters: Fundamental Circuits and Systems," Proc. IEEE, vol. 105, no. 25249029, pp. 2048–2065, 2017.
- [3] S. Kouro et al., "Recent Advances and Industrial Applications of Multilevel Converters," IEEE Trans. Ind. Electron., vol. 57, no. 8, pp. 2553–2580, 2010.
- [4] R. A. Ahmed, S. Mekhilef, and H. W. Ping, "New multilevel inverter topology with minimum number of switches," IEEE Reg. 10 Annu. Int. Conf. Proceedings/TENCON, pp. 1862–1867, 2010
- [5] J. Rodriguez, J.S. Lai, F.Z. Peng. "Multilevel Inverters: A Survey of Topologies, Controls and Applications," IEEE Trans. Ind. Electron., 2002, vol. 49, no. 4, pp. 724-738.
- [6] E. Colak, R. Kabalci, R. Bayindir. "Review of multilevel voltage source inverter topologies and control schemes," Energy Conversion and Management, 2011, vol. 52, pp. 1114-1128.
- [7] A.K. Panda, Y. Suresh, "Performance of cascaded multilevel inverter by employing single and three-phase transformers," IET Power Electron., vol. 5, no. 9, pp. 1694-1705, 2012.
- [8] A.K. Panda, Y. Suresh, "Research on cascade multilevel inverter with single DC source by using three-phase transformers," Electrical Power and Energy Systems, vol. 40, 2012, pp. 9-20.
- [9] J. Pereda, J. Dixon, "High-Frequency Link: A Solution for Using Only One DC Source in Asymmetric Cascaded Multilevel Inverters," IEEE Trans. Ind. Electron., vol. 58, no. 9, 2011, pp. 3884-3892.
- [10] E. Babaei, M. Sadegh, "Asymmetric Cascaded Multilevel Inverter with Charge Balance Control of a Low Resolution Symmetric Subsystem," Energy Conversion and Management, 2010, vol. 51, pp. 2272-2278.
- [11] Farakhor, R. Reza Ahrabi, H. Ardi and S. Najafi Ravadanegh, "Symmetric and asymmetric transformer based cascaded multilevel inverter with minimum number of components," IET Power Electron., vol. 8, no. 6, pp. 1052-1060, Jun. 2015.
- [12] M.R. Banaei, H. Khounjahan, E. Salary, "Single-source cascaded transformers multilevel inverter with reduced number of switches," IET Power Electron., vol. 5, no. 9, 2012, pp. 1748-1753.

BIOGRAPHY



Dr. R. Subramanian, working as Professor in the Department of Electrical and Electronics Engineering, International Maritime Academy, Chennai. He received B.E. Degree in Electronics and Communication Engineering from University of Madras in the year 1995. He received M.E and Ph.D Degrees in Electrical Engineering in the year 2005 and 2016 respectively from Anna University, Chennai. He has 23 years of teaching experience in Engineering colleges. He has published several papers in International and National journals. His area of interest includes Electrical Drives, Embedded Systems, DSP. He is Member of IEEE, Fellow of IETE and Life member of ISTE.



INNO SPACE
SJIF Scientific Journal Impact Factor

**Impact Factor:
7.512**

ISSN INTERNATIONAL
STANDARD
SERIAL
NUMBER
INDIA



INTERNATIONAL JOURNAL OF INNOVATIVE RESEARCH

IN SCIENCE | ENGINEERING | TECHNOLOGY

 9940 572 462  6381 907 438  ijirset@gmail.com



www.ijirset.com

Scan to save the contact details