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IOT Application development on Artix 7 FPGA and Thingspeak IOT Cloud

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ABSTRACT: FPGA with Internet of Things is a latest technology, and this technique has been used to introduce many smart devices with wonderful applications in our day today life. One more challenge for IOT is to handle vast amount of sensing the data generated from smart devices that are resource limited and subject to missing data due to link failures. In this paper mainly going to focus on FPGA with IOT platform, i.e., the use of low-cost FPGA implementation of entire IOT subset including TCP/IP protocol, Control System and Data Acquisition etc. In the past few years, we have enormous improvement in the field of IOT applications on FPGA platform. This technique has been updated with low cost, efficient power usage with real time observing and remote recognizing system. The main objective of this research is to focus how the FPGA based hardware resources can be accessed from anywhere. The maintenance cost of servers can be reduced by building a cloud-based monitoring system. The data losses are avoided with the help of this technique. To make the communication with various internets coupled devices (computer, tablet, mobile phone) at the same time anywhere in the world. There are various business spaces it needs you to observe temperature, light and update the status to the cloud. The temperature, light must be maintained at the moderate level in food preservation process. IOT based temperature, light monitoring system help us to monitor the food preservation system and update the data to the cloud at the regular interval. Artix-7 is latest series of FPGA for complex VHDL design with new VIVADO platform.

KEYWORDS: IOT, Thingspeak, Temperature and Light Monitoring System, Artix-7 FPGA, Vivado 2018.

I. INTRODUCTION

Web services with FPGA based hardware have already been realized and defined. Their embedded nature permits the developers to simply adjust those services to energetically interrelate with their surroundings, e.g., to attain real-world measurement data or control various actuators. Such entities can be called environmentaware web services in difference to classical web services that work on remote physical or virtual machines. The IOT applications can be developed by implementing IP address with the particular VHDL code in order to make Internet of Things.

IOT is implemented on various FPGA devices to project diverse devices for various applications. As the number of IOT devices are increasing fast, results the need to build a smart world of devices with less human stimuli [7]. General idea of IOT is to assign an IP address to a relative device to be pinged out from inaccessible distance, broadly used for real time data collection [14].

Internet of Things

The internet has enabled an unpredictable growth of information sharing with the introduction of embedded and sensing technology, the number of smart devices including sensors, mobile phones, RFIDs, and smart grids has grown quickly in recent years. Ericsson and Cisco predicted that fifty billion small, embedded sensors and actuators will be associated with the internet by 2020 [15].

Artix-7 FPGA

The Field Programmable Gate Array (FPGA) is a family of reconfigurable hardware, where Field Programmable means the operation changing capability in the field, and Gate Array means the construction of basic internal architecture of the device. Digital computing tasks can be developed in software and compiled into a bit stream



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file. This bit stream file contains information about how the components should be wired together. FPGAs combine the best parts of ASICs and processor-based systems, in fact FPGAs are parallel in nature. Advantage of using a software programmed processor is that software is very flexible to change while a disadvantage is that performance can suffer if the clock is not fast. The advantage of an ASIC is that it can provide very high performance because of its dedicated type of operation and its disadvantages are:

- 1) High cost to volume ratio.
- 2) Extended delay between designs to end product.
- 3) Incapability to include new changes after the system is fabricated and
- 4) Difficulties in debugging errors.

FPGAs fill the gap between hardware and software and offer numerous advantages such as:

- 1) Flexibility,
- 2) Reliability,
- 3) Low cost,
- 4) Fast time-to-market and
- 5) Long term maintenance.

After observing this, we conclude that an FPGA is the best reconfigurable hardware platform for the implementation of IoT applications.

II. METHODOLOGY

We are using7th series FPGA, which is Artix7. We areimplementing our proposed model inVivado 18 for simulation and bit file generation. Below diagram describes about internal architecture of Artix 7 FPGA.

Artix7 devices provide the highest performance-per-watt fabric, transceiver line rates, DSP processing, and AMS integration in a cost-optimized FPGA. Featuring the MicroBlaze soft processor and 1,066Mb/s DDR3 support, the family is the best value for a variety of cost and power-sensitive applications including software-defined radio, machine vision cameras, and low-end wireless backhaul.

The general FPGA architecture is shown in Fig. 1 consists of three types of modules. They are I/O blocks, Configurable logic blocks (CLB) and Switch Matrix/Interconnection Wires. The FPGA has two dimensional arrays oflogic blocks which is used to arrange the interconnection between the logicblocks.

FPGAs have gained rapid growth over the past decade because they are useful for a wide range of applications. Some of the applications are cryptography, filtering and communication encoding and many more.

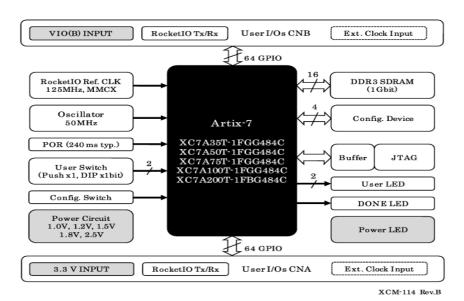


Figure 1: Block diagram of FPGA.



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Vivado Design Suite is a software suite produced by Xilinx for synthesis and analysis of HDL designs, superseding Xilinx ISE with additional features for system on a chip development and high-level synthesis. Vivado represents a ground-up rewrite and re-thinking of the entire design flow (compared to ISE). Like the later versions of ISE, Vivado includes the in-built logic simulator ISIM. Vivado also introduces high-level synthesis, with a toolchain that converts C code into programmable logic.

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| IMPLEMENTATION | ✓ xadc_wiz_0_synth_1 | xadc_wiz_0 | synth_design Complete! | | | | | | | | 0 | 0 | 0.00 | 0 | 0 | 1 |
| Run Implementation | × < | | | | _ | | | | | | | | | | | |

Figure 2: Proposed system implementation in Vivado 18.1

The Vivado Design Suite 2013.1 release includes the IP Integrator (IPI) feature, a new IP-centric design flow for accelerating the time-to-system integration. IPI increases programmable design productivity by 4X, lowering design costs and accelerating development of smarter systems.

| Nizard (3.3) | | |
|---|---|---|
| mentation 🖀 IP Location C Switch to Defaults | | |
| ow disabled ports | Component Name xadc_wiz_0 | |
| - s_axi_ite | Basic ADC Setup Alarms Channel Sequencer Summar | У |
| + s_drp + Vp_M + Vaux0 | Interface Options | Timing Mode |
| | ◯ AXI4Lite ● DRP ◯ None | Continuous Mode Event Mode |
| + Vaux4 vooint_alarm_out + Vaux5 vooaux_alarm_out + Vaux6 vcopint_alarm_out | Startup Channel Selection | DRP Timing Options |
| + Vaux? vecpaux_alarm_out - + Vaux8 vecddro_alarm_out - + Vaux9 et_out - | Simultaneous Selection | Z Enable DCLK |
| + Vaux10 channel_out[4:0] = + Vaux11 muxaddr_out[4:0] = | Independent ADC | DCLK Frequency(MHz) 50 (8.0 - 250.0) |
| + Vaux12 eoo_out - | Single Channel | ADC Conversion Rate(KSPS) 962 (39.0 - 962.0] |
| + Vaux14 alarm_out - + Vaux15 eos_out - | Channel Sequencer | Acquisition Time (CLK) 4 |
| m_axis_aolk buzy_out s_axis_aolk jtaglooked_out m_axis_resetn jtagmodified_out - | AXI4 STREAM Options | Clock divider value = 2 ADC Clock Frequency(MHz) = 25.00 |
| s_axi_aolk jtagbusy_out s_axi_aresetn temp_out[11:0] dok_jin | Enable AXI4Stream | |
| reset_in convist_in convist_ik in | FIFO Depth 7 [7 - 1020] | |
| | | |

Figure 3: IPI of ADC for analog temperature and light sensor





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The **Vivado** IDE allows you to use one or many **constraint files**. While using a single **constraint file** for the entire compilation flow might seem more convenient, it can be a challenge to maintain all the **constraints** as the design becomes more complex.

Finally, we have to generate bitstream file for flash of the FPGA. We can select bitstream option in Vivado.

| Q | Bitstream | | | | | | |
|--|--|--|--|--|--|--|--|
| Project Settings | Specify various settings related to writing bitstream | | | | | | |
| General Simulation Elaboration | ⑦ Note: Additional bitstream settings will be available once you open an implemented design. | | | | | | |
| Synthesis | Write Bitstream (write_bitstream) | | | | | | |
| Implementation | tcl.pre | | | | | | |
| Bitstream | tcl.post | | | | | | |
| > IP | -raw_bitfile | | | | | | |
| T 1 C | -mask_file | | | | | | |
| Tool Settings | -no_binary_bitfile | | | | | | |
| Project IP Defaults | -bin_file | | | | | | |
| Source File | -readback_file | | | | | | |
| Display WebTalk | -logic_location_file | | | | | | |
| | -verbose | | | | | | |
| Help | More Options | | | | | | |
| > Text Editor 3rd Party Simulators > Colors Selection Rules Shortcuts > Strategies > Window Behavior | | | | | | | |
| | Select an option above to see a description of it | | | | | | |
| | | | | | | | |

Figure 4: Bitstream file generation.

Fig. 5 is a proposed model of our complete system. A temperature sensor is a thermocouple or a resistance temperature detector (RTD) that gathers the temperature from a specific source and alters the collected information into understandable type foran apparatus or an observer. Here we are using LM35 as a temperature sensor. Temperature sensors are used in several application namely HV (high voltage) system and AC (alternating current) system environmental controls, medical devices, food processing units, chemical handling, controlling systems, automotive under the hood monitoring andetc.

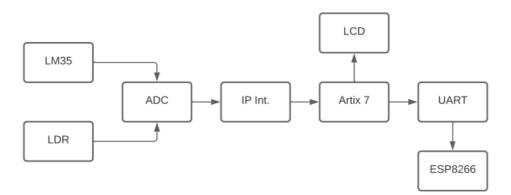


Figure 5: Block diagram of our proposed model.

LDR and resistor connected in series to form a light sensor. It gives the input to ADC using IP Integrator and further connected with FPGA.



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Artix 7 FPGA starter kit consists of on board 8 channels ADC with channel connected with LM35 temperature and LDR sensor. VHDL code is used to perform conversion of analog to digital and read the LM35 output as a digital data and 2*16 LCD is used to display theoutput.

ESP8266 Wi-Fi Module is used to transmit the temperature data wirelessly to the Wi- Fi Modem at the other end with internet connection. ESP826 Wi-Fi Module can be initialized using set of AT Commands. After the initialization process, we have to program for configuring the Wi-Fi module as a TCP/IP client. We are using Thingspeak as a IOT server for logging the data.

III. RESULT AND DISCUSSION

ThingSpeak is an open-source Internet of Things (IoT) application and API to store and retrieve data from things using the HTTP and MQTT protocol over the Internet or via a Local Area Network. ThingSpeak enables the creation of sensor logging applications, location tracking applications, and a social network of things with status updates".

We provide the power supply to our development board and test in differentcases. LM35 and LDR give temperature and light analog values, respectively. IPI of ADC convert it into digital value and further scale into decimal values. UART send values to ESP8266 via serial communication. LCD display same value in development board.

Channel Stats Created: <u>3.months.ago</u> Last entry: <u>2.months.ago</u> Entries: 62

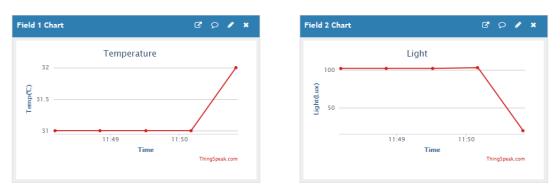


Figure 6: Temperature and Light values are logging into ThingSpeak server.

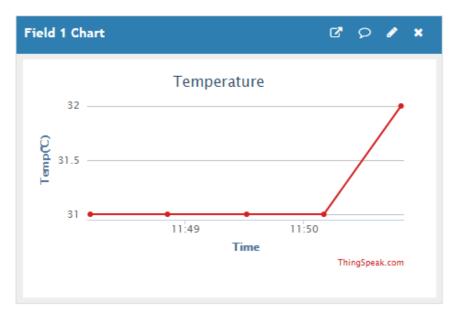


Figure 7: Temperature values in different time intervals.



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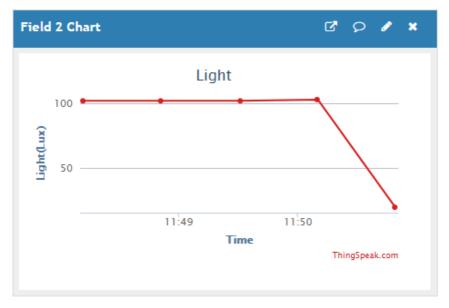


Figure 8: Light values in different time intervals.

IV. CONCLUSION AND FUTURE WORK

The IOT based embedded system has facing many challenges in difficult IOT applications. The Field Programmable Gate array structure is the alternate arrangement to overcome the problem which is facing in ARM processor. In this paper, we have introduced the study of technology paradigm for IOTs on FPGA Platform. The IOT based FPGA includes communication protocols, Data Acquisition and controlling systems. The temperature, Light has been monitored with the combination of IOT and FPGA architecture and for every second time period the temperature, light has been updated in the particular IP address. There are various business spaces it needs you to observe temperature, light and update the status to the cloud. The temperature must be maintained at the lowest level in food preservation process. IOT based temperature monitoring system help us to monitor the food preservation system temperature, light and update the data to the cloud at the regular interval.

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