

# Study of Dielectric Material Properties and its Selection for Hybrid Stackups

Puja S. Patil<sup>1</sup>, Sangam Borkar<sup>2</sup>, Aniket Udekar<sup>3</sup>

P.G. Student, Department of Electronics and Telecommunication Engineering, Goa College of Engineering, Goa, India<sup>1</sup>

Assistant Professor, Department of Electronics and Telecommunication Engineering, Goa College of Engineering, Goa, India<sup>2</sup>

Department of Research and Development, Siemens Limited Verna, Goa, India<sup>3</sup>

**ABSTRACT:** The aim of this paper is to study and analyse PCB stackup materials along with its properties and select an appropriate material for Hybrid PCB stackup configuration. This will help us understand the simulation of Hybrid stackup compared to standard stackups for studying the behaviour for signal integrity and insertion losses. As the frequency increases, signal attenuation becomes the major concern for PCB designers. Insertion loss is the mostly faced in the long channel routing on PCB. There are different approaches to mitigate these attenuation and losses on the printed circuit board. Enablers can be used like re-timers, re-drivers, using low loss dielectric etc. Low loss dielectrics are expensive, but when used along with FR4 it meets the design requirements and cost.

**KEYWORDS:** Dielectric material properties, Hybrid PCB stackup, signal attenuation, insertion loss, low loss dielectric, dielectric constant.

## I. INTRODUCTION

Printed circuit boards are widely used in all the electronic industries today. As the technology is improving and getting better, demand for faster PCB with very little EMI issues are preferred. As at high frequency, devices are fast. A small amount of signal attenuation causes major loss in the system. PCB stackup plays an important role in this. If at the manufacturing and design stage EMI issue is taken care, the PCBs operate as the desired norms. Hybrid PCB stackup consists of low loss dielectric material and high loss dielectric material (ideally FR4). It helps to solve the insertion loss and interference problems at the manufacturing stage. It's mainly useful for high frequency PCBs

## II. PCB STACKUP

PCB stackup is a substrate on which assembly of all circuit design component is done. It is an arrangement made up of copper layers and insulating layers. Initial stage of PCB stackup is important to mitigate the EMI problems along with losses and also minimize circuits vulnerability to the external noise and also the radiation, reduce crosstalk concerns on high speed circuits and reduce impedance.



Fig. 1. PCB stackup

### III. PCB STACKUP MATERIAL SELECTION

A complex PCB board consists of high-end components which require multiple layer count and low loss materials to operate at higher frequencies such as transceivers. The different loss materials decide the transmission rate of signal; therefore, it is important to understand the properties of material properly that will influence the signal losses and PCB manufacturing

### IV. MATERIAL LOSS CONSIDERATIONS

At lower frequencies, impedance mismatch is the reason behind signal loss in PCBs, so the dielectric loss and conductor loss has less effect at lower data rates. But as the data rate goes higher, dielectric material properties becomes an important parameter to consider. Therefore some critical parameters that have to be considered while selecting the dielectric material are as follows:

1. Relative Dielectric Constant
2. Loss Tangent

### V. RELATIVE DIELECTRIC CONSTANT

Relative Dielectric Constant is the ability of the material to get polarised in electric field and store electromagnetic energy, which varies with frequency. Dielectric material is an electric insulator. Application of electric field polarises the material and the molecules get oriented along the direction of electric field as shown in the diagram below. E represents the applied electric field.

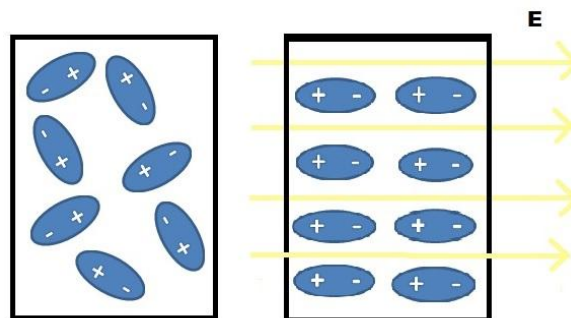


Fig. 1. Molecules in dielectric substrate

This polarisation induces equal and opposite charges on the two opposite faces of the dielectric. Consider two parallel conducting plates carrying surface charge density of  $+\sigma$  and  $-\sigma$ , so the magnitude of electric field will be given by  $E = (\sigma / \epsilon) \hat{a}$

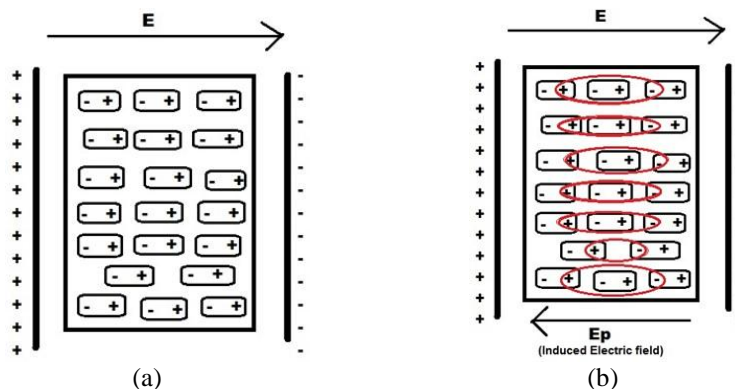


Fig. 2. (a) Electric field applied on dielectric (b) induced electric field on substrate



When dielectric substrate is placed between the two plates, an induced electric field is generated within the substrate. This induced electric field is in opposite direction to the applied electric field.  $E_p$  represents the induced electric field.

$$E_p = (\sigma_p / \epsilon_0) \hat{a}$$

Net electric field is given by;

$$E = E_o + (-E_p)$$

$$E = E_o - E_p$$

$$E = (\sigma / \epsilon_0) \hat{a} - (\sigma_p - \epsilon_0) \hat{a}$$

This electric field is called the reduced electric field. So therefore we can conclude that when we place dielectric substrate between two parallel plate conductors, the electric field reduces. Also we know that,

$$V = E * d$$

Where, E is the electric field

D is the distance between the two plates.

$$C = Q/V$$

Now coming to Dielectric Constant, we know that dielectric constant is the ability to polarise the substrate in electric field with respect to vacuum. For example consider that before placing the dielectric, the applied electric field was 10N/C, but after placing the dielectric the net electric field was decreased to 5N/C. this means that the electric field got reduced by two times after placing the dielectric so the dielectric constant of this material will be 2. It is given by  $D_k$  or  $\epsilon_r$ . Therefore we can see that as the dielectric constant reduces, the induced electric field reduces and so the capacitance also reduces.

Low dielectric constant has various advantages. It acts as a good insulator. Here signal propagates faster through the material. Low loss dielectric means the insertion loss which arises from reflection loss; copper loss etc, all reduces. Crosstalk also has slight improvement over high loss materials. Dielectric is said to depend on frequency. So when the circuits operate at higher frequency, the various digital circuits on the board operate at different frequencies and because of this impedance mismatch is caused which leads to signal loss. The main reason for signal loss is the phase jitter which arises from different harmonics. Therefore selecting a dielectric material with lower dielectric constant helps in flattening the frequency response and helps minimize the signal loss and phase jitter.

### VI. DIELECTRIC LOSS / LOSS TANGENT

Loss tangent or dielectric loss is the measure of how much signal gets lost the transmission process. The greater the loss tangent/dielectric loss means that the dielectric absorption is more and signal reaching its destination is less. Signal attenuation due to loss tangent is given by;

$$\text{Attenuation} = 2.3 * f * \tan(\delta) * \sqrt{\epsilon_r}$$

Where:  $f$ = frequency,  $\tan(\delta)$  is the dimensionless loss tangent,  $\epsilon_r$  is the relative dielectric constant of the material. Dielectric loss is caused due to leakage resistance.

$$P = V^2/R$$

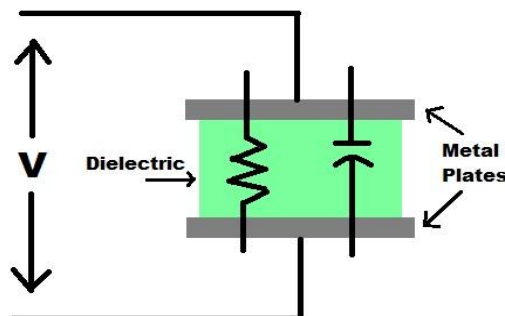


Fig. 3. Voltage applied across dielectric

When dielectric material is placed in alternating electric fields, atoms in the material get stressed and heat is produced. This is the dielectric loss. All dielectric materials are considered as imperfect capacitors and can be represented in the form of resistance and capacitance in parallel. As seen in the circuit diagram above Fig 3, a leakage resistance is created parallel across the capacitance.

The equivalent circuit of this will be as follows:

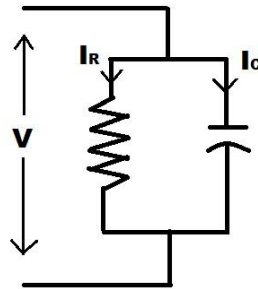


Fig. 4. Equivalent Circuit

This voltage V will produce leakage current due to the leakage resistance. There will be two currents, resistance current IR and capacitance current IC. This resistance current IR is the reason for the generation of the loss. Consider the phaser diagram below as shown in Fig 5.

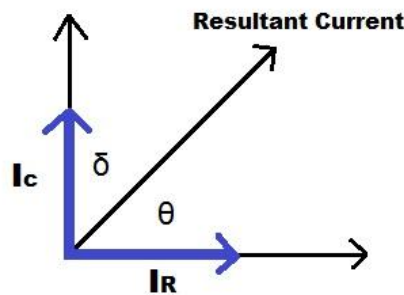


Fig. 5. Phaser Diagram

Here the resistance current IR is real current so it will be in real direction. The capacitance current IC will lead the resistance current by 90°. The resultant current makes an angle theta with resistance current and delta with capacitance current. Where angle theta is the power factor and angle delta is the loss angle. A material's loss tangent gives a measure of power lost due to the material. The lower the material's loss tangent, lower is the power lost.

Coming to phaser diagram, for small value of delta;

$$\delta = \tan \delta$$

$$\delta = \sin \delta$$

$$\delta = \sin (90 - \theta) = \cos \theta$$

Also, from phaser diagram we get;

$$\tan \delta = IR/IC$$

$$IR = V/R$$

$$IC = V/Xc = V/(1/\omega C)$$

Substituting the values of IR and IC in the equation of tan delta we get;

$$\tan \delta = 1/(\omega R C)$$

from here we get value of R as

$$R = 1/(\omega C \tan \delta)$$

the dissipated power is given as;

$$P = V^2/R = V^2 \omega C \tan \delta$$

Furthermore, substituting the values of omega and Capacitance C as



$$\omega = 2 \pi f$$

$$C = \epsilon \epsilon_r A/d$$

Where,  $\epsilon_r$  is the dielectric constant.

So, the equation for dissipated power then becomes;

$$P = V^2 (2 \pi f) (\epsilon \epsilon_r A/d) \tan \delta$$

From the above equation we can see that,

- Dissipated power is directly proportional to the square of voltage
- Dissipated power is directly proportional to loss angle
- The dissipated power is directly proportional to the dielectric constant of the dielectric material

So, we conclude that if loss tangent and dielectric constant increases, the dielectric heating increases.

### VII. HYBRID STACKUP

In hybrid stackup, the dielectric used is low loss in combination with normal high loss material like FR4. As we have studied the advantages of low loss material, let us see its improvement in insertion loss performance. There are different options for creating the hybrid stackup. Few are shown below:

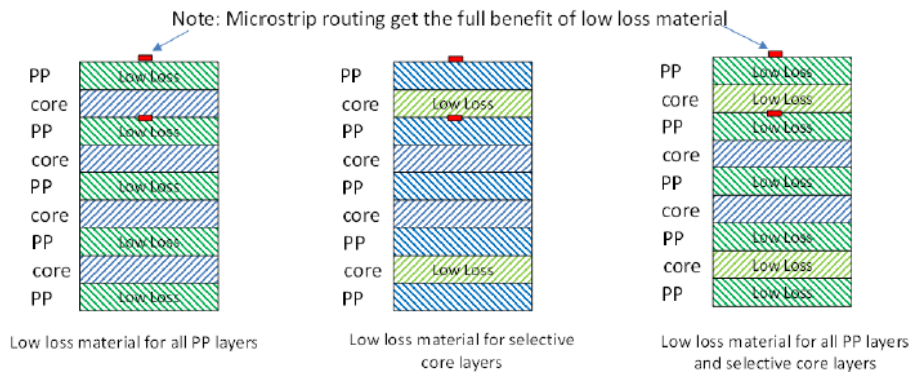


Fig. 6. Hybrid PCB stackup implementation examples

One example of 8 layer hybrid stackup is shown below which can be used to high speed dense boards. Here, Meg6 is the low loss material and Polyclad 370HR is the high loss material. The low loss material is in the inner layers and its thickness is kept lesser than the high loss material. E2 and E3 are the hybrid stripline routing layers.

	Dk (2 GHz)	Thickness (um)	Material Type
E1	3.68	1.70 (43)	FOIL
		2.90 (74)	1080 - Polyclad 370 HR
E2	3.35	1.20 (30)	Lam, Meg 6 .004 2x1035 1/1 HVLP 24x18
E3		4.00 (102)	
	3.90	1.20 (30)	2116 / 2116 / 2116 - Polyclad 370 HR
		13.65 (347)	
E4	4.06	1.20 (30)	Lam, 370HR .010 2x2116 1/1 DSTF 24x18
E5		10.00 (254)	
	3.90	1.20 (30)	2116 / 2116 / 2116 - Polyclad 370 HR
		13.65 (347)	
E6	3.35	1.20 (30)	Lam, Meg 6 .004 2x1035 1/1 HVLP 24x18
E7		4.00 (102)	
	3.68	1.20 (30)	1080 - Polyclad 370 HR
		2.90 (74)	
E8		1.70 (43)	FOIL

Fig. 7. 12 Layer stackup of Test PCB design

Figure 7 gives the insertion loss graph (S parameter) of three boards. One using all FR4 layers, one using all layers as low loss and third one hybrid. The loss improvement can be seen from the graph below;



Fig. 8. Insertion loss

### VIII. CONCLUSION

Hybrid stackup is proposed to meet the high frequency loss requirements. From the modelled PCB, the hybrid stackup shows improved performance compared to traditional FR4. We can conclude that using low loss material is one way to deal with insertion loss challenge and is also one enabler which will improve the signal integrity performance.

### REFERENCES

- [1] C. Ruiz, C. Ye, X. Ye, E. Lopez, M. Yin, J. Hsu, T. Su, Improve Signal Integrity Performance by Using Hybrid PCB Stackup, IEEE EMC Symposium, 2013
- [2] T. Su, J. Hsu, C. Ye, X. Ye, and A. Grigoras, Signaling enabler in high-speed system design by using hybrid stackup printed circuit board, 2013 8th International Microsystems, Packaging, Assembly and Circuits Technology Conference (IMPACT), pp. 8588, 2013
- [3] J. M. Zhang, A.C. Scogna, J. Fan, B. Archambeault, J.L. Drewniak and A. Orlandi, "A hybrid stack-up of printed circuit board for high-speed networking systems", IEEE EMS Symposium, 2012, pp.554-559
- [4] K.B.Wu, et al, A Hybrid Stack-Up of Printed Circuit Board for HighSpeed Networking, EDAPS, 2012