

e-ISSN: 2319-8753 | p-ISSN: 2347-6710

EDIA

International Journal of Innovative Research in SCIENCE | ENGINEERING | TECHNOLOGY

INTERNATIONAL JOURNAL OF INNOVATIVE RESEARCH

IN SCIENCE | ENGINEERING | TECHNOLOGY

Volume 10, Issue 12, December 2021

INTERNATIONAL STANDARD SERIAL NUMBER INDIA

Impact Factor: 7.569

9940 572 462

6381 907 438

 \bigcirc



e-ISSN: 2319-8753, p-ISSN: 2347-6710 www.ijirset.com | Impact Factor: 7.569



|| Volume 10, Issue 12, December 2021 || | DOI:10.15680/LJIRSET.2021.1012121 |

Hardware Analysis of Single Phase Seven Level Multilevel Inverter with Reduced Switches and Sources for Renewable Energy Applications

Abhijeet Anand Aiwale¹, Prof. A. P. Kinge², Dr. S. G. Kanande²

P.G. Student, Department of Electrical Engineering, TSSM's BSCOER, Pune, India¹

Professor, Department of Electrical Engineering, TSSM's BSCOER, Pune, India²

ABSTRACT: Multilevel Inverters are influencing many industries because of their applications in renewable energy with low switching losses, low THD and high dv/dt stress. This dissertation deals with analysis of single phase 7 level multilevel inverter with reduced number of switches and sources and their voltage and current outputs for 'R' loads. The switching angles and the corresponding time required to generate the gating pulses of MOSFET switches of multilevel inverter are calculated by Equal Phase (EP) Method. Since the number of switches and sources are less in case of 7 level multilevel inverter with reduced numbers of switches and sources as compared to conventional cascade multilevel inverter, the cost is less and the circuitry is simple. Hardware model is first simulated in Proteus software for the real time implementation and then hardware implementation of 7 level reduced numbers of switches and sources multilevel inverter is done and the results are shown.

KEYWORDS: Multilevel Inverter (MLI), Equal Phase (EP), Separate DC Sources (SDCS), Total Harmonic Distortion (THD).

I. INTRODUCTION

Multilevel inverters continue to receive more and more attention because of their high voltage operation capability, low switching losses, high efficiency and low Total Harmonic Distortion (THD). The term multilevel starts with the three-level inverter introduced by Nabae et al (1981). Nowadays, multilevel inverters are becoming increasingly popular in power applications, as multilevel inverters have the ability to meet the increasing demand of power rating and power quality associated with reduced harmonic distortion and lower electromagnetic interference.

There are different types of inverter topologies are available in which some are popular. Different types of MLI are Diode Clamped MLI, Flying capacitor type MLI and Cascaded H-Bridge multilevel inverter and that is very popular among all the topologies. In this paper, conventional single phase 21 level Cascaded H-Bridge Multilevel Inverter and single phase 21 level multilevel inverter with reduced switches and sources have been compared. The output voltage results were simulated and presented in this paper[1][2].

Also, Switching angles of both multilevel inverters can be calculated by following methods:-

- Equal Phase (EP) Method.
 - Half Equal Phase (HEP) Method.
 - Half Height (HH) Method.
 - Feed Forward (FF) Method.

The conventional inverters yield an output voltage with levels \pm Vdc, which are termed as a two level inverter. But this output is not a sinusoidal wave. To obtain nearly sinusoidal wave, multi-level inverters are used. Conventional inverters cannot be called as multilevel inverters. If the output of inverter consists of more than 2 levels, then only that type of inverter can be called as multilevel inverter. Three level inverter is the initiation of multilevel concept.

However, the fundamental perception of a multilevel inverter is to attain higher power with the use of sequence of H-Bridges, with numerous low voltage Direct current sources, to accomplish the power transformation, by generating a set of steps or stepped voltage waveform. Input Direct current sources to the multilevel inverter may be either Batteries or Capacitors or any renewable energy voltage sources.

International Journal of Innovative Research in Science, Engineering and Technology (IJIRSET)



| e-ISSN: 2319-8753, p-ISSN: 2347-6710| <u>www.ijirset.com</u> | Impact Factor: 7.569|

Volume 10, Issue 12, December 2021

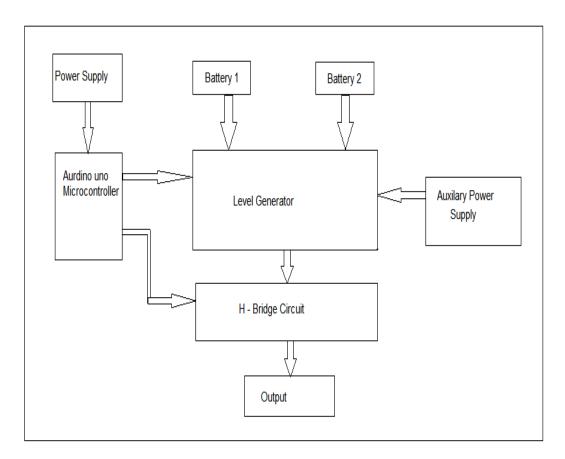
DOI:10.15680/IJIRSET.2021.1012121

As we go on increasing the levels of multilevel inverter, complexity goes on increasing with larger value of voltage drop. Thus for now, as a proof of concept, we are representing the hardware model of seven level multilevel inverter with R load. All the details of hardware model are mentioned in following topics.

In this paper 7 level Multilevel inverter is designed using Proteus software and then hardware model of 7 level multilevel inverter is analysed

II. BLOCK DIAGRAM OF SINGLE PHASE 7 LEVEL MULTILEVEL INVERTER TOPOLOGY WITH REDUCED NUMBER OF SWITCHES AND SOURCES

The block diagram of Single Phase 7 Level Multilevel Inverter Topology with Reduced numbers of switches and Sources consists of power supply for Arduinouno microcontroller. There are two batteries of different ratings used as a DC input power supply to the level generator. Arduinouno is a microcontroller used for the programming of gate triggering of MOSFETs in level generator and H bridge circuit. Level generator is used for the generation of voltage levels in inverter. H-bridge is used for positive and negative generation of levels. Output block is used for measuring the output. Auxiliary power is used for switching of level generator MOSFETs.



International Journal of Innovative Research in Science, Engineering and Technology (IJIRSET)

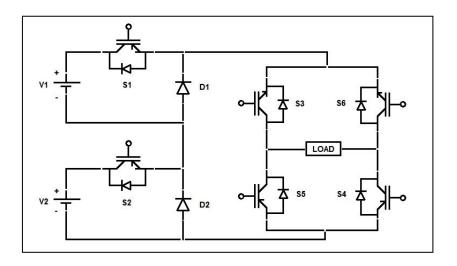
入 う は IJIRSET | e-ISSN: 2319-8753, p-ISSN: 2347-6710| <u>www.ijirset.com</u> | Impact Factor: 7.569|

Volume 10, Issue 12, December 2021

DOI:10.15680/IJIRSET.2021.1012121

III. CONSTRUCTION

Following is the circuit diagram of 7 level multilevel inverter with reduced numbers of switches and sources. It consists of 4 N channel MOSFETs and 2 P channel MOSFETs, two batteries having different voltage ratings and two diodes. MOSFETs S1 and S2 are connected as shown in figure such that it will generate the voltage levels. The four MOSFETs S3, S4, S5 and S6 are connected such that they are forming H bridge which will invert the voltage levels to make the staircase like sine waveform. Arduinouno is the microcontroller which is used to switch the MOSFETs of voltage level generator and H Bridge. The resistive load is connected at the output end of the inverter.



IV. OPERATION

For the positive levels, the operation of MOSFET will be as follows:

Mode 1: In this mode, when switch S1, S2, S3, S4, S5, S6 are turned "off", the output voltage will be '0'. Mode 2: When switches S1, S3, S4 are turned "on", the output voltage across the load will be 'V1'.

Mode 2: when switches S1, S3, S4 are turned on, the output voltage across the load will be vi Mode 2: When witches S2, S2, S4 are turned for a total when the second state of the second s

Mode 3: When switches S2, S3, S4 are turned "on", the output voltage will be 'V2'.

Mode 4: When switches S1, S2, S3, S4 are turned "on", the output voltage will be 'V1+V2'.

For the negative levels, the operation of MOSFET will be as follows:

Mode 1: In this mode, when switch S1, S2, S3, S4, S5, S6 are turned "off", the output voltage will be '0'.

Mode 5: when switches S1, S5, S6 are turned "on", the output voltage across the load will be '-V1'.

Mode 6: When switches S2, S5, S6 are turned "on", the output voltage will be '-V2'.

Mode 7: When switches S1, S2, S5, S6 are turned "on", the output voltage will be '-(V1+V2)'

e-ISSN: 2319-8753, p-ISSN: 2347-6710 www.ijirset.com | Impact Factor: 7.569



Volume 10, Issue 12, December 2021

DOI:10.15680/IJIRSET.2021.1012121

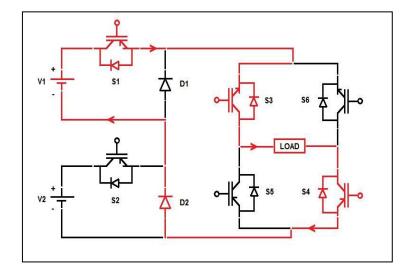


Figure - current flow for positive level of 7 level reduced numbers of switches and sources MLI for voltage output V1.

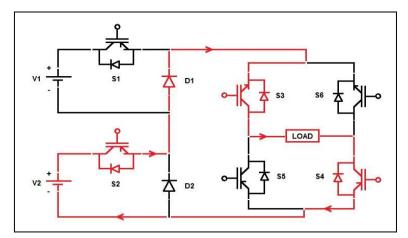


Figure -current flow for positive level of 7 level reduced numbers of switches and sources MLI for voltage output V2

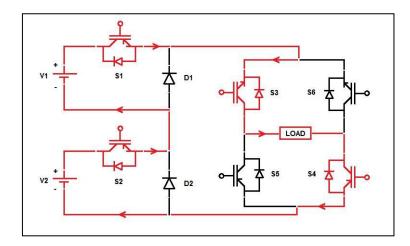


Figure – current flow for positive level of 7 level reduced numbers of switches and sources MLI for voltage output V1+V2

| e-ISSN: 2319-8753, p-ISSN: 2347-6710| <u>www.ijirset.com</u> | Impact Factor: 7.569|

Volume 10, Issue 12, December 2021

DOI:10.15680/IJIRSET.2021.1012121

Table 3.1 Switching Table for reduced number of Switch

Output Voltage	S1	S2	S3	S4	S5	S6
V1+V2	1	1	1	1	0	0
V2	0	1	1	1	0	0
V1	1	0	1	1	0	0
0	0	0	0	0	0	0
-V1	1	0	0	0	1	1
-V2	0	1	0	0	1	1
-(V1+V2)	1	1	0	0	1	1

V. HARDWARE MODEL

List of components

- 1. Arduinouno R3 microcontroller board- 2 No
- 2. IRFZ44N n channel MOSFET- 2 No
- 3. IRF9630 p channel MOSFET- 2 No
- 4. IRF630 n channel MOSFET- 2 No
- 5. 2N2222 Transistor- 4 No
- 6. Resistors- 10 No
- 7. 1N4007 Diodes- 2 No
- 8. LED- 6 No
- 9. Zero PCB- 2 No
- 10. Batteries- 2 No



| e-ISSN: 2319-8753, p-ISSN: 2347-6710| <u>www.ijirset.com</u> | Impact Factor: 7.569|

|| Volume 10, Issue 12, December 2021 ||

DOI:10.15680/IJIRSET.2021.1012121

Sr. No.	Name of Component	Specification of Component		
1	Arduinouno R3			
2	IRFZ44N - n channel MOSFET	VDSS = 55V, ID = 49A		
3	IRF630 - n channel MOSFET	VDSS = 200V, ID = 9A		
4	IRF9630 - p channel MOSFET	VDSS = -200V, ID = -9A		
5	2N2222 Transistor	VEB = 6V, IC 600 mA		
6	BC548 Transistor	VEB = 6V, IC 100 mA		
7	Resistor	0.25W, 10 KΩ		
8	Resistor	0.25W, 220 Ω		
9	Resistor	0.25W, 110 Ω		
10	1N4007 Diodes	IF = 1 A, VF < 1.1 V		
11	LED	IF= 25 mA, VF = 3.5V		
12	Zero PCB	-		
13	Battery 1	6 V		
14	Battery 2	14 V		
15	Auxiliary power supply	9 V		
16	Power supply for Arduinouno	Constant DC 5V supply		

Table 5.1 Specification of hardware Components

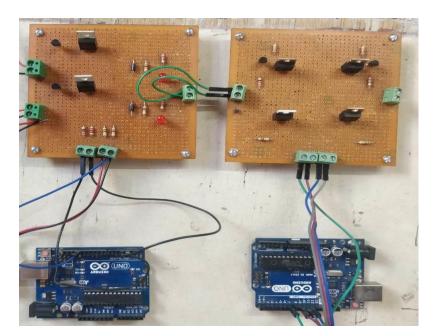
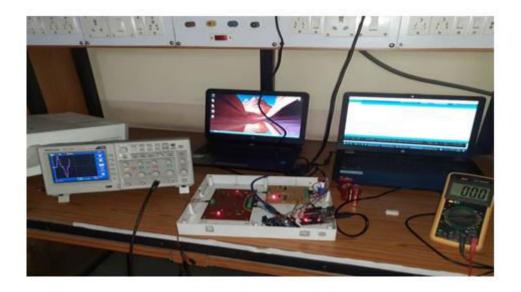
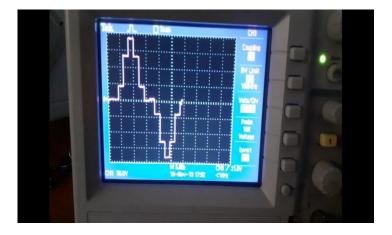


Figure - Actual hardware of 7 level multilevel inverter with reduced numbers of switches and sources

よう iJIRSET | e-ISSN: 2319-8753, p-ISSN: 2347-6710| <u>www.ijirset.com</u> | Impact Factor: 7.569| || Volume 10, Issue 12, December 2021 || | DOI:10.15680/LJIRSET.2021.1012121 |



VI. RESULT



VII. CONCLUSION

The proposed single phase 7 level multilevel inverter with reduced switches and sources offers minimum switching devices and minimum separate DC sources for generating 7 level output voltage. The results of the proposed MLI comes in diminished size, lesser loss, along with low installation cost. Therefore, it is reasonable for medium and high-power applications. The calculation of switching angles was obtained through Equal Phase Method. Future work can be performed having made a 31-level inverter from the same circuit

REFERENCES

- [1] M. bin Arif, S. Ayob, A. Iqbal, S. Williamson and Z. Salam, "Ninelevel asymmetrical single phase multilevel inverter topology with low switching frequency and reduce device counts", 2017 IEEE International Conference on Industrial Technology (ICIT), 2017.
- [2] AditayVardhan Singh, Ravi Shankar Singh, "A Comparative Study of Multilevel Inverter Topologies" IRJET, Volume: 05 Issue: 03 | Mar-2018

International Journal of Innovative Research in Science, Engineering and Technology (IJIRSET)

よう ぶ IJIRSET | e-ISSN: 2319-8753, p-ISSN: 2347-6710| www.ijirset.com | Impact Factor: 7.569

Volume 10, Issue 12, December 2021

DOI:10.15680/IJIRSET.2021.1012121

- [3] V. Devi and S. Srivani, "Modified phase shifted PWM for cascaded H bridge multilevel inverter", 2017 Third International Conference on Advances in Electrical, Electronics, Information, Communication and Bio-Informatics (AEEICB), 2017.
- [4] AhsanNajafi, *Member, IEEE*, and Abdul Halim Mohamed Yatim, *Senior Member, IEEE*, "Design and Implementation of a New Multilevel Inverter Topology ",IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS, VOL. 59, NO. 11, NOVEMBER 2012.
- [5] N. Agrawal and P. Bansal, "A new 21-level asymmetrical multilevel inverter topology with different PWM techniques", 2017 Recent Developments in Control, Automation & Power Engineering (RDCAPE), 2017.
- [6] AparnaPrayag, Sanjay Bodkhe, "A Comparative Study of Symmetrical and Asymmetrical Cascaded H Bridge Multilevel Inverter Topology for Industrial Drive." IRJET, Volume: 05 Issue: 02 | Feb-2018.
- [7] Md. Tariqul Islam, Md. Shahidul Islam and Arnob Kumar Bairagi, "A New Single Phase 21 Level Inverter Topology with Reduced Number of Switches and Sources for Renewable Energy Applications", 4th International conference on Electrical Engineering and information and communication technology.





Impact Factor: 7.569





INTERNATIONAL JOURNAL OF INNOVATIVE RESEARCH

IN SCIENCE | ENGINEERING | TECHNOLOGY





www.ijirset.com