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FPGA Implementation of Complex Floating Point Vedic Multiplier with Minimum Path Delay

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ABSTRACT: Digital media and signal processing applications are usually dominated by integer addition and multiplication. Hence, developing faster, smaller and power efficient Functional Units (FUs) is critical to implement efficient circuits. While partial carry-save adders are easily designed by splitting them into several fragments working in parallel, the design of partial carry-save multipliers is more challenging. Prior approaches have proposed several solutions based on the radix-4 recoding. This technique makes it possible to diminish the height of a multiplier by half, this being the most widespread option when designing multipliers, as only easy multiples are required. In the proposed system, design of low power 8 Bit VEDIC multiplier is being implemented using adjustable path selection routine that enable the Multiplier to save the carry path adjustable and finally combines both the result in the sum part. The proposed algorithm uses reconfigurable nature of VLSI systems. The proposed algorithm is executed in the Spartan-3E FPGA. The proposed structure utilizes low power and that would be compared in terms of power, path delay, efficiency, with array multiplier and existing multiplier.

KEYWORDS: Vedic mathematics, Path delay, Field Programmable Gate Array(FPGA)

I. INTRODUCTION

Very large-scale integration (VLSI) is the process of creating an integrated circuit (IC) by combining millions of MOS transistors onto a single chip. The design hierarchy involves the principle of "Divide and Conquer." It is nothing but dividing the task into smaller tasks until it reaches to its simplest level. This process is most suitable because the last evolution of design has become so simple that its manufacturing becomes easier. Multipliers play an important role in today's digital signal processing and various other applications. In high performance systems such as microprocessor, DSP etc addition and multiplication of two binary numbers is fundamental and most often used arithmetic operations. Statics shows that more than 70% instructions in microprocessor and most of DSP algorithms perform addition and multiplication. So, these operation dominates the execution time. That's why, there is need of high speed multiplier. The demand of high speed processing has been increasing as a result of expanding computer and signal processing applications. Low power consumption is also an important issue in multiplier design. To reduce significant power consumption it is good to reduce the number of operation thereby reducing dynamic power which is a major part of total power consumption So the need of high speed and low power multiplier has increased.

Vedic mathematics is part of four Vedas (books of wisdom). It is part of Sthapatya- Veda (book on civil engineering and architecture), which is an upa-veda (supplement) of Atharva Veda. It covers explanation of several modern mathematical terms including arithmetic, geometry (plane, co-ordinate), trigonometry, quadratic equations, factorization and even calculus. The system is based on 16 Vedic sutras or aphorisms, which are actually word formulae describing natural ways of solving a whole range of mathematical problems. Urdhva – Triyakbhyam is the general formula applicable to all cases of multiplication and also in the division of a large number by another large number. It means vertically and crosswise.

II. RELATED WORK

[1] This paper presents an IEEE 754 format 32 X 32 bit complex floating point multiplier using four floating point real multipliers solution with minimum path delay. Each 32 bit real floating multiplier requires a 24 bit fixed point real multiplier for mantissa multiplication. [2] Synthesis results show that a design with a 10-stage pipeline can achieve a



maximum clock rate of 224 MHz and 140 MHz for 16-bit and 32-bit designs, respectively. Both designs use the lowest amount of hardware in terms of gate equivalents as compared to a complex multiplier built with regular FPGA features.[3] Decimal number system multiplication technique based on such ancient mathematics is reported in this paper. Improvement in speed was achieved through stage reduction by “NikhilamNavatasaramamDasatah (NND)” which was adopted from Vedas, during multiplication. [4] In this paper, a detailed review is made on recent applications of Vedic Mathematics in the domain of VLSI to yield novel design, efficient architecture for Squarer, Multiplier, Arithmetic unit, Cubic and divider circuits along with their crucial performance criteria.[5] The main objective of this research paper is to design architecture for finite impulse response (FIR) filter based on complex Vedic multiplier by rectifying the problems in the existing method and to improve the speed by using the common Boolean logic (CBL).[6] A dual-channel multiplier (DCM) for energy efficient second-order piecewise-polynomial function evaluation for 3-D graphics applications is presented in this paper.

The proposed algorithm uses reconfigurable nature of VLSI systems. The proposed algorithm is executed in the Spartan-3E FPGA. The proposed structure utilizes low power and that would be compared in terms of power, path delay, efficiency. with array multiplier and existing multiplier.

III.METHODOLOGY

This technique makes it possible to diminish the height of a multiplier by half, this being the most widespread option when designing multipliers, as only easy multiples are required. In the proposed system, design of low power 8 Bit VEDIC multiplier is being implemented using adjustable path selection routine that enable the Multiplier to save the carry path adjustable and finally combines both the result in the sum part.

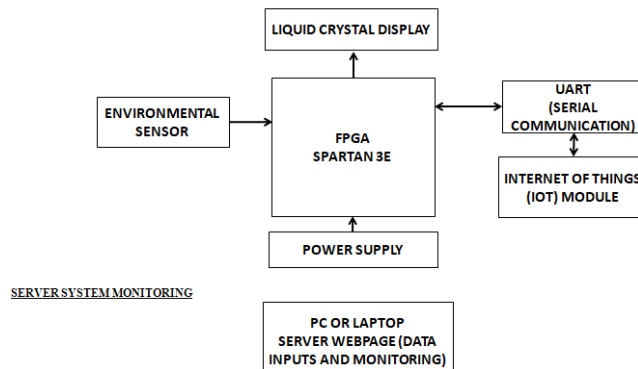


Figure 1: Block diagram for FPGA implementation of vedic multiplier

The description of each block is explained below:

1. Environmental Sensor: The LM35 series are precision integrated-circuit temperature devices with an output voltage linearly-proportional to the Centigrade temperature. The LM35 device does not require any external calibration or trimming to provide typical accuracies of $\pm 1/4^\circ\text{C}$ at room temperature and $\pm 3/4^\circ\text{C}$ over a full -55°C to 150°C temperature range.
2. UART: UART board is used to receive the data from the wireless communication devices and transmit the data in to a serial format. It is provided with a DB9 female port along with a data driver. This board has a filtering unit to reduce the unwanted noise in data transmission.
3. IoT: Node MCU V3 is an open-source firmware and development kit that plays a vital role in designing an IoT product using a few script lines. Multiple GPIO pins on the board allow us to connect the board with other peripherals and are capable of generating PWM, I2C, SPI, and UART serial communications.

FPGA Spartan 3E: The Spartan®-3E family of Field-Programmable Gate Arrays (FPGAs) is specifically designed to meet the needs of high volume, cost-sensitive consumer electronic applications. The Spartan-3E family is a superior alternative to mask



IV. EXPERIMENTAL RESULTS

The heat produced in the FPGA is overcome by using the heat sink component. Supplying the FPGA core voltage at the lower limit of the manufacturer’s specification can save significant static power. Some FPGA vendors use a triple-oxide process technology for some transistors to reduce static power consumption of non-speed-critical configuration circuitry. Another innovation is a shift to a coarser-grained logic architectures employing lookup tables (LUTs) with six inputs rather than the previous standard of four. This enables tighter logic packing, reduces the number of switching transistors, and shortens routing lengths, reducing dynamic power consumption.

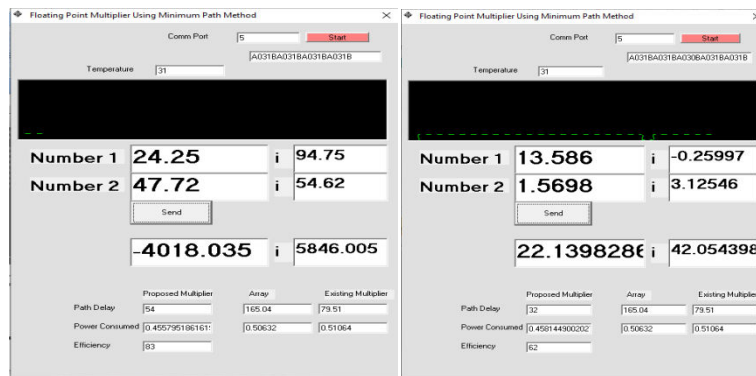


Figure 2: Obtained results

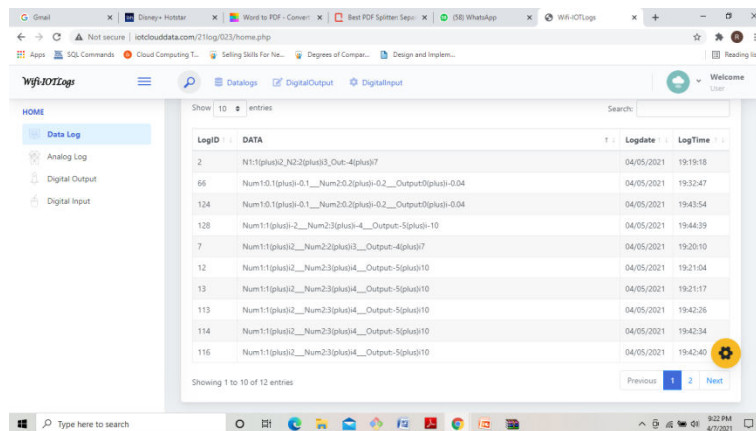


Figure 3: Obtained result of IoT webpage

V. CONCLUSION

This project illustrates the design and implementation of the low power vedic multiplier with minimum path delay which is widely used digital signal processing applications. This project mainly focuses on the multiplier parameters such as efficiency, path delay, power consumption. It is used to determine the cost effective and efficient method which gives higher efficiency. By comparing the results, it is observed that it is more efficient than the existing multiplier. In future this multiplier can be used in many digital signal processing and wireless communication applications. Since IOT hardware is interfaced with the FPGA hardware, the multiplier will be accessible from anywhere.



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