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Design of Power Efficient Voltage Level Shifter Circuit

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ABSTARCT: This paper focuses on reduction of power consumption in voltage level shifter circuit using power gating technique. Voltage level shifter is an interfacing circuit which is used to interface low core voltage with high input-output voltages and vice versa. Voltage level shifters are used to interface various circuit blocks operating at different supply voltages. But one of the major drawbacks of the existing conventional voltage level shifter is the amount of power dissipation is high, mainly due to leakage current. The proposed voltage level shifter circuit converts wide range of low voltage levels to high voltage levels and vice versa with much less power consumption. The architecture is designed with multithreshold voltage CMOS technique. The simulation is carried out using TANNER EDA V13.0 software at schematic level. Simulation results show that the proposed system consumes minimum power when compared to conventional level shifters.

I.INTRODUCTION

VLSI is the process of creating ICs by combining millions of MOS transistors in a single chip. But increase in the number of transistors embedded will increase the power. In early days, power was not a major concern. Speed and area are the major factors. As technology developed, power is also considered as an important factor. The battery operated devices like laptops, mobile phones, tablets etc are increasing, low power consumption has become a major consideration for circuit designing. There are two types of power consumption: static and dynamic power consumption. Dynamic power dissipation is mainly due to the charging and discharging of the load capacitor. The static power dissipation is due to the leakage current when the inputs are not active. Conventional level shifter is a circuit which converts one voltage level to another. But the major drawback of the existing level shifter is it is not that much efficient in battery operated devices and there will be a leakage current leads to wastage of power. Power dissipation is reduced by power gating techniques. In this technique, the shifter will be working in two modes- active and sleep, when shifter is required it will be in active mode and when it is not in use it goes to sleep mode.

EXISTING SYSTEM

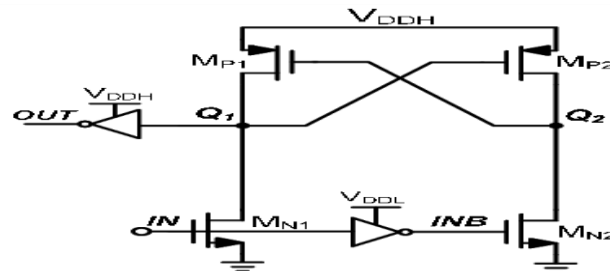


Figure 1: Existing conventional voltage level shifter

The above figure 1 is the circuit diagram of existing conventional voltage level shifter. The conventional shifter consists of two cross coupled PMOS transistors, two NMOS transistors and two voltages VDDH & VDDL.

Here, when the input signal IN is given “High = VDDL”, the transistors MN1 and MN2 are turned ON and OFF respectively. Therefore, MN1 tries to pull down the node Q1, consequently, transistor MP2 is gradually turned ON, which will pull up the node Q2 to VDDH and transistor MP1 is in OFF state. Similarly, when the input signal IN is given “Low = VSS”, the operation is forced to reverse states. In this case, the transistors MN1 and MN2 are turned OFF and ON respectively. Therefore, here MN2 tries to pull the node Q2 down. Consequently, transistor MP1 is gradually turned ON to pull up the node Q1 to VDDH and MP2 is in OFF state. Thus, the input voltage is shifted to the given VDDH voltage using this conventional level shifter. Drawback of this shifter is the amount of leakage current is high which will increase the power consumption. Also, this circuit is not efficient in battery operated devices.

III. PROPOSED STRUCTURE

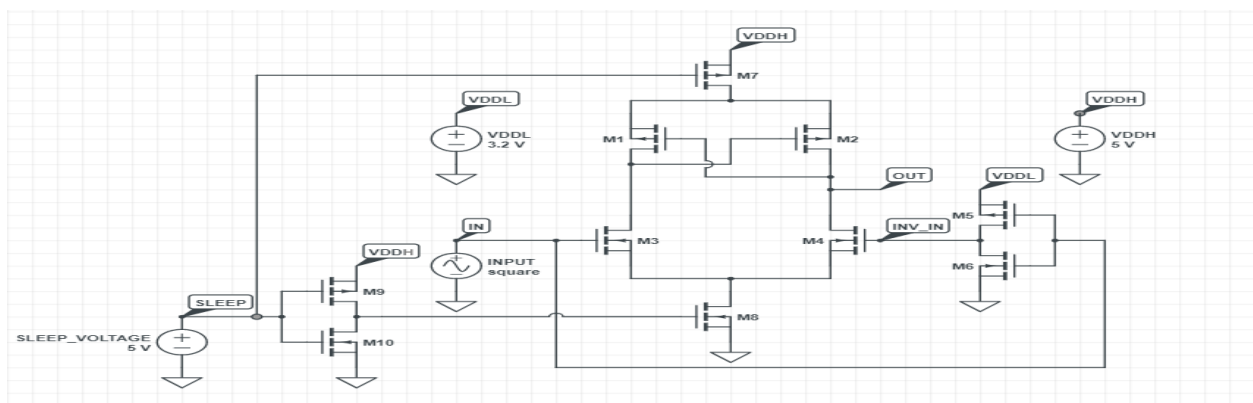


Figure 2. Proposed level shifter circuit

The above figure 2 is a modified level shifter with power gating techniques. To reduce power dissipation we are using two modes. One is active mode and another one is sleep mode. The operation is as follows,

1. ACTIVE MODE:

First, we have to give sleep voltage as 0V so that the circuit goes to active mode. This makes the transistor M9 and M10 to turn on and off respectively. So that the internal core circuit gets connected to VDDH and GND. When input is given as 3.2V, M3 will turn on and M4 will turn off. Since M3 is on this turns on M2 and turn off M1 transistor and this M2

transistor pulls the VDDH supply of 5v from the source to the drain. Output is taken. For an input 3.2V we had obtained output as 5V. The output depends on VDDH. Similarly when input voltage is given as 0V, the operation get reversed.

2. SLEEP MODE:

When sleep voltage is above 5V, this makes transistor M9 and M10 to turn off and on respectively. So that the internal circuit get disconnected from VDDH and GND. Now the internal core circuit is isolated from the high supply voltage VDDH and GND. This prevents the leakage current and leads to less power consumption. Output will be a very low voltage noise signal.

IV.SIMULATION RESULTS

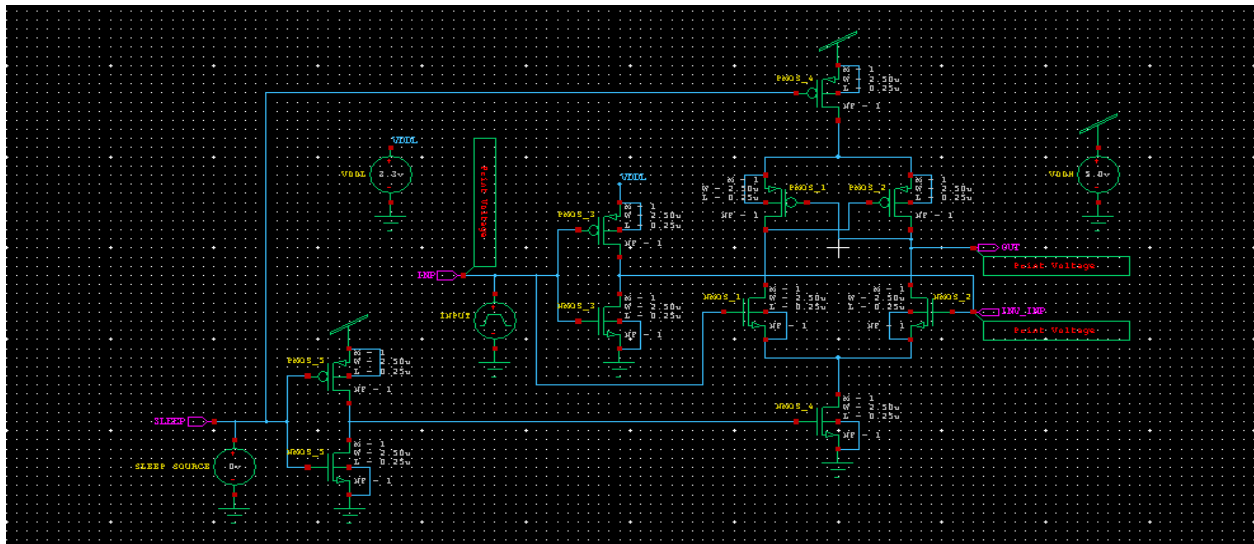


Figure 3. Schematic of proposed level shifter

Figure 3 shows the schematic diagram of our proposed level shifter. The proposed level shifter is simulated using Tanner EDA. And waveform obtained is shown in figures 3a and 3b. Here, the input is given as 3.2V and the output is shifted to 5V. Power consumption, area of the circuits are compared.

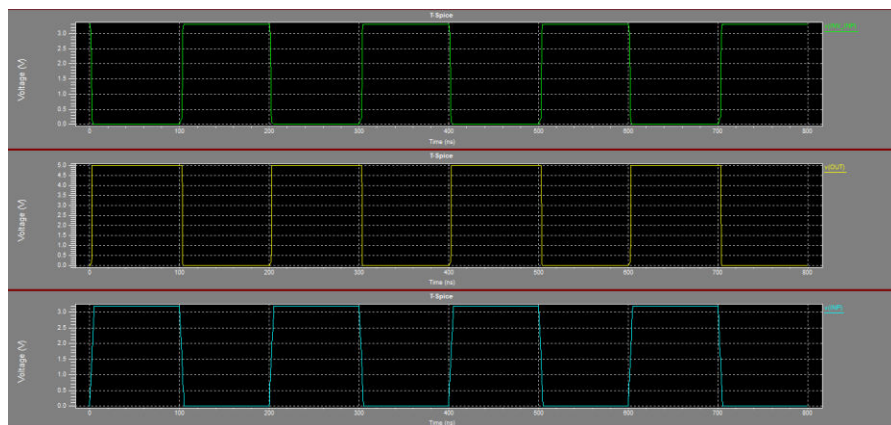


Figure 3a. Simulated waveform for active mode

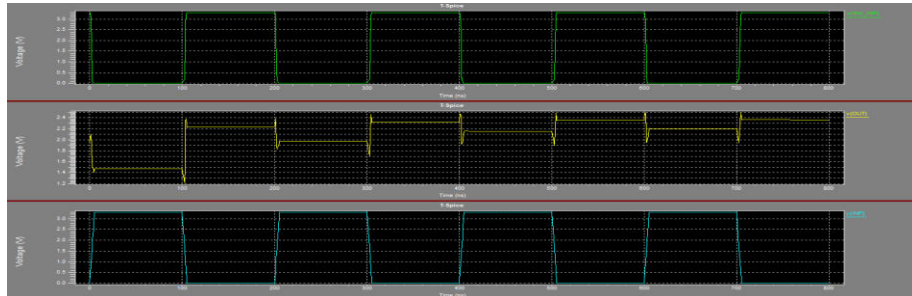


Figure 3b. Simulated waveform for sleep mode

POWER ANALYSIS

Table 1: Comparison of maximum power consumption

MAXIMUM POWER CONSUMED			
VOLTAGE LEVEL SHIFT	CONVENTIONAL LEVEL SHIFTER	PROPOSED LEVEL SHIFTER	
		ACTIVE MODE	SLEEP MODE
3.2V – 5V	9281.1	5384.3	19.265
5V – 12V	27303.5	19725.41	119.23
1.8V – 3.3V	2665.7	1923.4	9.317
12V – 3.3V	6285.2	2532.69	64.09
5V – 3.3V	5818.9	2474.7	18.345
24V – 5V	15099.6	6365.7	140.62

(All units are in micro watts)

Table 2: Comparison of minimum power consumption

MINIMUM POWER CONSUMED			
VOLTAGE LEVEL SHIFT	CONVENTIONAL LEVEL SHIFTER	PROPOSED LEVEL SHIFTER	
		ACTIVE MODE	SLEEP MODE
3.2V – 5V	0.0001	0.0012	0.000062
5V – 12V	0.0556	0.1399	0.000125
1.8V – 3.3V	0.0001	0.0001	0.000002
12V – 3.3V	0.0003	0.0005	0.000181
5V – 3.3V	0.0001	0.0005	0.000003
24V – 5V	0.0013	0.0021	0.000702

(All units are in micro watts)

Table 3: Comparison of average power consumption

AVERAGE POWER CONSUMED			
VOLTAGE LEVEL SHIFT	CONVENTIONAL LEVEL SHIFTER	PROPOSED LEVEL SHIFTER	
		ACTIVE MODE	SLEEP MODE
3.2V – 5V	39.93	29.78	0.024
5V – 12V	200.55	146.75	0.015
1.8V – 3.3V	18.09	16.47	0.006
12V – 3.3V	128.47	68.74	0.015
5V – 3.3V	35.2	15.95	0.004
24V – 5V	489.01	216.74	0.023

(All units are in micro watts)

From Table1, Table2 and Table3 it is concluded that power consumed by proposed level shifter is comparatively less when compared to conventional level shifter in active mode. And it also consumes very less amount of power in sleep mode.

AREA ANALYSIS

CONVENTIONAL SHIFTER

Device and node counts:

MOSFETs - 6	MOSFET geometries - 2
BJTs - 0	JFETs - 0
MESFETs - 0	Diodes - 0
Capacitors - 0	Resistors - 0
Inductors - 0	Mutual inductors - 0
Transmission lines - 0	Coupled transmission lines - 0
Voltage sources - 3	Current sources - 0
VCVS - 0	VCCS - 0
CCVS - 0	CCCS - 0
V-control switch - 0	I-control switch - 0
Macro devices - 0	External C model instances - 0
HDL devices - 0	
Subcircuits - 0	Subcircuit instances - 0
Independent nodes - 3	Boundary nodes - 4
Total nodes - 7	

PROPOSED SHIFTER

Device and node counts:

MOSFETs - 10	MOSFET geometries - 2
BJTs - 0	JFETs - 0
MESFETs - 0	Diodes - 0
Capacitors - 0	Resistors - 0
Inductors - 0	Mutual inductors - 0
Transmission lines - 0	Coupled transmission lines - 0
Voltage sources - 4	Current sources - 0
VCVS - 0	VCCS - 0
CCVS - 0	CCCS - 0
V-control switch - 0	I-control switch - 0
Macro devices - 0	External C model instances - 0
HDL devices - 0	
Subcircuits - 0	Subcircuit instances - 0
Independent nodes - 6	Boundary nodes - 5
Total nodes - 11	

Figure 4.Comparison of circuit elements

Figure 4 shows that area is slightly increased in the proposed level shifter than that of the conventional level shifter as the number of circuit elements is increased. But for any complex circuits, it only requires 1 sleep voltage and 4 extra MOSFETs to implement power gating.

V.CONCLUSION

The proposed voltage level shifter circuit consumes very less power when compared to conventional voltage level shifters. Since proposed voltage level shifter is an enhanced version of conventional voltage level shifter, replacement of conventional level shifter with the proposed level shifter is much easy and compatible. Considering the amount of power consumption, this circuit is more efficient. But the operation speed of this circuit is slightly reduced and hence this circuit is not suitable for devices having high switching frequencies. Thus, further enhancement of this circuit helps to overcome this problem.



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