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Design of 10-Bit Low Power Analog to Digital Converter Using Various Power Reduction Techniques

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ABSTRACT: This paper deals with the implementation of a low-power 10-bit successive approximation resistor ADC in the Cadence Virtuoso tool in 0.18-um technology. The advantage here is that using the successive approximation technique gives zero latency when compared to other ADC architectures. Further low power design techniques like Variable threshold CMOS logic and Dual split switching design techniques are used in building the sub-blocks of the successive approximation resistor. Synthesis results reveal that the proposed ADC achieved power savings of 82% compared to a precise generic architecture-based ADC. Measured results show that a sampling rate of 1 MS/s achieves power dissipation of 28.27uW, and a number of bits 10-bits, a differential nonlinearity of +0.9/-0.82 LSB, an integral nonlinearity (INL) of 0.94 LSB at 500mV power supply.

KEYWORDS: Analog to Digital Converter, Differential Non-Linearity, Integral Non-Linearity, Most Significant Bit, Least Significant Bit

I. INTRODUCTION

As the scale of integration keeps growing, loads refined signal processing systems are being implemented on a VLSI chip. Those signal process applications not solely demand great computation capability, they consume a sizable quantity of energy. While performance and space stay to be the two major design tools, power consumption has become a crucial concern in today's VLSI (Very giant Scale Integration) system design. The requirement for a low-power VLSI system arises from 2 main forces. First, with the steady growth of operating frequency and process capability per chip, large currents are to be delivered, and also the heat because of giant power consumption should be removed by correct cooling techniques. Second, the battery life in moveable electronic devices is limited. Low power style directly ends up in prolonged operation time in these moveable devices.

Analog to Digital Converters are the most useful blocks which are used in quite a lot of applications. In the current growing technology spectrum, Low power design techniques have predominantly come into play. Power consumption is one of the most critical factors in the design of electronic systems, such as wireless systems or implantable devices, power consumption is becoming one of the most critical factors. Thus, these reduced power consumption requirements lead to the development of low power circuit design techniques.

Analog-to-Digital Converters (ADCs) translate the analog quantities into digital language, used in information processing, computing, data transmission, and control systems [27]. ADCs are key components for the design of power-limited systems, in order to keep the power consumption as low as possible. Implantable Medical electronics, such as Pacemakers and cardiac defibrillators are typical examples of devices where ultra-low-power consumption is paramount. The implanted units rely on a small non-rechargeable battery to sustain a lifespan of up to 10 years. The lifetime of the artificial pacemakers should last up to 10 years which mandates low power consumption per

operation. The analog to digital convertor is that the crucial is an implantable pacemaker since it consumes an outsized quantity of power because the interface between a perceived analog signal and digital signal processor block. Therefore, decreasing the power consumption of the ADC is a major concern.



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Low power ADCs with moderate resolution and low sampling frequency are suited for biomedical applications. These specifications make SAR ADC the suitable choice. It consumes low power due to its simple structure. Moreover, SAR ADC is scalable with the technology scaling since most parts of the architecture apart from the comparator are digital. There are many parameters used to characterize an ADC namely resolution, speed, DNL (Differential non-linearity), INL (Integral non-linearity), signal to noise and distortion ratio (SNDR), total harmonic distortion (THD), etc. There are many types of ADCs used in the industry right now and some of them are Flash, Pipelined, SAR ADC, Sigma Delta Converters, and time-interleaved ADC. They can be differentiated based on their design style, sampling rate. For instance, all the above-mentioned Nyquist ADCs accept the sigma-delta and time-interleaved are over and under sampling ADCs respectively. Each of these is used based on the specifications and requirements for that job. Say for instance Flash gives top speed when compared to others but cannot attain high resolutions. In a conventional SAR ADC, the number of clock cycles required to make one complete conversion process is equal to the number of bits of the A/D converter.

Also, in a conventional SAR converter, the fundamental bottleneck for high-precision comes from the matching requirements in a Capacitive Digital to Analog Converter. Typically, in a high precision SAR ADC, the mismatch in the capacitors that occur during fabrication is trimmed at the final test using an in-package trimming mechanism. This is a time-intensive process and increases test costs enormously.



Figure 1 Successive Approximation ADC

Analog-to-Digital (A/D) change and Digital-to-Analog (D/A) transformation lie at the core of most present-day signal preparing frameworks. As digital signal processing (DSP) circuits design becomes progressively complex and accomplishes higher operating speeds additional handling capacities are acted in the digital domain. In most electronic systems, the input and output signals are analog in nature. Nonetheless, the vast majority of the changes are to be completed on the input signals prior on prior to obtaining the outputs which are carried in the digital domain. In this manner, there is a need to change analog input signals to digital input and back again to analog after processing. The circuits that convert simple signs to computerized signals are known as A/D Converters and the circuits that convert divanced signs to simple signs are known as D/A Converters. Charge scaling DACs work by binary division of the total charge which is applied to a capacitor array.

A conventional N-bit SAR A/D converter takes N clock cycles for one full complete conversion process. This A/D converter consists of a sample-and-hold (S/H) circuit, a comparator, a digital-to-analog converter (DAC), and digital logic.

The ADC employs a binary-search algorithm that uses the digital logic circuitry to see the value of every bit in a very sequential or successive manner supporting the result of a comparison between the outputs of the S/H circuit and DAC. Figure 1 illustrates a basic block diagram of a standard binary search SAR A/D. The digital logic then sets the Most-Significant Bit (MSB) to '1'.

With the remaining bits set to '0', the digital word is then applied to the DAC to give an analog output voltage that, once settled within 0.5 LSB of accuracy, is compared with the sampled voltage by the comparator. The analog equivalent of the digital word produced from DAC will be up to the mid-scale of the reference voltage, $\Box \Box \Box \Box$. Each conversion takes 'N' clock cycles to complete.

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II. PROPOSED BLOCK DIAGRAM



Figure 2 Block Diagram and Representation of Individual Blocks

This section describes different blocks of SAR ADC architecture. The main blocks of SAR ADC are a Sample and Hold, a Digital to Analog Converter (DAC), a Comparator, and a SAR Logic

III. BUILDING BLOCKS

A. SAR Control Logic



Figure 3: Proposed Gate level circuit of D Flip-Flop in SAR control logic

The advantage of Successive approximation resistor is to give zero-latency compared to other ADC architectures. The circuit schematic of SAR Control logic is considered from [26] but the basic cell which was used in SAR control is DFF, it is designed with a low on-resistance transmission gate with VTCMOS technique.



Figure 4: Cadence Schematic of Gate level circuit of D Flip-Flop in SAR logic

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B. Sample and Hold Circuit

The Sample & Hold uses a capacitor and an analog switch to connect or isolate the capacitor from the input. The most basic form of the sample and hold circuit combines a switch and a capacitor, the operation of the circuit as follows. In sampling mode, the switch is "on", creating the signal path that allows the capacitor to track an input voltage. When the switch is "off" an open circuit is created that isolates the capacitor from the input, hence changing the circuit from sampling mode into holding mode.



Figure 4: Cadence Schematic diagram of Sample and Hold Circuit

C. Comparator



Figure 5: Cadence Schematic diagram of Regenerative Comparator

The comparator is an important part of the SAR ADC. This Block consumes the most amount of power in the ADC. In an ideal comparator, with infinite gain, for input voltages higher than the reference voltage, the comparator outputs a logical one, and for the input voltages lower than the reference voltage it produces zero at the output.

D. Charge Scaling ADC

A 10-bit charge scaling capacitive DAC is designed with a combination of two 5-bit charge scaling sub-DACs with a scaling capacitor as shown in Figure.5. The series combination of scaling capacitors begins with an LSB array and eliminates the MSB array. The precision of the DAC depends upon the scaling capacitor as it is the eliminating capacitor between LSB and MSB array [27]. The area of the DAC is proportional to the size of the unit capacitor. From the simulation test results, the unit capacitance value is 59.4fF [27]. The folded cascade operational amplifier which was studied in the previous portion is utilized in the DAC as a buffer to increase the linearity and to decrease comparator offset error. Figure.4 shows the sampling circuit designed with a simple transmission gate with Variable Threshold CMOS (VTCMOS). Using the VTCMOS technique the transmission gate is operated in variable threshold voltage, total capacitance on the right of the scaling capacitor 2nF and left of the scaling capacitor 2.62nF.

DAC plays almost 40% in the total power dissipation of ADC because dynamic power dissipation and during the switching event capacitances charge up phase consumes more heat in the circuit.



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Dual split switching minimizes the switching energy by decreasing the on-resistance of the transmission gate that could be described in later portions. The high performance of the DAC is described from the calculations of differential nonlinearity (DNL) and integral nonlinearity (INL). In this paper, ADC design is transferred out for low-frequency applications such as Physiological signals. Although, all the performance grades are transferred out for well-organized ADC as shown in Figure.8 DNL is the difference between an actual step width and the ideal value of 1 LSB

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Figure 6: Cadence schematic of 10-Bit Charge Scaling DAC

E. Switch

The transmission gate is nothing but a bilateral switch consisting of NMOS and PMOS transistors controlled by outwardly applied logic levels. MOS technology uses each NMOS and PMOS device to perform the logic functions, thus permitting a computing machine or logic circuit to regulate the operation of those analog switches.



Figure 7: Cadence schematic diagram of Switch

IV. LOW POWER DESIGN TECHNIQUES

F. VTCMOS

Here MOS transistor substrate bias voltage is dynamically varied to control the threshold voltage. The circuit operates with low-power dissipation (due to low V_DD) and a high switching speed (due to a low V_TH). When the circuit is in the standby mode, the substrate bias control circuit generates a lower substrate bias voltage[27] for the nMOS transistor and a higher substrate bias voltage for the pMOS transistor. As a result, the magnitudes of the threshold voltages (V_THn and V_THp) increase in the standby mode due to the body effect. Since the sub-threshold leakage current drops exponentially with an increasing threshold voltage, the leakage power dissipation in the standby mode can be significantly reduced with this circuit design technique[27]. Anyhow, with the technology scaling, the channel length becomes smaller, or the VTH values are decreased.

G. Dual Split Switching

Dual Split switching is done with a 2:1 MUX design. In charge scaling DAC, 2:1 Mux is used to switch between V_{in} to V_{ref} and in Preamplifier regenerative comparator design also dual split switching is used to switch between amplifier and comparator. The primary element used in the dual splitting design is a transmission gate. Two

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NMOS and PMOS transistors are in shunt connection so that the on-resistance and sampling distortion are maintained as low as possible. The length and widths are in a 2:1 ratio.



Figure 8: Mux with dual transmission gates with on-resistance reducing method

V. SYNTHESIS AND RESULTS



Figure 9: Cadence schematic of Successive Approximation Register ADC

The 10- bit SAR-ADC once completed outputs data at every clock period after an initial latency of ten clock periods. Digital output bits produced by the ADC under test are to perform a weighted sum on the output bits. If Vin, *Vout*, *Vref* are the input-output and reference voltages of the ADC respectively, then *Vout* can be calculated as follows. As this design has both positive and negative references, the range is calculated as shown in the equation below.

The equation shows the method to calculate the weighted sum from the digital output bits from the ADC.

$Vout = Vref - + [MSB^* (Vrange/2) + (MSB-1)^* (Vrange/4) + ... + LSB^* Vrange/2^N]$

The figure 10 shows the DC current of Successive Approximation Register ADC. The value of Bias current is 100nA.

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Architecture	SAR
VDD[V]	0.5v
Power Dissipation[uW]	28.27uW
Technology[nm]	180nm
Resolution[Bits]	10
F _{sample}	Up to 1Msps
DNL[max]	+0.9/-0.82 LSB
INL	0.94 LSB

Table 1: Specifications of SAR ADC



Figure 10: The Digital Outputs of the 10-Bit SAR ADC

VI. CONCLUSIONS

A 10-bit SAR ADC with a 100mV Vref input range using a dual split switching network in DAC is presented. A regenerative comparator operating in the sub-threshold region with low offset was used, along with low power SAR logic with negative edge-triggered flip-flop at a 500mV supply voltage. The measurement results verify the power consumption of the ADC is 28.27uW.

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