



e-ISSN: 2319-8753 | p-ISSN: 2347-6710

IJIRSET

International Journal of Innovative Research in
SCIENCE | ENGINEERING | TECHNOLOGY



INTERNATIONAL JOURNAL OF INNOVATIVE RESEARCH

IN SCIENCE | ENGINEERING | TECHNOLOGY

Volume 11, Issue 4, April 2022

ISSN INTERNATIONAL
STANDARD
SERIAL
NUMBER
INDIA

Impact Factor: 8.118

Design and Implementation of High Performance Carry Select Adder

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ABSTRACT: This high-performance square-root carry select adder (SQRT CSLA) architectures with high speed, area and energy efficiency when compared to the existing SQRT CSLA architectures. The first method (ARCA) uses an optimized design of binary to excess-1 converter (BEC)- based SQRT CSLA by incorporating a carry enable binary to excess-1 converter (CEBEC) design that exploits a new logic optimization on the carry propagation path to improve speed of operation, area and energy efficiency. The second proposed method (CEBEC) is an optimized design of the regular SQRT CSLA by employing the carry enable and add-one ripple carry adder (ARCA) architectures to decrease the number of gates. Simulation results show that the proposed CEBEC SQRT CSLA offers a savings of 22.81%, 9.95%, 7.95% and 3.98% on area, 14.50%, 5.21%, 3.72% and 3.11% in power consumption and offers 6.78%, 15.46%, 6.57% and 3.83% lesser delay, 20.33%, 19.92%, 10.09% and 6.89% lesser PDP, 28%, 23.85%, 13.78% and 7.58% lesser ADP than the existing regular, BEC SQRT CSLA, SQRT CSLAI and SQRT CSLA2 architectures. The proposed ARCA SQRT CSLA architecture exhibits 9.26%, 17.71%, 9.06% and 6.39% lesser delay than the existing regular, BEC SQRT CSLA, SQRT CSLA and SQRT CSLA2.

KEYWORDS: Area , Efficient , High speed, Low power, SQRT CSLA ,VLSI

I. INTRODUCTION

In recent years, the increasing demand for high-speed arithmetic units in microprocessors, image processing units and DSP chips has paved the path for development of high-speed adders as addition is an indispensable operation in almost every arithmetic unit; also it acts as the basic building block for synthesis of all other arithmetic computations. To increase portability of systems and battery life, area and power are the critical factors of concern. Even in Servers and Personal Computers (PC), power dissipation is an important design parameter. In today's scenario, design of area-efficient and power-efficient high-speed logic systems is the one of the crucial areas of research in VLSI design. In digital adders, the speed of addition is limited by the time required by the carry to propagate through it. Depending on the area, delay and power consumption requirements, several adder implementations have been proposed. Ripple Carry Adders with the most compact design among all types of adders are slowest in speed.

Carry Select Adder (CSLA) is one of the fastest adders used in many data processing processors to perform fast arithmetic functions. By gate level modification of CSLA architecture, we can reduce area and power. The basic motive of this work is to design and develop an efficient less area and low power adder. From the structure of the CSLA, it is clear that there is scope for reducing the area and power consumption in the CSLA. This work uses simple and efficient gate-level modification to significantly reduce the area and power of the CSLA. The proposed design reduces area and power as compared with the regular SQRT CSLA with only a slight increase in the delay.

Adders are considered as the basic elements of the digital system, most of the arithmetic operations are based on adders. Adders are commonly used in various electronic applications like Central Processing Unit (CPU) and many other computation circuits and blocks to perform numerous algorithms such as FIR, IIR etc. These devices show that there is a huge necessity in designing and creating new enhanced digital circuits so that the circuit is compact, requires low energy, and operate at a faster rate. Enhancing adders can provide huge advancement in system. A large variety of adder architectures are accessible in the findings so far. CSLA is a high speed adder because of its small size and minimized power consumption. (RCAs) is considered the most basic and the simplest binary adder.

Design of area- and power-efficient high-speed data path logic systems are one of the most substantial areas of research in VLSI system design. In digital adders, the speed of addition is limited by the time required to propagate a carry through the adder. The sum for each bit position in an elementary adder is generated sequentially only after the previous bit position has been summed and a carry propagated into the next position. The CSLA is used in many

computational systems to alleviate the problem of carry propagation delay by independently generating multiple carries and then select a carry to generate the sum. However, the CSLA is not area efficient because it uses multiple pairs of Ripple Carry Adders (RCA) to generate partial sum and carry by considering carry input C_{in} and C_{out} then the final sum and carry are selected by the multiplexers (mux).

The performance of a full adder circuit depends to a great extent on the type of design style used for implementation as well as the logic function realized using the design style. For instance, a standard CMOS implementation allows circuits to achieve a reasonable power delay product with high noise margins, regular layout and relatively higher tolerance to process variations. Dynamic implementations on the other hand may yield an extremely fast design but end up paying higher costs in the overall power consumption. Data driven dynamic logic (D3L) and Split pre-charge data driven dynamic logic (sp-D3L) are two design styles which allow high performance dynamic circuit design without the additional power consumption in the clock distribution network. Thus these styles form interesting implementation strategies for realizing high performance, power-efficient full adders. Power consumption is one of the critical design factors in modern VLSI design.

The dependency of the speed of addition of these adders with the time needed to transport a carry all along this adder. Carry look-ahead adders are employed mostly in time-critical applications, at the cost of more area when large combinational logic is required. Carry select adder shows a better tradeoff among the size requirement and speed characteristics. The primary function of a PPA is that it provides high-speed performance when compared with RCA. PPAs generally belong to the carry look-ahead adder family as they are derived from those adders. In carry select adder, delay due to carry propagation is avoided by parallelly generating various carries simultaneously and then choosing the apt carry value to create the corresponding output. However, it is found that CSLA is not compact as it utilizes more than one pairs of basic adders to output the intermediate carry as well summation on taking into consideration the input carry value $C_{in}=0$ and $C_{in}=1$. CSLA implemented with PPA like Kogge Stone shows better performance in terms of delay.

Therefore rather than realizing pure CSLAs, hybrid CSLA architecture incorporating several adder logic within can improve the design efficiency of CSLAs. Here a peculiar type of hybrid design architecture is presented. In this design RCA stages in regular carry select adder is substituted with speedy adders such as Kogge Stone adder and CLA adder. Carry look ahead adders are employed in the least significant bit position and Kogge Stone in the other remaining position of the hybrid adder. The new proposed adder provides high speed performance. Area and power reduction in data path logic systems are the main area of research in VLSI system design. High speed addition and multiplication has always been a fundamental requirement of high-performance processors and systems. In digital adders, the speed of addition is limited by the time required to propagate a carry through the adder. The sum for each bit position in an elementary adder is generated sequentially only after the previous bit position has been summed and a carry propagated into the next position. The major speed limitation in any adder is in the production of carries and many authors have considered the addition problem. The CSLA is used in many computational systems to moderate the problem of carry propagation delay by independently generating multiple carries and then select a carry to generate the sum. However, the CSLA is not area efficient because it uses multiple pairs of Ripple Carry Adders (RCA) to generate partial sum and carry by considering carry input and then the final sum and carry are selected by the multiplexers (mux).

II. LITERATURE SURVEY

[1] In this review research work we have analyzed the various adders in order to improve the system performance of Carry Select Adder. A multiplier is one of the key hardware blocks in most digital and high performance systems such as FIR filters, digital signal processors and microprocessors etc. With advances in technology, many researchers have tried and are trying to design multipliers which offer either of the following- high speed, low power consumption, regularity of layout and hence less area or even combination of them in multiplier. However area and speed are two conflicting constraints. So improving speed results always in larger areas. In this review research work we have tried to analysis different adders and compare their speed and complexity of circuit i.e. the area occupied. The Ripple Carry Adder had a smaller area while having lesser speed, in contrast to which Carry Select Adders are high speed but posses a larger area. And a Carry Look Ahead Adder is in between the spectrum having a proper trade off between time and area complexities.

[2] This paper investigated on the add-on circuits of CSLA. The CSLA has two ripple carry adders (RCA). One with carry-in=0 and another with carry-in=1. In this paper the ripple carry adder (RCA) with carry-in=0 was not disturbed. The ripple carry adder (RCA) with carry-in=1 was replaced by binary to excess-1 converter (BEC). Since the

difference between sums of two ripple carry adders in conventional CSLA is 'one'. The binary to excess-1 converter (BEC) is a special type of logic whose inputs are in binary format and gives the output which is same as by adding one to the input binary number. The binary to excess-1 converter (BEC) takes the inputs which are the outputs of ripple carry adder (RCA) with carry-in=0. For N-bit ripple carry adder (RCA) requires (N+1)bit binary to excess-1 converter. The outputs of binary to excess-1 converter were given to multiplexer. Multiplexer has carry-in as selection line and gives final sum and carry. When compared to conventional CSLA the area was decreased with this implementation but delay was increased.

[3] In this paper the redundant cells used in conventional carry select adder (CSLA) was eliminated. They proposed a new logic for implementing the carry select adder (CSLA). By analyzing the truth table of full adder, they find out a new logic. For carry-in=0, the output sum of full adder follows the XOR logic and output carry following the AND gate logic. For carry-in=1, the output sum following XNOR logic which is inversion to the XOR i.e., output sum with carry-in=0. Output carry following the OR gate logic in case of carryin=1. These XOR output and its inversion given as two inputs for a multiplexer whose selection line is carry-in. The output of multiplexer gives final output sum. The AND gate and OR gate outputs given to another multiplexer with same selection line i.e., carry-in. The output of multiplexer is given as carry-in for another block. By using this connection, the gate count almost reduced to half when compared to conventional CSLA. We can save 70% power compared with CSLA and 2% increase in power compared with ripple carry adder. The speed is little slower than CSLA because of a shortage of parallel path in the design.

[4] This paper proposed a new logic for designing carry select adder(CSLA). The proposed logic contain four blocks, half sum generation (HSG), full sum generation (FSG), carry generation (CG), carry selection (CS). Carry generation consists two carry blocks CG0 and CG1 corresponding to the carry-input 0 and 1. The HSG block takes the binary inputs and gives the outputs as half-sum and half-carry. The CG block generates the two full carry words for corresponding to the carry input 0 and 1. The CG block equations are same as full adder carry equations. In general, CS block consists of a multiplexer with carry-input as selection line. However, the carry words follows a specific bit pattern. So, the optimization of CS unit has been done. CS unit has ANDOR gates which decides the output carry words depends on the carry-input. After selecting the final carry words, the FSG unit generates the output sum by using carry words and half- sum. This design technique has less area and delay than BEC based CSLA. The area delay-product (ADP) was 35% less than the BEC based CSLA.

III. PROPOSED SYSTEM

The main goal of this proposed system to identify redundant logic functions and data dependencies for the possible input variables and remove the redundant logic functions on the carry propagation path of the existing BEC-based and regular SQR CSLA to achieve higher speed, area and energy efficiency.

Proposed 16-bit CEBEC SQR CSLA Design:

The layout of existing of the 16-bit regular or BEC SQR CSLA architecture has five groups. In the group 4 of the existing BEC-based SQR CSLA a 4-bit RCA, 5-bit BEC and 2:1 multiplexer enable the carry selection on the carry propagation path.

Blocks	Delay	Area
2-bit RCA _0	6	19
2-bit RCA _1	8	26
3-bit RCA _1	10	39
4-bit RCA _1	12	52
5-bit RCA _1	14	65

Table : Delay and area of the basic blocks of existing SQR CSLA

Similar to the existing 16-bit regular or BEC SQR CSLA, the proposed layout has five groups. Indicates the design of existing BEC-based SQR CSLA with a 4-bit RCA, 5bit BEC and 2:1 multiplexer modules pertaining to group 4. The sum and carry outputs of 4-bit RCA with Cin = 0 are given as input to 5-bit BEC, which in turn will add a binary one to the present input and give the output which is equivalent to the 4-bit RCA output when Cin = 1.

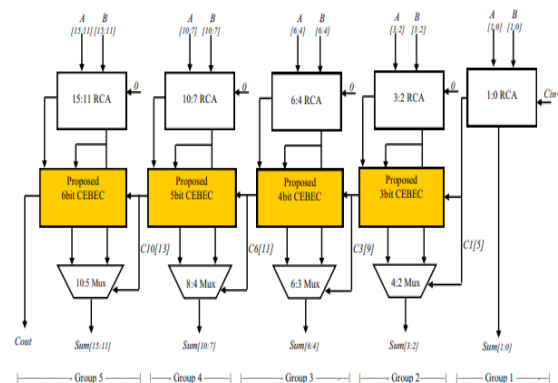


Fig : Architecture of the proposed 16-bit CEBEC Sqrt CSLA

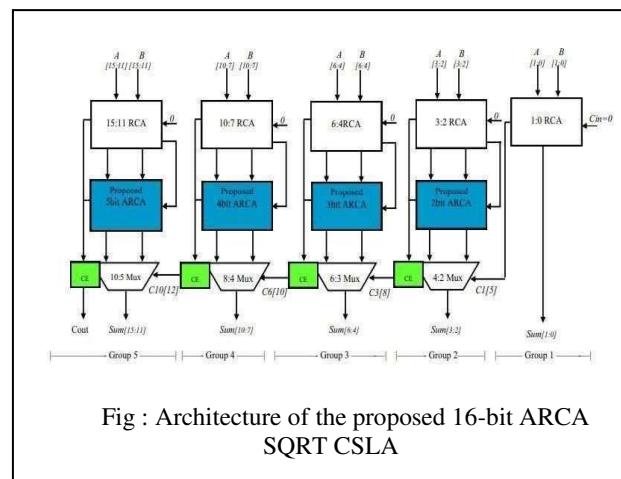


Fig : Architecture of the proposed 16-bit ARCA Sqrt CSLA

Proposed 16-bit ARCA Sqrt CSLA Design :

The second part of this which includes the proposed 16-bit ARCA Sqrt CSLA architecture and its layout using add-one ripple carry adder (ARCA) and carry enable (CE) modules for optimizing the delay, area and power consumption than the existing 16-bit regular Sqrt CSLA. The proposed architecture has five groups for area and delay estimation. The proposed m-bit ARCA module is used in this research instead of using mbit

RCA when $C_{in} = 1$, where $m = 2, 3, 4, 5$. The proposed m-bit ARCA module has $(m - 1)$ number of FAs and one add-one (A-1) logic module.

This section focuses on evaluating the proposed modification in group 5 of the 16-bit CEBEC Sqrt CSLA architecture shown in for the estimation of delay and area. The delay and area evaluation methodology considers all gates made up of AND, OR and inverter (basic logic gates), each having a delay of one unit and an area of one unit. The number of gates for delay in the longest path of each logic block contributes to the maximum delay and the area evaluation by counting the total number of basic gates required for each logic block.

Type	Regular Sqrt CSLA [20]		BEC Sqrt CSLA [20]		Sqrt CSLA1 [17]		Sqrt CSLA2 [19]		Proposed CEBEC Sqrt CSLA	
	Delay	Area	Delay	Area	Delay	Area	Delay	Area	Delay	Area
Group 1	6	19	6	19	11	26	9	23	6	19
Group 2	11	57	13	43	12	48	12	38	12	36
Group 3	13	87	16	66	14	65	14	62	14	59
Group 4	16	117	19	89	16	86	16	84	16	82
Group 5	19	147	22	112	18	109	18	106	18	105

Table :Delay and area count of 16-bit Sqrt CSLA groups



1. APPLICATIONS

1. Image Processing
2. Signal Processing
3. Advanced microprocessors design
4. High speed multiplications

V. RESULTS AND CONCLUSIONS

The proposed implementation of the high-performance square-root CSLA is very efficient. Performance of any circuit in VLSI design process is mostly determined by the power consumption, delay propagation and area. Thus, reduction in delay, total power and area is achieved by reducing the number of gates used in the proposed method. Based on the simulation results, the proposed CEBEC square root carry select adder has 20.33%, 19.92%, 10.09% and 6.89% lesser PDP, 28%, 23.85%, 13.78% and 7.58% lesser ADP and the proposed ARCA squareroot carry select adder exhibits lesser delay when compared to the existing regular, BEC SQRT CSLA, SQRT CSLA1 and SQRT CSLA2 architectures for higher speed, energy and area-efficient applications.

V. CONCLUSION AND FUTURE WORKS

The addition operation is also used to improvise all other arithmetic operations; hence, it is the basic block for well-designed implementations in an arithmetic logic unit. The method in which an adder is constructed is critical in the manufacturing of hardware integrated circuits for any processor applications; specially pertaining to the processor, the digital adders form the core block. By considering the delay time, area utilization and consumption of power, the proposed implementation of the high-performance square-root CSLA is very efficient. Performance of any circuit in VLSI design process is mostly determined by the power consumption, delay propagation and area. Thus, reduction in delay, total power and area is achieved by reducing the number of gates used in the proposed method. Based on the simulation results, the proposed CEBEC square-root carry select adder has 20.33%, 19.92%, 10.09% and 6.89% lesser PDP, 28%, 23.85%, 13.78% and 7.58% lesser ADP and the proposed ARCA square-root carry select adder exhibits lesser delay when compared to the existing regular, BEC SQRT CSLA, SQRT CSLA1 and SQRT CSLA2 architectures for higher speed, energy and area-efficient applications.

This project uses System VHDL i.e., the technology used is direct test cases, randomized test cases, OVM for verification. Even though the coverage is 100%, there may be some errors which cannot be shown. So in order to overcome this, the new technology of System VHDL is OVM and UVM. In the coming future, the Router can be done by using OVM and UVM.

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