



e-ISSN: 2319-8753 | p-ISSN: 2347-6710

# IJIRSET

International Journal of Innovative Research in  
**SCIENCE | ENGINEERING | TECHNOLOGY**



# INTERNATIONAL JOURNAL OF INNOVATIVE RESEARCH

IN SCIENCE | ENGINEERING | TECHNOLOGY

Volume 11, Issue 4, April 2022

**ISSN** INTERNATIONAL  
STANDARD  
SERIAL  
NUMBER  
INDIA

Impact Factor: 8.118



9940 572 462



6381 907 438



ijirset@gmail.com



www.ijirset.com

# Survey of Parallel FIR $2 \times 2$ Filter using Vedic Multiplier and Kogge Stone Adder

Sangam Yadav<sup>1</sup>, Prof. Satyarth Tiwari<sup>2</sup>, Prof. Amrita Pahadia<sup>3</sup>

M. Tech. Scholar, Department of Electronics and Communication, Bhabha Engineering Research Institute,  
Bhopal, India<sup>1</sup>

Guide, Department of Electronics and Communication, Bhabha Engineering Research Institute, Bhopal, India<sup>2</sup>

Co-guide, Department of Electronics and Communication, Bhabha Engineering Research Institute, Bhopal, India<sup>3</sup>

**ABSTRACT:** Several VLSI architectures have been suggested for the parallel FIR Filter in last decade to meet space and time requirement of real-time application. All these designs differ by arithmetic complexity, cycle period, throughput rate and they use almost same amount of on-chip memory words and equal amount of frame buffer words. The mainly digital signal processing system depends on the multiplier. Vedic Multipliers has been used to solve the typical and tedious engineering calculation by simple Vedic methods. Here in this paper we have proposed  $2 \times 2$  and  $3 \times 3$  parallel FIR filter with kogge stone adders replacing the traditional carry select adder. The Vedic multiplier has also been designed using this Kogge-stone adder to improve the propagation delay time and area on silicon chip. With this slight improve in the multiplier, great results have been achieved in signal processing tasks. All the design is implemented Xilinx software with different device family.

**KEYWORDS:** Kogge Stone Adder, Vedic Multiplier,  $2 \times 2$  Parallel FIR Filter,  $3 \times 3$  Parallel FIR Filter, Delay, Slice Flip Flop

## I. INTRODUCTION

Due to the explosive growth of multimedia application, the demand for high-performance and low-power digital signal processing (DSP) is getting higher and higher. Finite-impulse response (FIR) digital filters are one of the most widely used fundamental devices performed in DSP systems, ranging from wireless communications to video and image processing [1]. Some applications need the FIR filter to operate at high frequencies such as video processing, whereas some other applications request high throughput with a low-power circuit such as multiple-input multiple-output (MIMO) systems used in cellular wireless communication. Furthermore, when narrow transition-band characteristics are required, the much higher order in the FIR filter is unavoidable. For example, a 27-tap digital filter is used in a video ghost canceller for broadcast television, which reduces the effect of multipath signal echoes [2]. On the other hand, parallel and pipelining processing are two techniques used in DSP applications, which can both be exploited to reduce the power consumption. Pipelining shortens the critical path by interleaving pipelining latches along the data path, at the price of increasing the number of latches and the system latency, whereas parallel processing increase the sampling rate by replicating hardware so that multiple inputs can be processed in parallel and multiple outputs are generated at the same time, at the expense of increased area [3]. Both techniques can reduce the power consumption by lowering the supply voltage, where the sampling speed does not increase. In this paper, parallel processing in the digital FIR filter will be discussed.

## II. LITERATURE REVIEW

S Narendran et al. [1], a definitive objective of the examination work is to dissect the exhibition of FIR channel planned in view of FFA calculation. The proposed structure focuses on region improved adders which are intended for symmetric coefficient that diminishes equipment cost in the plan with an oblige that the channel tap is of even request. Region investigation of silicon chip is performed utilizing various adders like Ripple Carry Adder (RCA), Carry Look-Ahead Adder (CLA) and Conditional Sum Adder (COS). Execution examination report for a 3 equal 96-tap channel is viewed as founded on the above viper, where the RCA requires less region use contrasted with other three adders. The symmetric convolution-based RCA Fast FIR Algorithm (FFA) structure requires just 896 cuts while COS requires 1024 cuts and CLA requires 960 cuts. For higher-request, FIR channel design of 1024 or higher taps, the reserve funds in the space usage for RCA based FFA is roughly 10% and 15% contrasted with CLA and COS based FFA separately in light

of the fact that COS requires more equipment building blocks. The RCA based FFA expands the idleness by around 9% and 7% contrasted with CLA and COS based FFA separately, and there will be a compromise.

**K. Anjali Rao et al. [2]**, in this paper, we propose 3-equal limited motivation reaction (FIR) structures with the use of polyphase coefficient evenness and quick FIR calculations (FFAs). For symmetric convolution of odd length channel The proposed structures are advantageous as far as the quantity of multipliers which can lessen the execution intricacy of the equal FIR channels. At first, 3-equal customary FIR structures are reconfigured so that the polyphase coefficient evenness of odd length FIR channels can be applied for the decrease of the half number of multipliers, from there on, FFAs are utilized for bringing down the equal subfilter parts of a polyphase channel. On contrasting the presentation and existing comparative designs the proposed FFA based structure is tracked down unrivaled concerning diminished number of required multipliers.

**Yi Zheng et al. [3]**, to make students ace an equipment execution of computerized channels, we take the plan of an equal FIR advanced low-pass channel as a showing case, which can introduce the execution strategy for computerized channels joining Matlab and an equipment portrayal language together. In the first place, as per the undertaking of the showing case, the coefficients of FIR advanced not entirely settled by a FDATool utilization of Matlab. By standardization and quantization, the channel coefficients and examined information are both changed over from the drifting point information to the fixed-point information. The digit width of substantial information pieces of FIR channel still up in the air as per the standard of increase gather activity of FPGAs. Then, at that point, we use Verilog HDL to execute a quick multiplier and the equal FIR computerized low-pass channel. At long last, we contrast the channel results of FPGAs and the ones of Matlab, and investigate the explanation. The case showing technique, which consolidates Matlab and FPGAs, is useful to foster the equipment execution capacity of computerized signal handling of students.

**S. Sreekanth et al. [4]**, in this paper, Polyphase Finite Impulse Response (FIR) computerized channel is planned and carried out by utilizing 40 nm LP CMOS TSMC Library. For some advanced channelized collectors and transmitters in computerized correspondence frameworks the speed of FIR channel and idleness are significant elements. Polyphase channel is executed with equal methodology in which equal multipliers, adders and FFT block utilizing the Radix-2 2 calculation are utilized. Radix-2 2 purposes not many multipliers contrasted with Radix-2 calculation. In this work elite execution is accomplished contrasted with ordinary direct structure plan and different plans.

**Qiaoyu Tian et al. [5]**, the Cook-Toom calculation is generally utilized in short-length direct convolution, which is the structure square of enormous focuses convolution calculations. This paper proposes further developed equal limited motivation reaction (FIR) channel structures for direct stage FIR channel, which depends on the Cook-Toom calculation. In the proposed structures, Cook-Toom calculation is utilized to diminish the quantity of sub-channels, and the symmetric properties of the straight stage FIR channel's coefficients is utilized to additionally lessen the quantity of multipliers in sub-channels. Contrasted and the announced FFA and ISCA equal FIR channel structures, the proposed technique can significantly decrease the computational intricacy. In particular, for a 8-equal 144-tap channel, the proposed plan saves 18 multipliers (5%), 45 adders (7.9%) contrasted and the construction in light of Winograd convolution calculation.

**Payal Paliwal et al. [6]**, equal FIR channel is the need of many low power and rapid DSP applications. In this paper, quick FIR calculation based equal symmetric FIR channel utilizing Han-Carlson snake based vedic multiplier is proposed. FFA calculation lessens the multiplier consider contrasted with the conventional equal plan. To work on the presentation of the proposed channel, as of late evolved Han-Carlson viper based Vedic multiplier is utilized. In the proposed plan the viper unit is additionally carried out utilizing Han-Carlson snake. In the proposed plan two and three equal FIR channels of request 24 and 72 are executed utilizing VHDL. The execution results show that the proposed engineering gives low basic way deferral and power dispersal when contrasted with the regular one. With the upside of low postponement and power, proposed design is valuable in present day signal handling and correspondence applications.

**Swetha Annangi et al. [7]**, in this paper, a 144-tap 16-equal Fast Finite Impulse Response (FIR) Algorithm (FFA) channel structure is planned utilizing verilog HDL. The planned channel structure is mimicked utilizing XILINX ISE 14.7. The planned module is combined utilizing CADENCE RTL Compiler and the application explicit incorporated circuit (ASIC) plan of the proposed channel structure is executed utilizing CADENCE apparatus set on CADENCE GPD45nm innovation. By applying Fast FIR Algorithm, 65% of multipliers are diminished and the quantity of adders are expanded. The adders possess less silicon region than multipliers. Subsequently, the decrease in region is



accomplished by supplanting the multipliers with adders. Further, the proposed 16 equal FFA channel structure lessens the postpone when contrasted with 16 equal FIR channel structure without applying Fast FIR Algorithm. The proposed channel engineering involves an area of 79220 sq.  $\mu\text{m}$  and consumes a force of 20mW at 333MHz when integrated.

**Shalina Percy et al. [8]**, have the requirement for productive Finite Impulse Response (FIR) channels in fast applications targets Field Programmable Gate Arrays (FPGAs) as a powerful and adaptable stage for computerized execution. In spite of the fact that FIR channel offer benefits like direct stage trademark, no criticism circles and great framework strength, its convolution nature balances a test in parallelization because of information reliance and computational intricacy. To determine this, we propose a clever FPGA-based reconfigurable channel engineering, which processes a few information tests in equal and separates information interdependency in a twisting design. This conventional pipelined-equal channel is parameterizable as far as channel request and level of parallelization. Exploratory outcomes show a throughput of 7.2 GSPS with a working recurrence of just 450 MHz for a channel length of 11 with 16 equal sources of info. With parallelization of 4, it is 4.64 times quicker than the best in class answer for a channel length of 16 and a promising 41% expansion in throughput is accomplished for a higher request of 61.

### III. VEDIC MULTIPLIER USING KOGGE STONE ADDER

As specified prior, Vedic Mathematics can be isolated into 16 unique sutras to perform scientific counts. Among these the Urdhwa Tiryakbhyam Sutra is one of the most exceedingly favored calculations for performing increase. The calculation is sufficiently able to be employed for the duplication of whole numbers and also binary numbers. The expression "Urdhwa Tiryakbhyam" started from 2Sanskrit words Urdhwa and Tiryakbhyam which mean "vertically" and "transversely" respectively. It depends on a novel idea through which the era of every single fractional item should be possible with the simultaneous expansion of these halfway items. The calculation can be summed up for  $n \times n$  bit number. Since the incomplete items and their totals are figured in parallel, the multiplier is free of the clock recurrence of the processor. In this way the multiplier will require the same measure of time to figure the item and henceforth is free of the clock recurrence.

The net advantage is that it reduces the need of microprocessors to operate at increasingly high clock frequencies. While a higher clock frequency generally results in increased processing power, its disadvantage is that it also increases power dissipation which results in higher device operating temperatures. The processing power of multiplier can easily be increased by increasing the input and output data bus widths since it has a quite a regular structure. Due to its regular structure, it can be easily layout in a silicon chip. The Multiplier has the advantage that as the number of bits increases, gate delay and area increases very slowly as compared to other multipliers. Therefore it is time, space and power efficient.

To illustrate this multiplication scheme, let us consider the multiplication of two decimal numbers ( $14 \times 12$ ).

#### Example- $14 \times 12$

- The right hand most digit of the multiplicand, the first number (14) i.e., 4 is multiplied by the right hand most digit of the multiplier, the second number (12) i.e., 2. The product  $4 \times 2 = 8$  forms the right hand most part of the answer.

$$\begin{array}{r} 14 \\ \times 12 \\ \hline 8 \end{array}$$

- Now, diagonally multiply the first digit of the multiplicand (14) i.e., 4 and second digit of the multiplier (12) i.e., 1 (answer  $4 \times 1 = 4$ ); then multiply the second digit of the multiplicand i.e., 1 and first digit of the multiplier i.e., 2 (answer  $1 \times 2 = 2$ ); add these two i.e.,  $4 + 2 = 6$ . It gives the next, i.e., second digit of the answer. Hence second digit of the answer is 6.

$$\begin{array}{r} 14 \\ \times 12 \\ \hline 68 \end{array}$$

- Now, multiply the second digit of the multiplicand i.e., 1 and second digit of the multiplier i.e., 1 vertically, i.e.,  $1 \times 1 = 1$ . It gives the left hand most part of the answer. Thus the answer is 16 8.

$$\begin{array}{r} 1 \quad 4 \\ \downarrow \\ 1 \quad 2 \\ \hline 1 \quad 6 \quad 8 \end{array}$$

- Thus the answer is 16 8.

### 8-BIT VEDIC MULTIPLIER USING KS ADDER

The multiplication of two numbers is done by using Urdhwa Triyakbhyam. Here first the least significant bits of the two digits are multiplied. Then the intermediate digits are cross multiplied and added together. After this the most significant digits are multiplied. For the 16X16 bit multiplication small block of 2X2 or 4X4 or 8X8 multiplier were used in parallel to make the process easy and efficient.

In our proposed method the high speed carry select adder is replaced by the carry select adder along with Kogge Stone (KS) adder which claims to provide a better speed and less propagation delay. Here we have used four multiplier of 8 bit to perform 16 bit multiplication. The method used is the addition of all partial product formed by the cross multiplication of one bit with another. The LSB bits of first multiplier P1 (7-0) gives the LSB bits Q (7-0) of the final output. Another bits of first multiplier P1 (15-8) are added in series with LSB 8 bits of second multiplier to form the 16 bits, which in turn get added with 16 bits of third multiplier by using KS Adder. The LSB bits of the output of KS adder forms the Q (15-8) bits of the final output. The remaining 8 bit P2(15-8) is then added with the left 8 bits of KS output to form 16 bits, which is then added with 16 bits of the fourth multiplier by using KS 2 adder. The output from KS 2 adder forms the Q (31-16) bits. This is how the 32bit output is achieved in the less possible time.

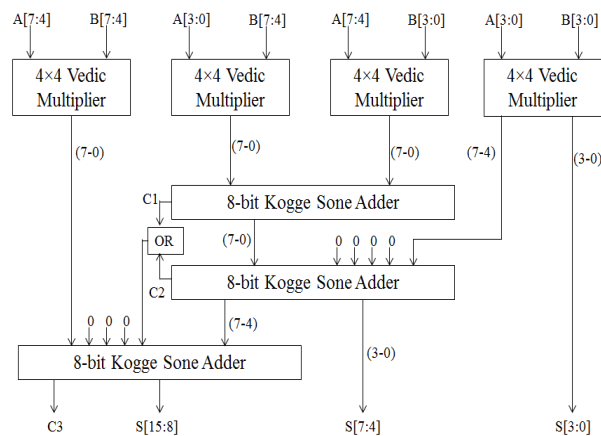


Figure 1: Logic Diagram of 8-bit Vedic Multiplier using Kogge Stone Adder

### 16X16-bit VEDIC MULTIPLIER USING KOGGE STONE ADDER

The multiplication of two numbers is done by using Urdhwa Triyakbhyam. Here first the least significant bits of the two digits are multiplied. Then the intermediate digits are cross multiplied and added together. After this the most significant digits are multiplied.

For the 16X16 bit multiplication small block of 2X2 or 4X4 or 8X8 multiplier were used in parallel to make the process easy and efficient.

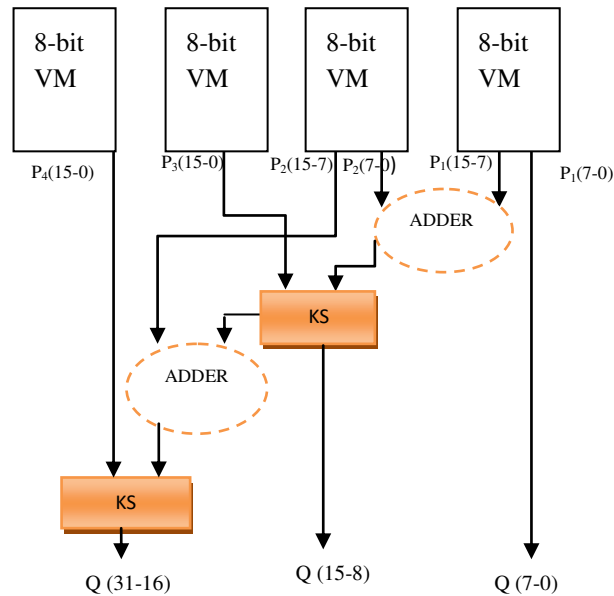


Figure 2: Proposed 16x16 Vedic Multiplier

In our proposed method the high speed carry select adder is replaced by the carry select adder along with Common Boolean logic which claims to provide a better speed and less propagation delay. Here we have used four multiplier of 8 bit to perform 16 bit multiplication. The method used is the addition of all partial product formed by the cross multiplication of one bit with another. The LSB bits of first multiplier  $P_1$  (7-0) gives the LSB bits  $Q$  (7-0) of the final output. Another bits of first multiplier  $P_1$  (15-8) are added in series with LSB 8 bits of second multiplier to form the 16 bits, which in turn get added with 16 bits of third multiplier by using CBL 1 Adder. The LSB bits of the output of CBL 1 adder forms the  $Q$  (15-8) bits of the final output. The remaining 8 bit  $P_2$ (15-8) is then added with the left 8 bits of CBL 1 output to form 16 bits, which is then added with 16 bits of the fourth multiplier by using CBL 2 adder. The output from CBL 2 adder forms the  $Q$  (31-16) bits. This is how the 32bit output is achieved in the less possible time.

#### IV. PROPOSED METHODOLOGY

In general, two parallel FIR filter can be expressed as traditional two parallel digital filters is shown in figure 3. For this two parallel FIR filter  $L=2$ . This will require three FIR sub-filter blocks of length  $N/2$ , one pre-processing adder and three post-processing adders. Total number of multiplier and adders required are  $3N/2$  and  $3(N/2-1) + 4$  respectively.

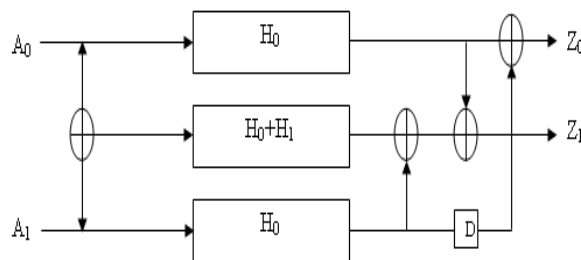


Figure 3: Parallel 2x2 FIR Filter

Following are the equations used to design the two parallel FIR filter with two inputs  $A_0$ ,  $A_1$  and two outputs  $Z_0$ ,  $Z_1$ . For implementing this filter three FIR sub-filter blocks has been used as compare to traditional two FIRs sub-block filter, having length  $N/3$ . Two of three sub-filters  $H_0+H_1$  and  $H_0-H_1$  are having symmetric coefficient which reduces

the number of multiplier and adders. Here two preprocessing and four post-processing adders have been used along with delay equipment. The symmetric sub-filter block has been implemented at the cost of two additional adders among those one is pre-processing and other one is post-processing for  $L=2$ . Following are the equations used to design the filter:

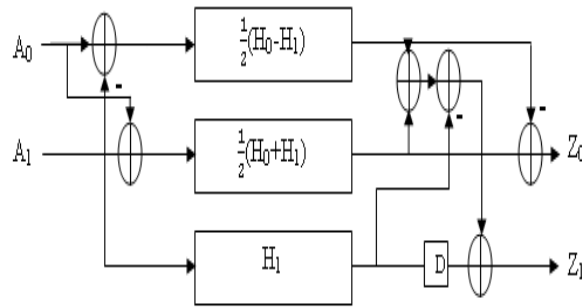


Figure 4: Proposed Parallel 2x2 FIR Filter

This same process is used for the  $n$  number of bits and thus we get the final sum and carry as output.

Example 1: Consider a 33-tap FIR filter with a set of symmetric coefficient as follows:

$\{h(0), h(1), h(2), h(3), h(4), \dots, h(29), h(30), h(31)\}$

Where

$$h(0) = h(32),$$

$$h(1) = h(31),$$

$$h(2) = h(29),$$

$$h(3) = h(28)$$

.....

$$h(12) = h(20)$$

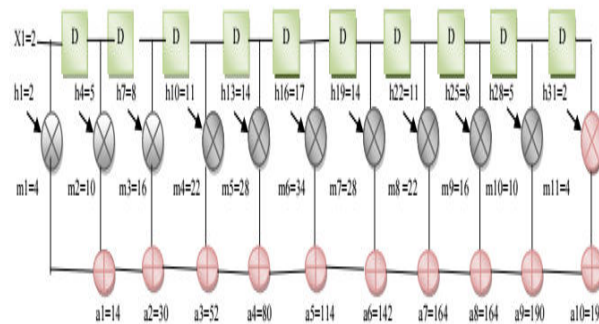


Figure 5: Internal Structure of H1

The symmetric parallel FIR filter is shown in Figure 3. The three parallel FIR filter consists of filter blocks. The input to the system is represented as  $A_0, A_1$  and the response of the system as  $Z_0$  and  $Z_1$ . Let  $X_0=5, X_1=2, X_2=3$ . The filter blocks  $H_1$  with its mod 3 coefficients are shown in Figure 3.

The proposed high speed Vedic multiplier is used in parallel FIR architecture. The proposed technique improves the speed of FIR filters and area utilization when compared to traditional Vedic multiplier.

## V. CONCLUSION

The proposed 16x16 Vedic multiplier architecture has been designed and synthesized using on Spartan 3 XC3S400 board and is used in parallel FIR filter design. The proposed Vedic Multiplier with carry select adder is compared with the existing Vedic multiplier using Carry select adder along with Common Boolean Logic and can be inferred that

proposed architecture is faster compared to existing Vedic multiplier. In future the proposed multiplier performance parameters can be improved by high level pipelining operations and applied in signal processing applications like image processing and video processing.

## REFERENCES

- [1] S Narendran and B T Geetha, "Performance Analysis of Parallel FIR Digital Filter Based on Even Symmetric Fast FIR Algorithm using Different Adders", 5th International Conference on Electronics, Communication and Aerospace Technology (ICECA), IEEE 2021.
- [2] K. Anjali Rao;Abhishek Kumar;Neetesh Purohit, "Efficient Implementation for 3-Parallel Linear-Phase FIR Digital Odd Length Filters", IEEE 4th Conference on Information & Communication Technology (CICT), IEEE 2020.
- [3] Yi Zheng;Ping Zheng, "Case Teaching of Parallel FIR Digital Filter Design Combined Matlab with FPGAs", International Conference on Artificial Intelligence and Education (ICAIE), IEEE 2020.
- [4] S. Sreekanth; Pratima B. Shinde; G. Vijaya Durga, "Performance Analysis of Higher Order FIR Polyphase Filter", Second International Conference on Intelligent Computing and Control Systems (ICICCS), IEEE 2018.
- [5] Qiaoyu Tian;Yinan Wang;Guiqing Liu;Xiangyu Liu;Jietao Diao, Hui Xu, "Hardware Efficient Parallel FIR Filter Structure Based on Modified Cook-Toom Algorithm", IEEE Asia Pacific Conference on Circuits and Systems (APCCAS), IEEE 2018.
- [6] Payal Paliwal;Janki Ballabh Sharma, "Efficient FPGA Implementation Architecture of Fast FIR Algorithm Using Han-Carlson Adder Based Vedic Multiplier", International Conference on Inventive Research in Computing Applications (ICIRCA), IEEE 2018.
- [7] Swetha Annangi;Ravisankar Puli, "ASIC implementation of efficient 16-parallel fast FIR algorithm filter structure", 8th International Conference on Computing, Communication and Networking Technologies (ICCCNT), IEEE 2017.
- [8] Shalina Percy Delicia Figuli;Peter Figuli;Jürgen Becker, "A reconfigurable high-speed spiral FIR filter architecture", 40th International Conference on Telecommunications and Signal Processing (TSP), IEEE 2017.
- [9] Shahnam Mirzaei, Anup Hosangadi, Ryan Kastner, "FPGA Implementation of High Speed FIR Filters Using Add and Shift Method", 1-4244-9707-X/06/\$20.00@2006 IEEE.
- [10] Amina Naaz.S, Mr.Pradeep M.N, Satish Bhairannawar and Srinivas halvi, "FPGA Implementation Of High Speed Vedic Multiplier using CSLA For Parallel Fir Architecture", 2014 2nd International Conference on Devices, Circuits and Systems (ICDCS).
- [11] Laxman P.Thakre, Suresh Balpande, Umesh Akare, Sudhir Lande, "Performance Evaluation and Synthesis of Multiplier used in FFT operation using Conventional and Vedic algorithms," Third international conference on emerging trends in Engineering and Technology , IEEE, 2010.
- [12] S. S. Kerur, Prakash Narchi, Jayashree C N, Harish M Kittur and Girish V. A., "Implementation of Vedic Multiplier for Digital Signal Processing," International Conference on VLSI ,Communication & Instrumentation (ICVCI), 2011.
- [13] G.Vaithyanathan, K.Venkatesan, S.Sivaramakrishnan, S.Sivaand, S.Jayakumar, "Simulation and implementation of Vedic multiplier usingVHDL code," International Journal of Scientific & Engineering Research, vol.4, 2013.
- [14] Pushpalata Verma and K. K. Mehta, "Implementation of an Efficient Multiplier based on Vedic Mathematics Using EDA Tool," International Journal of Engineering and Advanced Technology(IJEAT), vol.1, June 2012.
- [15] C. Cheng and K. K. Parhi, "Further complexity reduction of parallel FIR filters," in Proc. IEEE ISCAS, May 2005, vol. 2, pp. 1835–1838.
- [16] C. Cheng and K. K. Parhi, "Low-cost parallel FIR structures with 2-stage parallelism," IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 54, no. 2, pp. 280–290, Feb. 2007.
- [17] J. G. Chung and K. K. Parhi, "Frequency-spectrum-based low-area low-power parallel FIR filter design," EURASIP J. Appl. Signal Process., vol. 2002, no. 9, pp. 444–453, Jan. 2002.
- [18] K. K. Parhi, VLSI Digital Signal Processing systems: Design and Implementation. New York: Wiley, 1999.
- [19] Nivedita A. Pande, Vaishali Niranjane, Anagha V. Choudhari, " Vedic Mathematics for Fast Multiplication in DSP," International Journal of Engineering and Innovative Technology (IJEIT) ,vol.2, 2013.
- [20] Krishnaveni D. and Umarani.T.G, "Vlsi implementation of Vedic multiplier with reduced delay," International Journal of Scientific & Engineering Research, vol.2, May-2011.





**INNO SPACE**  
SJIF Scientific Journal Impact Factor  
**Impact Factor: 8.118**



**ISSN** INTERNATIONAL  
STANDARD  
SERIAL  
NUMBER  
**INDIA**



# INTERNATIONAL JOURNAL OF INNOVATIVE RESEARCH

IN SCIENCE | ENGINEERING | TECHNOLOGY

 **9940 572 462**  **6381 907 438**  **ijirset@gmail.com**



[www.ijirset.com](http://www.ijirset.com)

Scan to save the contact details