



e-ISSN: 2319-8753 | p-ISSN: 2347-6710

IJIRSET

International Journal of Innovative Research in
SCIENCE | ENGINEERING | TECHNOLOGY



INTERNATIONAL JOURNAL OF INNOVATIVE RESEARCH

IN SCIENCE | ENGINEERING | TECHNOLOGY

Volume 11, Issue 2, February 2022

ISSN INTERNATIONAL
STANDARD
SERIAL
NUMBER
INDIA

Impact Factor: 7.569



9940 572 462



6381 907 438



ijirset@gmail.com



www.ijirset.com



Leakage Power Reduction Technique for Network Routing Using TCAM

N.Subharathna¹, K.Sharmilee²

PG Scholar, Department of Electronics and Communication Engineering, Nandha Engineering College, Erode,
Tamil Nadu, India¹

Assistant Professor, Department of Electronics and Communication Engineering, Nandha Engineering College, Erode,
Tamil Nadu, India²

ABSTRACT: Ternary content on the market recollections (TCAMs) unit of measure hardware-based parallel operation tables with bit-level masking capability, they're collaborating for applications like packet forwarding and classification in network routers. Despite the collaborating selections of TCAMs, high power consumption is one in every of the foremost essential challenges two-faced by TCAM designers. The ternary content on the market memory (TCAM) is wide used among the routing table as a result of its high operation performance. However, AN outsize vary of transistors would cause the ability consumption of TCAM to be sizable. throughout this transient, a recent state-preserved technique, named data retention based totally TCAM (DR-TCAM), is planned to cut back the escape power dissipated at intervals the TCAM memory. in step with the continual feature of mask data, the DR-TCAM will dynamically adapt the ability supply of mask cells therefore on shrink the TCAM escape power. significantly, the mask data would not be destroyed at intervals the DR-TCAM. supported TSMC 40nm technology, the simulation results show that the DR-TCAM performs on the far side the progressive works. Compared to the standard TCAM vogue, the DR-TCAM will deliver a TCAM escape power reduction of forty first for a bunch of real routing tables. Besides, the final power reduction is relating to twelve-tone system.

I. INTRODUCTION

Fantastic growth within the variety of web users and also the increasing quality of bandwidth-hungry period of time applications have resulted terribly demand for very high-speed networks. the net may be a mesh of routers and switches, that method information packets and forwards them toward their destinations. every packet contains a header and a payload. The header contains data like a supply address, a destination address, the info length, a sequence variety and also the information form of the packet. A network switch transfers associate degree incoming information packet to associate degree output port supported the data within the header of the packet. A router may be a lot of refined switch that forwards associate degree incoming packet once routing its path from the supply to the destination . every router maintains a routing table and forwards incoming packets supported the data keep within the routing table. Routers conjointly communicate with each other to update their routing tables.

II. LITERATURE SURVEY

“A Static Power Reduction Technique for Ternary Content available Memories” Ternary content available reminiscences (TCAMs) area unit enticing for high-speed packet forwarding and classification in network switches and routers. historically, the static power in TCAMs has been a little fraction of the whole power because of high activity of TCAMs. However, technology scaling and design level techniques area unit reducing the dynamic power of TCAMs. The technology scaling is additionally increasing the off-current of transistors. Hence, the static power is turning into a major portion of the whole power consumption in TCAMs. This paper presents a method to cut back the static power in SRAM-based TCAMs while not poignant the speed of operation. “Low escape mask vertical management TCAM for network router” Ternary content available memory (TCAM) is mostly employed in the network router since it will perform the parallel information science operation. However, the ability consumption of ancient router is sizable. notably, the escape power can increase because the technology feature size shrinks. during this paper, a TCAM design with mask vertical management (MVC) technique is projected to cut back the escape power of network router. within the forwarding table, supported the information science hold on so as of prefix length, the MVC technique will shut down the spare power provide to cut back the escape power. The TCAM with the MVC technique was simulated by victimization the TSMC 90nm method. Compared with the standard TCAM design, the MVC theme can do concerning

twenty first escape power reduction. “Filter-Based Dual-Voltage design for Low-Power Long-Word TCAM Design” Ternary Content available Memory (TCAM) provides superior table-lookup performance to the traditional search algorithms. However, as word length will increase, large-sized TCAM suffers from high power consumption and output degradation. This paper presents filter-based twin voltage design for long-word TCAM. While not sacrificing output and noise immunity, the projected filter-based twin voltage design will cut back ample dynamic and static power consumption. Simulation results show that the projected technique can do 87 of dynamic power and sixty three static power reduction in 40nm CMOS technology in comparison with ancient TCAM architectures.

III. EXISISTING SYSTEM

A. Ancient TCAM design As shown in Fig. 1, a TCAM cell consists of 3 elements, i.e., XOR-type CAM cell, analysis logic, and SRAM cell. The XOR-type CAM cell stores information in the infothe information (D) that may be compared with the search data (SL and $\sim S-L$). The SRAM cell stores the mask knowledge (M) to point whether or not this TCAM cell is in don't-care state (i.e., “X” state) or not. once the TCAM cell is within the “X” state, the compare result should be matched.

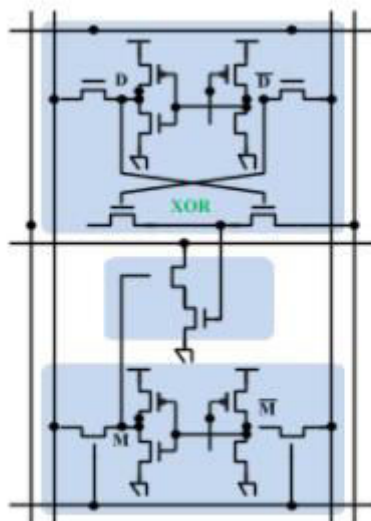


Fig.1.a One ancient TCAM cell consists of XOR-type CAM cell, analysis logic, and SRAM cell.

The function of the network router is forwarding the input packets to alternative routers in step with the destination scientific discipline address of the packet header. The mask (prefix) bit is employed to work out the domain of IPv4 (IPv6) address. TABLE I shows the samples of IPv4 address mask and also the corresponding domain address. A TCAM entry stores the scientific discipline knowledge within the CAM cells and also the mask knowledge within the SRAM cells. as an example, 140.120.7.14/24 will be divided into 2 elements. The IP 140.120.7.14 is hold on within the CAM cells. The mask length is 24 that is hold on within the SRAM cells as 255.255.255.0, i.e., 11111111.11111111.11111111.00000000. The domain of this scientific discipline address will be calculated by victimization logical AND, and also the result's 10001100.01111000.00000111.00000000, i.e., 140.120.7.0. the quantity 24 represents that there square measure twenty four care bits and eight don't- care bits during this scientific discipline. As shown in TABLE I, it's obvious that the mask knowledge consists of continuous 1s and 0s.

IV. WORKING

The TCAM Input entry is portioned into four segments

1) Segments S1 and S2 (all 1s phase): within the all 1s segment, the PSM and PSL area unit each H so the VDD methods and GND methods of internal SRAM cells area unit each set to VDD. This makes the inner cells' knowledge M6 to M1 remaining one, however the inverse knowledge Mb6 to Mb1 area unit raised from zero to 1–, as shown in



Fig. 4(b). as a result of the voltage distinction between VDD and GND path of the inner mask cells is reduced, the run power may be for the most part reduced.

2) Segment S4 (all 0s phase): within the all 0s segment, the VDD and GND methods of internal SRAM cells area unit each set to GND. This makes the inner cells' knowledge M6 to M1 still remaining zero, however the inverse knowledge Mb6 to Mb1 area unit discharged from one to 0-. Similarly, the run power consumption may be for the most part reduced.

3) Segment S3 (boundary phase): within the boundary segment, the mutual savings bank M7 should be one and also the LSB M0 should be zero. consequently, the PSM and PSL area unit set to VDD and GND, such the inner SRAM cells work as traditional. No run power may be saved during this case.

TCAM Cell:

A typical one6T static TCAM cell is shown in Figure 1.6. it's almost like the binary CAM cell except that it's 2 SRAM cells to store ternary information, as shown in Figure one.6. READ, WRITE and SEARCH operations during this cell square measure performed within the same approach as delineated in section one.1.1. For the given circuit vogue, masking are often achieved by turning off each ML-to- GND pull-down ways. as an example, international masking is performed by $SL1 = SL2 = '0'$, and native masking is achieved by $Vx = Vy = '0'$. A CAM Array A CAM word (1-bit) is enforced by connecting (l) CAM cells in parallel. All the cells during a exceeding a very CAM word share an cubic centimeter however they need separate SLs.

The cubic centimeter is connected to a cubic centimeter sense electronic equipment (MLSA), that determines if the corresponding word matches with the search key. throughout this operation, the cubic centimeter remains at VDD provided that the cell-level comparisons of all the bits end in "match". In alternative words, even a single-bit "mismatch" will produce a discharge path for cubic centimeter indicating a word (l- bit) "mismatch".

This work focuses on the SRAM-based TCAMs because of 2 main reasons:

- i)SRAM-based TCAMs square measure compatible with the regular CMOS logic method.
- ii)Most industrial TCAM vendors have moved aloof from DRAM-based TCAMs.

V.PROPOSED WORK

The planned work can processed to exchange the SRAM primarily based TCAM with the memristor TCAM , so the low power leak are going to be achieved with one.8 provide voltage. This presents a Ternary Content available Memory (TCAM) cell that employs memristors as storage component. The TCAM cell needs 2 memristors nonparallel to perform the standard memory operations (read and write) moreover because the search and matching operations for TCAM; this memory cell is analyzed with relation to totally different options (such as memristance vary and voltage threshold) of the memristors to method quick and expeditiously the ternary information. A comprehensive simulation primarily based assessment of this cell is pursued by HSPICE. Comparison with different memristor-based CAMs moreover as CMOS-based TCAMs shows that the planned cell offers important benefits in terms of power dissipation, reduced electronic transistor count and search/match operation performance.

A content-addressable memory compares Associate in Nursing input search word against all rows of hold on words during an array in a extremely parallel manner. whereas provision a really powerful functionality for several applications in pattern matching and search, it suffers from massive area, value and power consumption, limiting its use. Past enhancements are complete by victimization memristors to switch the static random-access memory cell in typical styles, however use similar schemes based mostly solely on binary or ternary states for storage and search. we tend to propose a replacement analog content-addressable memory idea logic gate to beat these limitations by utilizing the analog electrical phenomenon tunability of memristors. Our analog content-addressable memory stores information at intervals the programmable electrical phenomenon and may take as input either analog or digital search values. Experimental demonstrations, scaled simulations and analysis show that our analog content-addressable memory will scale back space and power consumption, that allows the acceleration of existing applications, however additionally new computing application areas.

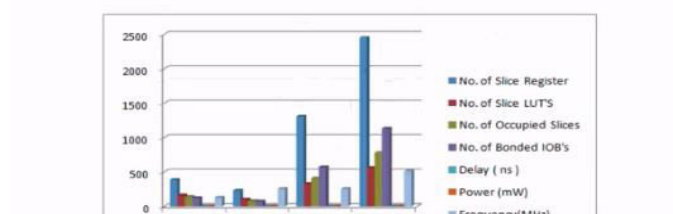
VI. RESULTS

In this paper, all TCAM styles are enforced with TSMC 40nm technology and simulated with HSPICE in 25°C and one.0V power provide. The TCAM size is 1024 × 32, which suggests that there are 1024 entries, and every entry is 32-bit. Here, the input word size is 1119:0 and also the address bit is 8:0.

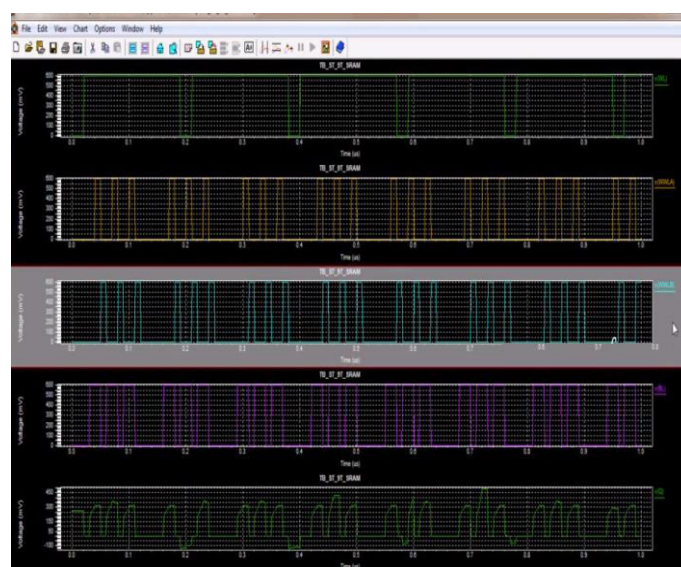
The Structure having four blocks of SRAM, every sub-blocks contains 512x280. The input to the TCAM are given only

the information writing method gets completed. The input word have to be compelled to run among a 1 clock cycle. For a true information distribution, 3 routing table benchmarks from BGP Report , as well as AS1221, EQIX, and APNIC, square measure won't to examine all TCAM styles. to focus on the prevalence of DR-TCAM in outflow power reduction, besides the normal TCAM style, 3 low-leakage styles, as well as DPS-TCAM , TSSG-TCAM , and MVC-TCAM , also are enforced and simulated with the same condition for comparison.

	Case I 512x28 (P=4)	Case II 512x32 (P=2)	Case III 1024x140 (P=4)	Case IV 2048x280 (P=4)
No. of Slice Register	388	232	1308	2450
No. of Slice LUTS	162	101	330	560
No. of Occupied Slices	139	81	408	779
No. of Bonded IOB's	122	76	572	1133
Delay (ns)	3.187	3.264	3.300	3.457
Power (mW)	3.309	3.301	3.322	3.370
Frequency(MHz)	128	256	256	512



A. SIMULATION RESULTS



VII. CONCLUSION

TCAMs area unit gaining importance in high-speed lookup-intensive applications. However, the high power consumption of TCAMs is limiting their quality and flexibility. This work planned many circuit techniques to cut back TCAM power consumption, that is usually dominated by the frequent shift of MLs and SLs. the most contribution of this work has been in reducing the milliliter energy using:

(i) positive-feedback MLSAs, (ii) low-capacitance comparison logic, and (iii) low-power milliliter segmentation techniques (such as twin milliliter and charge-shared ML). Additionally, this work planned techniques to cut back the



static power consumption, that is turning into a priority in TCAMs using low-power architectures.

REFERENCES

1. N. Mohan, and M. Sachdev, "A Static Power Reduction Technique for Ternary Content Addressable Memories," Proceedings of the IEEE Canadian Conference on Electrical and Computer Engineering (CCECE), Niagara Falls, pp. 711-714, May 2- 5, 2004.
2. N. Mohan, and M. Sachdev, "Low power dual matchline ternary content addressable memory," Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS), Vancouver, pp. 633-636, May 23-26, 2004.
3. N. Mohan, and M. Sachdev, "A comparative study of low-power techniques for ternary CAMs," Proceedings of the IEEE International Conference for Upcoming Engineers (ICUE), Waterloo, Ontario, Canada, May 13-14, 2006.
4. N. Mohan, W. Fung, D. Wright, and M. Sachdev, "Design techniques and test methodology for low-power TCAMs," IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 14, no. 6, pp. 573-586, Jun. 2006.
5. N. Mohan, W. Fung, D. Wright, and M. Sachdev, "Match line sense amplifiers with positive feedback for low-power content addressable memories," Proceedings of the IEEE Custom Integrated Circuits Conference (CICC), San Jose, Sep. 11-13, 2006.
6. N. Mohan, and M. Sachdev, "Novel ternary storage cells and techniques for leakage reduction in ternary CAM," Proceedings of the IEEE International SOC Conference (SOCC), Austin, Texas, Sep. 24-27, 2006.
7. N. Mohan, W. Fung, and M. Sachdev, "Low-power priority encoder and multiple match detection circuit for ternary content addressable memory," Proceedings of the IEEE International SOC Conference (SOCC), Austin, Texas, Sep. 24-27, 2006.
8. N. Mohan, and M. Sachdev, "Low-capacitance and charge-shared match lines for low-energy high-performance TCAMs," submitted to IEEE Journal of Solid-State Circuits.
9. N. Mohan, W. Fung, D. Wright, and M. Sachdev, "A ternary CAM with positive- feedback match line sense amplifiers and a match-token priority encoding scheme," submitted to IEEE Journal of Solid-State Circuits.
10. D. Wright, N. Mohan, and M. Sachdev, "A comprehensive test method for TCAMs," submitted to IEEE Design and Test of Computers.
11. Yen-Jen Chang, Kun-Lin Tsai, and Hsiang-Jen Tsai, "Low Leakage TCAM for IP Lookup Using Two-Side Self-Gating," IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 60, no. 6, pp. 1478-1486, June 2013.
12. Yu-Cheng Cheng, Jin-Hao Chen, Tung-Chi Wu, and Yen-Jen Chang, "Low Leakage Mask Vertical Control TCAM for Network Router," in Proc. IEEE Asia Pacific Conference on Circuits and Systems (APCCAS), Oct. 2016, pp. 469-472.
13. Weiqiang Zhang, Linfeng Li, and Jianping Hu, "Design Techniques of P- Type CMOS Circuits for Gate-Leakage Reduction in Deep Sub-micron ICs," in Proc. IEEE 52nd International Midwest Symposium on Circuits and Systems (MWSCAS), Aug. 2009, pp. 551-554.



**Impact Factor:
7.569**



INTERNATIONAL JOURNAL OF INNOVATIVE RESEARCH

IN SCIENCE | ENGINEERING | TECHNOLOGY

 **9940 572 462**  **6381 907 438**  **ijirset@gmail.com**



www.ijirset.com

Scan to save the contact details