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# An Efficient 2D-DCT/IDCT Architecture for Portable HEVC- Encoding

AN.Ramalakshmi<sup>1</sup>, P.Sukumar<sup>2</sup>

PG Scholar, Department of Electronics and Communication Engineering, Nandha Engineering College,  
Tamil Nadu, India

Assistant Professor, Department of Electronics and Communication Engineering, Nandha Engineering College,  
Tamil Nadu, India

**ABSTRACT:** Low power hardware acceleration cores for integration into period High potency Video secret writing (HEVC) codec for good phones, tablets, camcorders, and televisions square measure in nice demand. This want motivates one for AN economical realization of separate circular function remodel (DCT) and Inverse-DCT (IDCT) for HEVC. This paper presents AN rule to calculate the desired minimum variety of low frequency DCT-output/IDCT-input coefficients for four, 8, 16, and 32-point DCT/IDCT in HEVC, such there's a small decrease in peak-signal-to-noise-ratio (< zero.15 decibel) and a minor increment in bit rate (< one.5%) as compared to the reference HEVC-Test-Model (HM) computer code. However, the cryptography time gets reduced at the most by seventeen.95% for sophistication a sort sequences, whereas news mean-squared-error and structural-similarity of one.42 and 0.9913, severally for 4K ultra-high-definition videos. Moreover, HEVC-compliant computationally economical architectures square measure introduced for n purpose DCT/IDCT. The conferred versatile Transpose Memory design uses solely sixteen random-access-memories to support all transform-unit sizes in HEVC. The projected two-dimensional DCT/IDCT design will method up to 288@4K frames-per-second, and it consumes the minimum power, energy, and space of zero.011 mill watts, and 1.0 kilo-gate-equivalents, severally. Such style with low power, area, and energy options may be enclosed in an exceedingly period HEVC codec for HEVC-compliant client electronic devices.

**KEYWORDS:** HEVC, DCT/IDCT, low power

## I. INTRODUCTION

Over the past twenty years, there has been a dramatic increase in developing extremely economical video committal to writing to support accessible and future communication systems. The non-guaranteed quality of service in real time video delivery presents a difficult task for each domain and business sectors. Therefore, error resilience approaches at video committal to writing layer may be a major space of interest inside the sphere of video communication systems. In fact, the rise in video committal to writing potency comes at the price of accelerating put down prediction and motion compensation processes. These chiefly concerned in increasing the quantity of temporal redundant info. additionally to the high necessities of computation complexness, a extremely compressed bit stream suggests that a lot of redundant video info encoded. As a result, compressed video content becomes additional sensitive to channel bit errors. As a result, transmittal a extremely compressed video bit stream in unreliable transmission ends up in degradation of the perceived decoded visual quality or failure within the coding Process for the entire video sequence if errors hit the sensitive encoded information like slice header .demonstrates a video

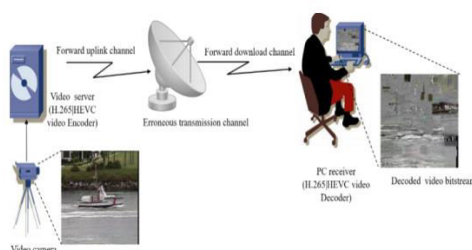


Figure: video transmission issue scenario



of affairs There are 2 main error management classes to scale back the consequences of transmission errors on perceived visual quality. The primary one employs ancient information error management strategies that use lossless channel secret writing tools in information recovery like ARQ error management schemes. However, implementing such error recovery tools in compressed video delivery is a smaller amount economical as a result of the character of the compressed bit stream is of a variable length code, that makes error recovery of decoded video contents a terribly difficult task. To attenuate the consequences of the transmission errors expeditiously at the video decoder facet, the video error management is divided into 3 approaches; forward error recovery, error concealment, and interactive error recovery approaches. In forward error recovery approach, the video encoder takes the complete responsibilities to insert redundant error resilience codes and makes the coded bit stream additional strong against errors. The second approach is error concealment techniques during which the decoder is accountable to hide the errors spatially and temporally. The spatial error concealment employs properly received data mistreatment interpolation techniques on the encircled macro blocks. Or just in case of complete macro block data is lost; simplest and commonest concealment techniques are substitution of the lost macro blocks with its same location.

## II. LITERATURE SURVEY

Gary J. Sullivan [2021] introduces H.264/AVC video coding standard. The main goal is to enhance compression, performance. The advantage of this paper is that it explains the standardization process. The disadvantage of this paper is that the desired efficiency of video compression couldn't be achieved to that extent.

Yunqing Ye and Shuying Cheng [2020] Implement 2D-DCT Based on FPGA with Verilog HDL Discrete Cosine Transform is (widely used in image compression. This paper describes the FPGA implementation of a two-dimensional (8x8) point Discrete Cosine Transform (8x8 point 2D-DCT) processor with Verilog HDL for application of image processing. The row-column decomposition algorithm and pipelining are used to produce the high quality circuit design with the max clock frequency of 318MHz when implemented in a Xilinx VIRTEX-IIPRO FPGA chip.

AnasHatim, S.Belkouch (2019) Efficient hardware architecture for direct 2D DCT computation and its FPGA Implementation In this paper, we propose a low complexity architecture for direct 2D-DCT computation. The architecture will transform the (pixels from spatial to spectral domain with the required quality constraints of the compression standards. In our previous works we introduced a new fast 2D DCT with low computations: only 40 additions are used and no multiplications are needed. Based on that algorithm we developed in this work a new architecture to achieve the computations of the 2D DCT directly without using any transposition memory. We defined Sk functions blocks to build the 2D DCT architecture. The Sk block performs 8 functions depending on the control signals of the system. The number of additions/subtractions used is 63, but no multiplication or memory transposition is needed. The architecture is suitable for usage with statistical rules to predict the zero quantized coefficients, which can considerably reduce the number of computations. We implemented the design using an FPGA Cyclone 3. The design can reach up to 244 MHz and uses 1188 logic components, and it respects the important time video needs.

AinyHaziyahAwab (2018) a comparison study has been performed for 2-D HEVC DCT for ASIC and FPGA implementations. The aim is to see appropriate architectures for these implementation platforms. Moreover, overall energy potency comparison between FPGAs and ASICs has additionally been determined. The study includes the planning and implementation of 2 unremarkably used 2-D DCT architectures that square measure the parallel and collapsible. 3 DCT sizes are designed and compared, that square measure the 4x4, 8x8, and 16x16. Results show that parallel design is best suited for ASIC because of an additional foreseeable instance placement and routing; whereas the considerably additional wiring in parallel design leads to comparatively poor performance in FPGAs. Results additionally show that mistreatment the Silterra 180nm technology achieves roughly 58x less energy compared to mistreatment the Xilinx

KintexUltrascale at 14nm technology. Future work is to finish the HEVC DCT for size 32x32 and 4x4 DST. Min Chen(2017) resented a style of two-dimensional (2D) separate circular function remodel (DCT) hardware design dedicated for prime potency Video cryptography (HEVC) in field programmable gate array (FPGA) platforms. The projected methodology with efficiency precedes 2D-DCT computation to suit internal elements and characteristics of FPGA resources. A four-stage circuit design is developed to implement the projected methodology. This design supports variable size of DCT computation, together with four x four, 8 x 8, 16 x 16, and thirty two x thirty two. The projected design has been enforced in System Verilog and synthesized in varied FPGA platforms. Compared with existing connected works in literature, this projected design demonstrates vital benefits in hardware price and

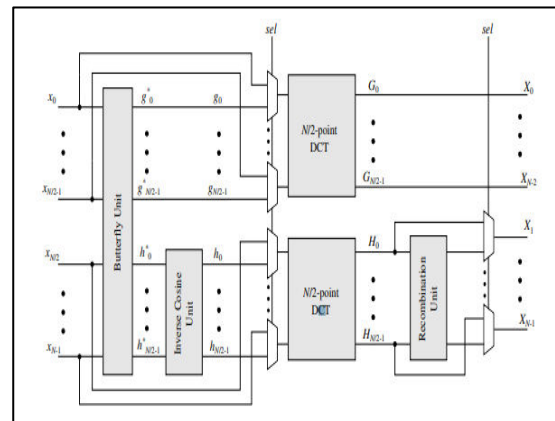
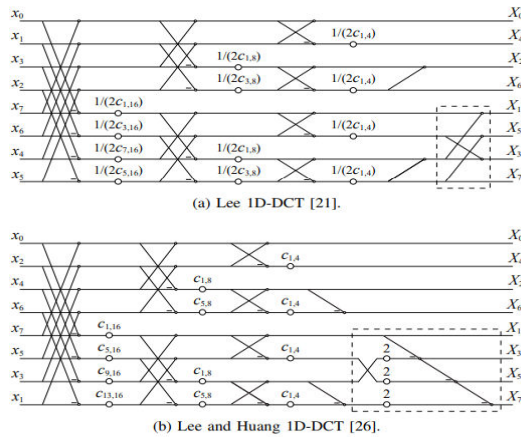




performance improvement. The projected design is in a position to sustain four K@30 Federal Protective Service extremist high definition (UHD) TV period encryption applications with a discount of 31–64% in hardware price. Ashfaq Ahmed (2012) bestowed a versatile VLSI design to figure the 4-point DCT. Since HEVC supports totally different block sizes for the computation of the DCT, that's 4x4, up to 32x32, the planning of a versatile design to support them helps reducing the realm overhead of hardware implementations. The hardware projected during this work is part collapsible to avoid wasting space and to induce speed for giant video sequences sizes. The projected design depends on the decomposition of the DCT matrices into thin sub matrices so as to scale back the multiplications. Finally, multiplications square measure utterly eliminated mistreatment the lifting scheme. The planned design sustains data processing of 1080P HD video codec running at one hundred fifty megacycle per second

III.EXISTING SYSTEM

The diagram of the planned design for structure decomposition.it's divided into J stages, and every stage consists of serial letter of the alphabet followed by a bit-reordering circuit. The design is analogous to serial electric switch FFT. The riffle butterfly of the SFG is mapped to the planned design as serial letter of the alphabet that takes knowledge serially and computes the coefficients at each stage. The bit rearrangement circuit reorders the intermediate coefficients starting up serially from PEs.Finally, riffle coefficients ar obtained serially at the Jth stage. The lifting theme was introduced by Swelden. it's AN economical methodology for computing DWT/DWPT. Consistent with, any variety of FIR riffle filter is factored into a sequence of lifting steps. The lifting-based riffle filter is that the planned riffle filter that computes riffle coefficients for serial knowledge.One-dimensional N-point DCT and two-dimensional DCT on top of the  $N \times N$  block ar said as 1D-DCT and 2D-DCT, severally. Solutions enforced in [6] for 1D-DCT ar fixed-point structures that believe the work of Cen et al. That is, resolution 1D-DCT for the layer of Walsh Hatmart remodel (WHT) and Givens cycles. On the opposite hand, handle the number DCT approximation outlined within the HEVC normal. Bookwright et al. [8] Propose AN integrated forward and reverse transformation unit exploitation symmetry at intervals the HEVC normal outlined transformation. Mehr et al. Presents AN economical number DCT design within which the 1D-DCT hub implements the partial-butterfly constant suggested by a  $N / \text{two}$ -point DCT and a  $N / \text{two} \times N / 2$  matrix multiplier factor by multiple constant [3]. Multiplication (MCM) technique. Zhao et al. Reduced the hardware price of the planning by exploitation add-ons and conversion functions to represent number DCD coefficients.



Dias et al. Use the systolic-sequence-based style to propose a multi-standard framework that supports each H.264 / AVC and HEVC number DCTs. The DCT design ought to support multiple transformation scales (i.e.  $N = 4, 8, 16, 32$ ) and aim to scale back hardware prices victimization resource allocation, with a outline review of the precise coefficients and number approximations projected within the literature for 1D-DCT

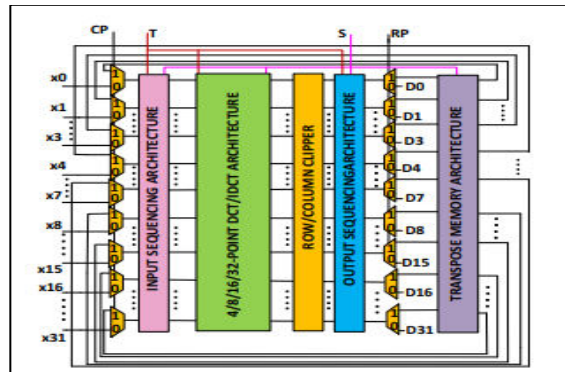


Fig.1 Existing variable-size 1D-DCT architecture for N = 8, 16 and 32.

The projected design for computing DWPT coefficients of a 3-level 8-point 6-bit. The DWPT coefficients for various levels are computed in many stages. At every level, wave coefficients are computed with the assistance of the projected wave filter and reordered to create subbands.

#### IV. PROJECTED SYSTEM

The projected 2nd 4-/8-/16-/32-point DCT/IDCT design. It needs only 1 DCT/IDCT module to reckon 2nd DCT/IDCT for all TU sizes whereas compared to 2 DCT processors as bestowed within the progressive styles. The DCT/IDCT processor generates thirty two DCT/IDCT coefficients counting on the choose lines (S and T) of MUXes. The lines ‘S’ and ‘T’ permit the design to pick out the dimensions (4-/8-/16-/32-point) and sort (DCT/IDCT) of the rework, severally. This convention is additionally followed within the Input and Output sequencing architectures. The choose lines (CP and RP) of MUXes and DEMUXes permit the 2nd design to perform column and row process of the input samples as pictured. Min Num rework Coeff, to calculate . Here, represents the minimum needed variety of DCT-output/IDCT-input coefficients to reckon n-point DCT/IDCT for the Transform-and-Quantization (TQ) block of HEVC,

Here,  $h_{an}$  and  $b_{min}$  represent the most PSNR and minimum bitrate rumored by metric linear unit software package [30] for a video sequence (I) regarding the initial reference formula [1], i.e.,  $X_n = X_{max}$ . Moreover,  $P_{av}$  and  $R_{av}$  represent the common values of PSNR and bitrate, severally. Here,  $f_P(X_n)$  and  $f_R(X_n)$  represent the values of PSNR and bitrate, severally calculated for n-point DCT/IDCT at  $X = X_n$  by metric linear unit software package [30]. The reference quantisation parameters (QP) thought of for the present formulas within the algorithm, the amount of DCT-output/IDCT-input coefficients (X) needed for n-point DCT/IDCT area unit varied at the same time within the vary of  $X_{max}$  to  $X_{min}$  in metric linear unit software package [30]. whereas calculative the PSNR and bitrate for 32-point DCT/IDCT, the values of  $X_{max}$  and  $X_{min}$  area unit thought of to be thirty two and 0, severally.

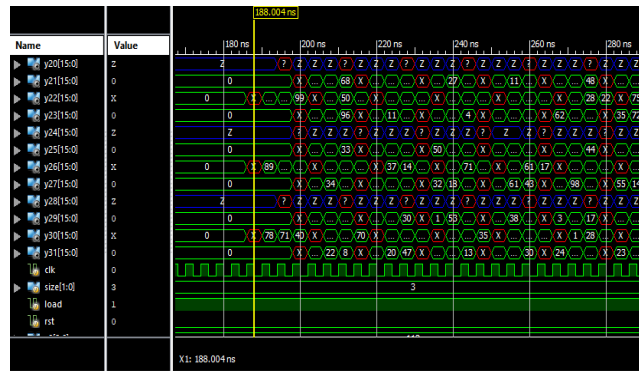
#### V. RESULT AND SNAPSHOTS

The planned second 4-/8-/16-/32-point DCT/IDCT design as given in Fig. eleven will calculate second DCT/IDCT for all the TU sizes as mentioned within the HEVC commonplace [1]. It conjointly includes MCM formula and clock gating to cypher the second DCT/IDCT output coefficients. Hardware implementation of the planned architectures is administered in Verilog lipoprotein. Moreover, RTL implementation result matches thereupon of the HEVC metric linear unit software package [30]. For example validation of the planned second DCT/IDCT hardware, the planning is enforced AND tested on an FPGA in ninety nm CMOS technology.

Table IV shows the FPGA implementation results of the planned second 4-/8-/16-/32-point DCT/IDCT design. The planned second style reports important reduction (>50%) in FPGA resource utilization and Block RAMs (BRAMs) whereas compared to the separate implementation of original DCT and IDCT modules [26]. For implementation on ASIC platform, the Verilog codes of the planned architectures are synthesized by employing a ninety nm commonplace digital cell library. Moreover, ASIC implementation results of the planned 1D and second DCT/IDCT architectures for



HEVC area unit shown in Table V. Here, the facility and space area unit calculable at a frequency constraint of one hundred forty five Mc.



The hardware implementation of the projected 2nd 4-/8-/16-/32-point DCT/IDCT design needs solely sixteen twin port RAMs of size sixty four × sixteen bits every and reports most operational frequency of 149.35 MHz, power dissipation of eleven.23 mW, space of a hundred and twenty kGates (Logic+16-SRAMs area), and energy-peroutput-coefficient (EoC) of two.34 pJ. moreover,

Table VI shows that the projected 2nd DCT/IDCT style reports seventy eight reduction in space consumption whereas compared to the separate implementation of DCT and IDCT modules [26]. Therefore, the projected style are often integrated into a time period HEVC codec for moveable metal devices. Comparison of hardware of the projected 2nd 4-/8-/16-/32-point DCT/IDCT design as bestowed in Table VII indicate that the projected style reports low power and smaller space as compared to the architectures. Moreover, the architectures will perform solely forward DCT and need a minimum of thirty two RAMs to perform 2nd remodel. Thus, these styles would force some extra hardware for playacting 2D-IDCT. The architectures will perform solely 1D remodel operation, and thus these styles would force extra hardware for implementation of 2nd remodel. The design has not been designed to perform 2nd IDCT. Therefore, it's slightly lower hardware consumption than the projected style during this work. not like the architectures bestowed within the state-of-the-art, the projected hardware during this work will work out 2nd DCT/IDCT operation for all TU sizes in HEVC at the minimum hardware consumption whereas supporting up to 288@4K frames-per-second. Min Num remodel Coeff, to calculate . Here, represents the minimum needed range of DCT-output/IDCT-input coefficients to work out n-point DCT/IDCT for the Transform-and-Quantization (TQ) block of HEVC, wherever n = four, 8, 16, and 32.

The algorithmic rule determines the quantity of minimum needed DCT output/IDCT-input low-frequency coefficients required for the calculation of n-point DCT/IDCT in HEVC-Test Model (HM) software system [30] in order that the decrease in PSNR (dB) and therefore the increment in bit rate (Mbps) is a smaller amount than zero.15dB and 1.5%, severally. once the algorithmic rule is extended to HEVC-test-Model (HM), it considerably decreases the procedure overhead of the reference algorithmic rule.

Therefore, the whole cryptography time of metric linear unit software system [30] gets reduced at the most by seventeen.95% for sophistication a kind video sequences. within the algorithmic rule, the edge for PSNR (Pth) and bitrate (Rth) ar taken solely zero.15 decibel less and one.015 times than and , severally.

S.No	parameter	ExistingMethod	ProposedMethod
1	Slice	365	64
2.	LuT	1084	1053
3.	Dff	854	989
4	FreQuencyin(MHz)	100.526	711.61
5	PowerinWatts	0.115	0.81



Here,  $h_n$  and  $b_n$  represent the utmost PSNR and minimum bitrate according by hectometre software package [30] for a video sequence (I) regarding the initial reference rule [1], i.e.,  $X_n = X_{max}$ . Moreover,  $P_{av}$  and  $R_{av}$  represent the typical values of PSNR and bitrate, severally. Here,  $f_P(X_n)$  and  $f_R(X_n)$  represent the values of PSNR and bitrate, severally calculated for n-point DCT/IDCT at  $X = X_n$  by hectometre software package [30]. The reference division parameters (QP) thought-about for the present rules within the algorithm, the amount of DCT-output/IDCT-input coefficients (X) needed for n-point DCT/IDCT area unit varied at the same time within the vary of  $X_{max}$  to  $X_{min}$  in hectometre software package [30].

```

Algorithm 1: Min_Num_Transform_Coeff
Input: I, PTH, RTH, Rmin, Pmax
Output: X4OPT, X8OPT, X16OPT, X32OPT
1 I ← Test Video Sequence;
2 Pth ← (Pmax - 0.15);
3 Rth ← 1.015 * Rmin;
4 Initialize Init =  $\lfloor \frac{P_{max}}{R_{min}} \rfloor$ , Var = 0;
/* Init, Var are data variables */
5 for (X4 = 4, X4 ≥ 0, X4 --) do
6   for (X8 = 8, X8 ≥ 0, X8 --) do
7     for (X16 = 16, X16 ≥ 0, X16 --) do
8       for (X32 = 32, X32 ≥ 0, X32 --) do
9         Pav ← Average{fP(X4), fP(X8),
10          fP(X16), fP(X32)};
11         Rav ← Average{fR(X4), fR(X8),
12          fR(X16), fR(X32)};
13         Var ←  $\lfloor \frac{P_{av}}{R_{av}} \rfloor$ ;
14         if (Var < Init && Pav ≥ PTH &&
15          Rav ≤ RTH) then
16           Init ← Var;
17           X4OPT ← X4;
18           X8OPT ← X8;
19           X16OPT ← X16;
20           X32OPT ← X32;
21         end
22       end
23     end
24   end
25 end
    
```

whereas conniving the PSNR and bitrate for 32-point DCT/IDCT, the values of  $X_{max}$  and  $X_{min}$  area unit thought-about to be thirty two and 0, severally. So, the amount of DCT-output/IDCT-input coefficients area unit varied at the same time from thirty two thirty two zero for 32-point DCT/IDCT. The remaining DCT-output/IDCT-input coefficients that aren't thought-about whereas computing n-point DCT/IDCT area unit created zero in hectometre software package [30]. whereas varied the coefficients from  $X_{max}$  to  $X_{min}$  for 32-point DCT/IDCT, the remaining algorithms of 4-, 8-, and 16-point DCT/IDCT area unit unbroken dateless. a similar technique is additionally followed whereas varied the coefficients for 4-, 8-, and 16-point DCT/IDCT. Because the input video sequences (I) area unit varied, it's determined that on a median the minimum range of needed DCT-output/IDCT-input coefficients for 4-, 8-, 16-, and 32-point DCT/IDCT area unit four, 3, 6, and 7, severally, i.e.,  $X_{4OPT} = 4$ ,  $X_{8OPT} = 3$ ,  $X_{16OPT} = 6$ , and  $X_{32OPT} = 7$ .

**VI.CONCLUSION**

The formula succeeds in decreasing the coding time at the most by seventeen.95% of hectometer code for sophistication a kind video sequences. whereas compared to the styles reportable within the progressive, the planned approximate whole number 1D 4-, 8-, 16-, 32-, and 4-/8-/16-/32-point DCT/IDCT architectures need comparatively fewer computations and change to the HEVC customary. The planned 2nd 4-/8-/16-/32- purpose DCT/IDCT design wants just one DCT/IDCT module to figure 2nd 4-/8-/16-/32-point DCT/IDCT and consumes lower energy (2.34 pJ), space (120 KGates), and power (11.23 mW) than those of the architectures reportable within the progressive. The planned 2nd DCT/IDCT design conforms to the realm and power necessities of a typical HEVC codec, and it's dowered with low energy, area, and power consumption. Thus, this featured style are often integrated in a very period of time HEVC codec for power restrained HEVC-compliant moveable metallic element devices like good phones, tablets, and camcorders.

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