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Low Power Multiplier Design using Hybrid Full Adder

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ABSTRACT: The multiplier factor is that the simplest unit of Associate in nursing arithmetic circuit that is preponderantly employed in digital process units and a number of other integrated circuits. The potency of a process unit is measured by its speed and power consumption. The multiplier factor circuit involves intensive use of adders that typically boost its hardware quality and this can be a significant defect for quick processes and additionally consumes high power. Therefore, it becomes essential to enhance speed and scale back power consumption within the multiplier factor module. The standard multipliers enforced mistreatment the CMOS and GDI technologies and their combination versions, still the improved speed and low power consumption suffer from high hardware quality. A style of, a hybrid Full Adder (FA) mistreatment Pass Transistors (PTs), Transmission Gates (TGs) and, standard Complementary Metal compound Semiconductor (CCMOS) logic is given. The FA was enforced in forty-five nm technology mistreatment tanner tools. In judge the responsibility, a comparative examination on performance parameters of the projected style has been conducted with twenty existing FA styles with provide voltage varied from 0.4 V to 1.2 V. Moreover, the FAs are extended to wide word length adders to check their performance parameters in massive scale large-scale

I. INTRODUCTION

As VLSI style engineers, we tend to as a society face 2 main issues: Power Dissipation and Propagation Delay. There square measure completely different technologies offered to assist U.S.A. style our circuits. However, each style technology has some limitations that can't be unnoticed. For instance, microprocessors, digital signal process, and image process use subtractions, additions, ANDs, and ORs. Most of the adders increase each the delay and power dissipation that may be a major drawback in digital signal process with reference to our turn, latency, and delay. Therefore, within the circuit, our main focus is to cut back the ability and delay. As VLSI circuit's square measure being developed and integrated into individual chips with higher performance, semiconductor unit intensities square measure of reduced, that not solely will increase the electrical consumption of the circuit however additionally will increase their quality. Nowadays era, one among the most important challenge is to style that kind of circuit provides which provides which supplies not solely the low power however additionally gives the high performance within the VLSI circuits and additionally the delay parameters will be minimized at the corresponded time. For that we will improve these 2 parameters to urge the suitable result. In Complementary Metal compound Semiconductor (CMOS) circuits, there are a unit 3 major enhancements through that we will consume the facility is mentioned below:- The active power because of charging and discharging of the circuit capacitance throughout change.

- Because of the discharge current, there's a discharge power within the circuit.
- There's a brief circuit current that moves from offer to GND wherever the P-Sub still
- N-Sub Network of Complementary Pass semiconductor device computer circuit charge at the same time.

Adiabatic Logic is one in all the foremost distinguished technique that plays a really important role for the facility consumption within the circuit. Adiabatic logic aims to decrease the facility within the logic circuit. Though there are a unit several techniques like pass semiconductor device logic United Nations agency helps to scale back the facility however adiabatic logic is one in all the foremost distinguished technique that is employed for the consumption of power. In VLSI, another most distinguished technique that is employed to scale back the facility i.e. Domino Logic. In terribly giant Scale Integration Circuit, performance plays a really essential role for the design of low power and high speed within the circuit. For division, multiplication still as exponential operations, full adder is one in all the essential block. In VLSI style circuits, hybrid logic is additionally accustomed scale back the facility and offers the high speed

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performance. It's the mixture of the Transmission Gate (TG) logic and C-CMOS (Complementary Metal compound Semiconductor) logic.

1.1 Objectives

To develop the performance of VLSI circuits the dimensions of the semiconductor device are reducing that result not solely within the circuit power consumption still because it develops the completeness of the chips. Nowadays amount, planning of the less power consumption and therefore the and high-speed accomplishment have become a significant issue within the VLSI circuits. Also, we've got to scale back the facility still delay within the circuit at the identical time. The increased utilization of natural philosophy equipment's has created power dissipation an important parameter within the fashionable natural philosophy. Electronic devices that employment for utilizing A battery has the restricted offer of the battery. Up until currently, power consumption in a very circuit wasn't the most significant issue as a result of cooling techniques has the capability of intense the created heat. Though because of unending developing intensity still because of the density of the chips within the system cause obstruction of providing the suitable cooling. Consequently, it adds applicable worth to the system. That's as a result of we'd like a circuit United Nations agency offers an occasional power consumption notwithstanding a various parts area unit unreal over one chip. To style and analyse the essential operations of GDI, RTL, Domino, and adiabatic Logic

- To scale back low power within the circuit
- To scale back the Propagation Delay within the circuit.
- To figure on the dimensions of the circuit.
- To check the projected style with different existing techniques.

1.2 Drawback Formulation

A VLSI style engineer is primarily involved with power dissipation and delay in a very circuit. during this work, we tend to projected one bit hybrid full adder circuit that possesses 2 techniques - Gate Diffusion Input (GDI) and Pass semiconductor device logic the planning state of affairs has altered considerably within the previous couple of decades and adders, that area unit thought-about to be the core of the many applications like Arithmetic Logic Units, Digital Signal process, and Microprocessors, are underneath scrutiny. Observant that each the Gate diffusion technique and therefore the Pass semiconductor device Logic have identical drawback is that the low swing output as a result of each don't use a voltage supply.

II. LITERATURE SURVEY

2.1 space and Power economical Carry choose Adder mistreatment 8T Full Adder B. Sathyabhama, M. Deepika, and S. Deepthi, 2020 during this paper 8T full adder is employed as a building block for 8-bit SQRT CSLA. 8T full adder by XNOR hybrid CMOS design. To perform quick arithmetic operations, carry choose adder is one in all the quickest adders that is employed for the process of knowledge complicated.. The SQRT CSLA consists of 8T XNOR full adder. By mistreatment the Pass semiconductor device Logic, 8T XNOR full adder is performed. SQRT CSLA is built by equalizing the delay through 2 carry chains. to attain low power consumption 8T FA is employed because the building block for ripple carry adder. A hybrid CMOS full adder with 8T is built by mistreatment 3T XNOR circuit. Since XNOR consists of three transistors solely. The 3T XNOR circuit. This 3T XNOR is meant mistreatment pass semiconductor device logic (PTL). It's an extremely compact style. XNOR operation is performed double in 8T full adder and by mistreatment electronic device, total and carry were determined. The key issue for top speed style is that the range of P-transistors ought to be but N-transistor.

2. A Competent style of two:1 electronic device and Its Application in 1-Bit Full Adder Cell Amit Dubey Sachin DubeyShyamAkashe, 2020In this paper, Associate in Nursing design of 2:1 electronic device has been projected. As we all know that multiplier factor is additionally called MUX. In terms of consumption of power, temperature, delay and cargo capacitance of output, MDCVSL offers the great result by the addition of double weak P channel. In terms of delay, consumption of power and cargo capacitance of output the changed electronic device of DCVSL 2:1 offers the higher result. Within the MDCVSL, the association of six NMOS and therefore the four PMOS is finished and single addition of offer is used on the circuit for change. VPULSE is connected on each input port out of six input on that we discover out the autumn time, rise time, voltages V1 and V2, fundamental measure and breadth of pulse and Z and Zb is connected at the 2 output port and at the bottom port GND is connected within the circuit.

3. 1-Bit Hybrid Full Adder by GDI and PTL Technique KshitijShant, Rita Mahajan, 2020 during this paper one bit full adder hybrid circuit has been projected that encompass 2 techniques i.e. Pass semiconductor device Logic AND gate

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Diffusion Technique. One bit full adder cell is meant to represent the potency of the projected design. For the planning of low power the strategy (GDI and PTL) is employed, the standard complication in PTL and GDI technique is that the swing output is a smaller amount as a result of the Vdc isn't enclosed within the Gate Diffusion Input still because the Pass semiconductor device Logic. Last of Power dissipation and delay it analyzed that the performed information of adder of hybrid is varies in between the PTL and therefore the GDI. On increasing the provision voltage of input, the characteristics of hybrid adder conjointly changes. Because of the deficiency of voltage supply (Vdc), the GDI and PTL don't turn out the output of full swing. On increasing the provision voltage of input (Vp) additional voltages is needed for the transmission from input to output through that the opposite transistors will simply dead.

4. Analysis of Full Adder mistreatment adiabatic Charge Recovery Logic Amalin docking facility, S ShunbagaPradeepa T, Dr. A Rajeswari, 2019 This paper shows the correlative study of full adder utilizing numerous adiabatic logic designs. Power analysis is dead at 45nm for numerous frequencies and output represents that at less frequencies economical Charge Recovery Logic (ECRL) absorbs sixty nine minimum power as compared it with the standard CMOS logic style whereas at higher frequencies the facility consumption of Secured-Quasi adiabatic logic possess seventy one.8% lesser as compare it with the CMOS. SQAL is that the advancement over ECRL. Analysis represents that the ECRL is capable at less frequencies still because it represents minimum in power of sixty eight compared with CMOS whereas SQAL is a lot of capable at most frequencies and it represents the decrease in power of 71% in comparison with standard CMOS logic vogue.

5.Changed feedback adiabatic Logic for extremist Low Power Adder knife Pratap Singh Kushawaha, TrailokyaNathSasamal, 2018 This paper suggest changed feedback adiabatic Logic (MPFAL) that is utilized for ultralow-power circuits. MPFAL depends on positive DC voltage starting from 0.1V-0.3V. [*fr1] Adder and 1-bit full adder consolidate this system used for the low power circuits. once compared between these 2 techniques, we tend to over that the common power is decreased just in case of changed feedback Adder as compared to the feedback adiabatic Logic All the simulations area unit dead in Cadence Virtuoso Tool utilizing UMC 180nm CMOS Technology. This system may be used in ultra-low-power digital circuits dead in most frequencies.

III. EXISTING WORK

3.1Existing Full Adder style Approach The style of the present FA is split into four major modules: 2 modules for carry generation and also the different 2 for total. Schematic of the present style is diagrammatic by Fig. 2. The look strategies and careful description of the modules as provided within the following subsections. Style approach of the present FA is shown in Fig. 1..



Fig. 1.Diagram of existing full adder.

Carry Generation From the reality table of a FA, it may be ascertained that

If, $C_{in} = 0$ then $C_{out} = AND$ function and if, $C_{in} = 1$ then $C_{out} = OR$ function

Therefore, the projected carry generation half consists of a completely unique AND-OR module (module 1) supported TG and CPL logic. Among the AND-OR module, implementation of AND and OR gates as quite similar, except the actual fact that nMOS and pMOS transistors as interchanged. The conditions needed to style the projected AND circuit as follows:

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If $A = 0$, then $output = 0$ and	(1)
If $A = 1$, then $output = B$	(2)

The first condition for AND circuit style in (1) is administrated by the pass semiconductor device N2 and TG1, severally. The later condition (2) is administrated by TG1. Within the same manner, conditions for planning gate are:

If $A = 1$, then $output = 1$ and	(3)
If $A = 0$, then $output = B$	(4)

Here, conditions (3) and (4) as administrated by pass semiconductor device P2 and TG2, severally. A TG primarily based 2:1 MUX (module 2: consists of TG3 and TG4) is employed to pick out the acceptable carry-out signal from the AND-OR module looking on input carry Cin.

Schematic of the present FA Total Generation The total output of the projected FA is generated by cascading 2 XOR modules (modules three and 4). The XOR gates have precisely the same structure and as enforced victimization TGs and PTs. The conditions for planning the XOR gate for module three are:

If $A = 0$, then $output = B$	(5)
If $A = 1$ and $B = 0$, then $output = A$	(6)
If $A = 1$ and $B = 1$, then $output = \overline{A}$	(7)

In this case, condition (5) has been enforced victimization TG5. The pass semiconductor P3 in module three (XOR gate) implements condition (6) and also the pass transistor N3 implements condition (7). Using precisely the same methodology, XOR gate for module four has been designed victimization C in and $A \oplus B$ (output of module 3) as inputs. For this case, the conditions are:

If $C_{in} = 0$, then $output = A \oplus B$	(8)
If $C_{in} = 1$ and $A \oplus B = 0$, then $output = C_{in}$	(9)
If $C_{in} = 1$ and $A \oplus B = 1$, then $output = \overline{C_{in}}$	(10)

In this case, the conditions (8), (9) and (10) are enforced by TG6, P4 and N4, severally, to investigate numerous performance parameters, simulation has been conducted in GPDK forty-five nm technology node victimization Tanner simulation tools. Buffers as additional within the input and output facet for simulation take a look at bench. The output facet additionally consisted a load capacitance of six ff. during this manner, the circuit experiences vital signal distortion in contrast to realistic atmosphere. Input frequency has been set to one hundred rate. For optimized semiconductor device size, particle swarm optimization algorithmic program has been utilized for implementation of FAs. For semiconductor device size victimization swarm algorithmic program, we have a tendency to initialize a vector wherever m is that the semiconductor device count and n is that the variety of particles. Every particle has three styles of movement tendency within the search space: (a) tendency because of its own inertia (b) tendency towards particle's best price (c) tendency towards team's best price. The circuit is simulated by arbitrarily dynamical semiconductor device dimension among to vary of minimum to most allowable size. the target is minimum Power Delay Product (PDP). If a particle's current PDP < best PDP price to this point found by that particle, then the present PDP is about because the particle's best PDP. Within the same manner, if the most effective PDP for current simulation run < the most effective PDP price to this point found within the entire search area, then the team's best price is updated with the present price. During this manner, once finishing the required variety of iterations, the team's best price of PDP is chosen because the best PDP and also the corresponding semiconductor device widths as chosen for circuit implementation.

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IV. PROPOSED WORK

The computing speed of contemporary electronic devices is directly associated with the semiconductor space and power dissipation of the device, however the layout footprint is reciprocally proportional to the semiconductor space. Consequently, circuit designers as needed to form trade-offs to satisfy the system's demands. Arithmetic blocks play a vital role in digital microprocessors, however consume an oversized quantity of power. Several digital arithmetic applications bank heavily on the effective style of arithmetic circuits, since they generate hot spots in microprocessors. Arithmetic circuits as usually the causes of hot spots in a very silicon chip and should be taken into thought throughout circuit style.



Block Diagram Of Proposed Hybrid Full adder Design

V. OUTPUT RESULTS

5.3.1 Exiting method 5.3.1.1 Simulation Output wave form



5.3.1.2 Power report

Power Results

```
V1 from time 0 to 1e-007
Average power consumed -> 1.037762e-005 watts
Max power 4.401043e+000 at time 8.0002e-008
Min power 1.065372e-009 at time 2e-012
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5.4. Comparison results

S.No	Parameters	Existing hybrid Full Adder Design	Proposed hybrid Full Adder Design
1	Average Power in Watts	1.037e-005	4.46e-005
2	Delay in ns	2.25	3.58
3.	Transistor Count	22	20

VI. CONCLUSION

Using Tanner style and simulation tools, we tend to implement a hybrid full-swing FA style supported by the XOR-XNOR module. It's been shown that a planned FA exhibits thirty-three percent and twelve percent system improvement in Propagation Delay as compared with the traditional CCMOS FA. The measurability of existing and planned FA styles in wide word-length design has been investigated by extending the styles to 4-bits. In an exceedingly 32-bit configuration, the average power is improved by twenty-two percent, propagation delay by thirty-one, and performance is increased by eight.58% over the CCMOS FA. The simulation-based analysis conducted during this work proves that the planned FA style is very appropriate for contemporary superior VLSI arithmetic block styles. As a future scope of this work, the result of mistreatment of the planned FA in different arithmetic blocks like multiplication, subtraction, magnitude comparison are often analyzed.

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