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Study of Successive Approximation Register and Charge Redistribution Digital to Analog Converter

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ABSTRACT: In this paper, an overview of SAR ADC has been demonstrated. This work has been carried out based on some parameters like power dissipation, on-chip area, and accuracy, etc. Principally the overall performance of SAR ADC depends on the Capacitive Digital to Analog Converter (CDAC) block, so the optimal design of 14-bit differential SAR ADC demands the accurate design of the CDAC model. Types of CDAC has been discussed with their advantages and disadvantages. An end to end the comparative study of both the conventional CDAC and the split CDAC has been carried out with their advantages and disadvantages in this exercise.

KEYWORDS: - SAR, ADC, DAC,

I. INTRODUCTION

The ADC and DAC developed by Alec Harley Reeves represent one of the first all-electronic data converters. From fig 1, the ADC technique uses sampling pulses to take a sample of the analog signal, set an S/R F.F. (flip-flop), and then simultaneously start a controlled ramp voltage. The ramp voltage is compared with the sampled input, and when they are equal, a pulse is generated that resets the S/R flip-flop. The flip-flop outputs are a pulse waveform whose width is proportional to the analog signal at the sampling instant. This pulse-width modulated (PWM) pulse controls a gated oscillator, and the number of pulses out of the gated oscillator represents the quantized value of the analog signal. This pulse train can be easily converted to a binary word by driving a counter. In Reeve's system, a master clock of 600 kHz is used, and a 100:1 divider generates the 6-kHz sampling pulses. The system uses a 5-bit counter and 31 counts (out of the 100 counts between sampling pulses) therefore represents a full-scale signal. [1].

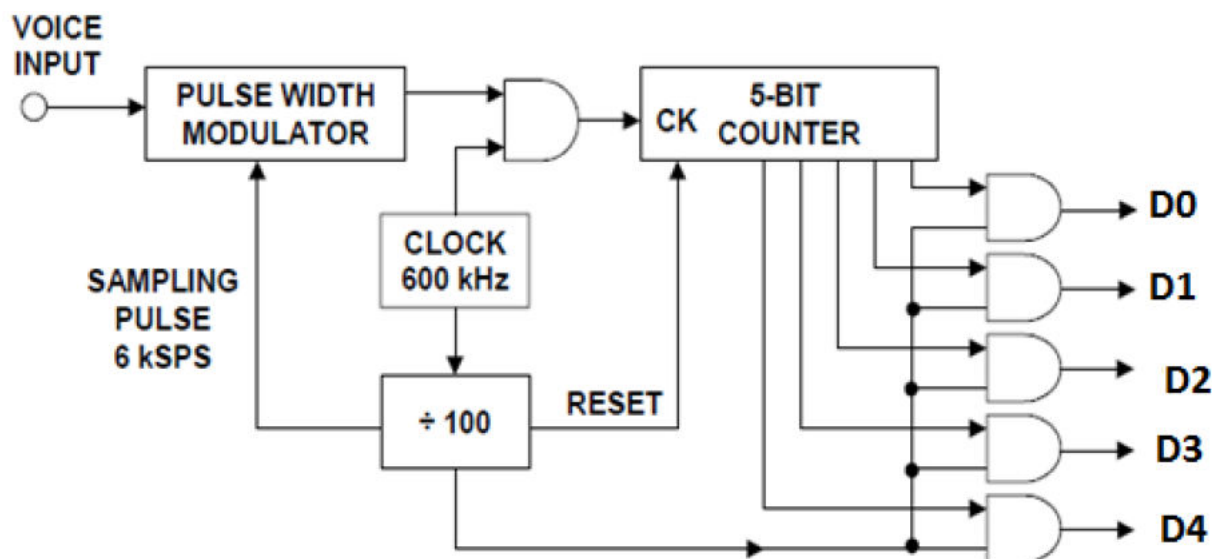


Figure 1: 5-bit counting ADC

The DAC uses a similar counter and clock source, as shown in Figure 2. The received binary code is first loaded into the counter, and the S/R flip-flop is reset. The counter is then allowed to count upward by applying the clock pulses. When the counter overflows and reaches 00000, the clock source is disconnected, and the S/R flip-flop is set. The number of pulses counted by the encoding counter is thus the complement of the incoming data word. The S/R flip-flop's output is a PWM signal whose analog value is the complement of the input binary word. Reeves uses a simple lowpass filter to recover the analog signal from the PWM output. The phase inversion in the DAC is easily corrected in either the logic or in an amplifier further down the signal chain.

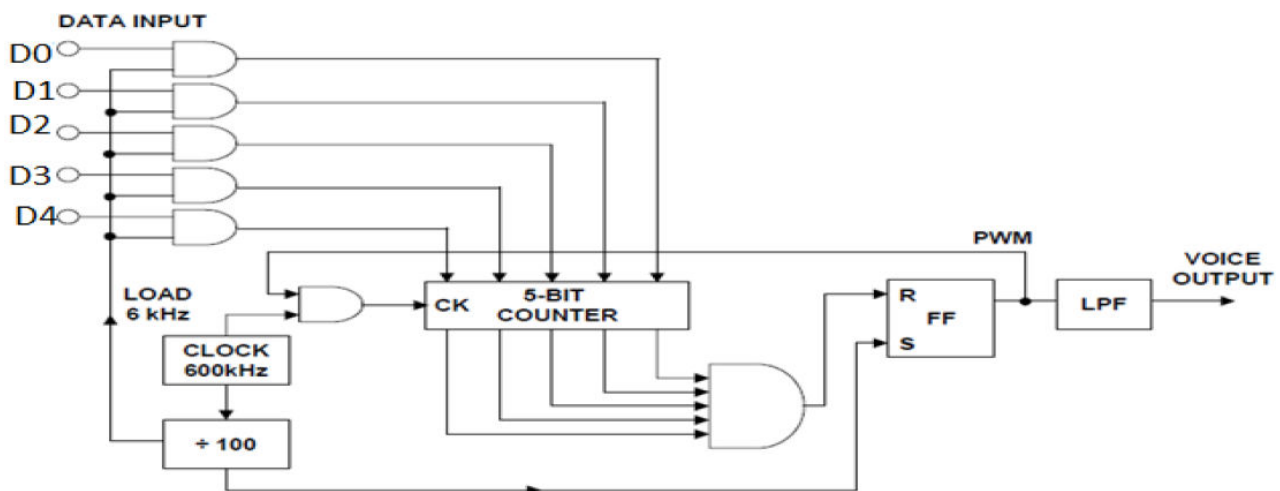


Figure 2: 5-bit counting DAC

II. SUCCESSIVE APPROXIMATION CONVERTER

To understand the successive approximation converter, firstly, we have to know about its working algorithm. SAR ADC is working on a binary search algorithm, which has been explained below by assuming simple weigh scale topology.

The balance scale topology is the best example of the binary search algorithm. Let us assume the value of $X = 45$, which has been put on one side of the weighing machine and the other side for testing. Now take 32 for the test (randomly selected value), and the whole conversion is explaining in figure 3.

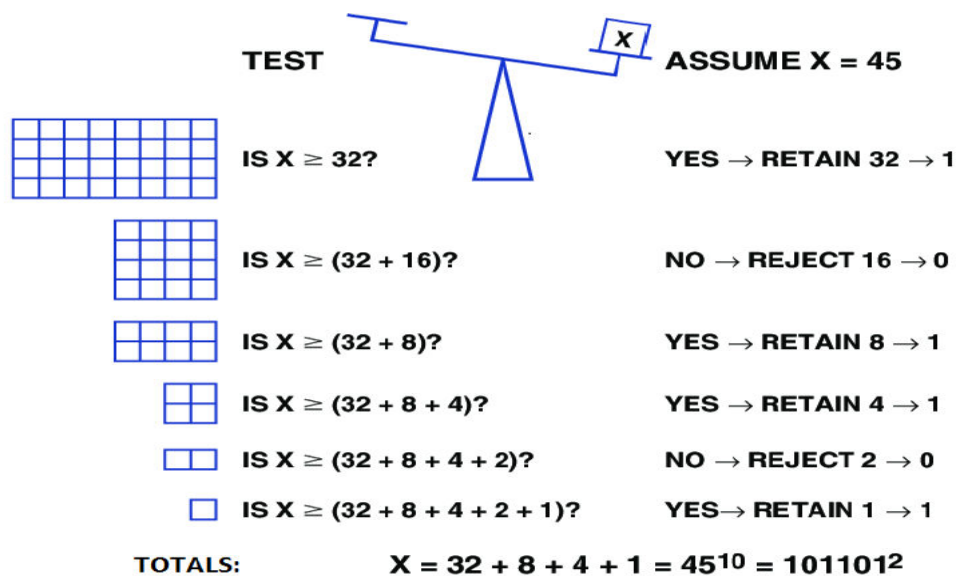


Figure 3: Weigh scale topology [3]

So, based on the above discussion, we can better understand the working principle of SAR ADC. The SAR ADC uses a binary search algorithm similar to that shown in figure 4 to perform an A/D conversion. Since only one bit is converted at a time, the device's complexity and power consumption can be reduced at the reduced conversion rate. The time required for an n-bit conversion is (n+1) clock cycles, an additional one clock cycle is needed for sampling the input signal before the actual conversion occurs.

In order to investigate the effective operation of the SAR ADC, consider a 4 bit ADC. As shown in Figure 3.3, in the first clock cycle sampling would take place, then after a second clock cycle DAC voltage is set to half of V_{ref} (according to the binary search algorithm) by setting the code to 1000, the input voltage is compared to $V_{ref}/2$ and based on the comparison result, MSB is defined. If $V_{S\&H} > V_{ref}/2$, the MSB will not be changed and will remain at one; otherwise, the MSB is reset to zero. So in figure MSB (Bit3) remains at one. In the next clock cycle, the DAC input is set to 1100, and again $V_{S\&H}$ is compared to $3V_{ref}/4$. Bit2 rejects its value since $V_{S\&H} < 3V_{ref}/4$. For the next bit, the DAC input is set to 1010. Based on the comparison, Bit1 is retained its value to one since $V_{S\&H} > 3V_{ref}/4$, and finally, for defining LSB, the DAC input is set to 1011. Bit0 is one because $V_{S\&H} > 13V_{ref}/16$. Therefore, the analog input is converted to the digital code 1011 in four clock cycles.

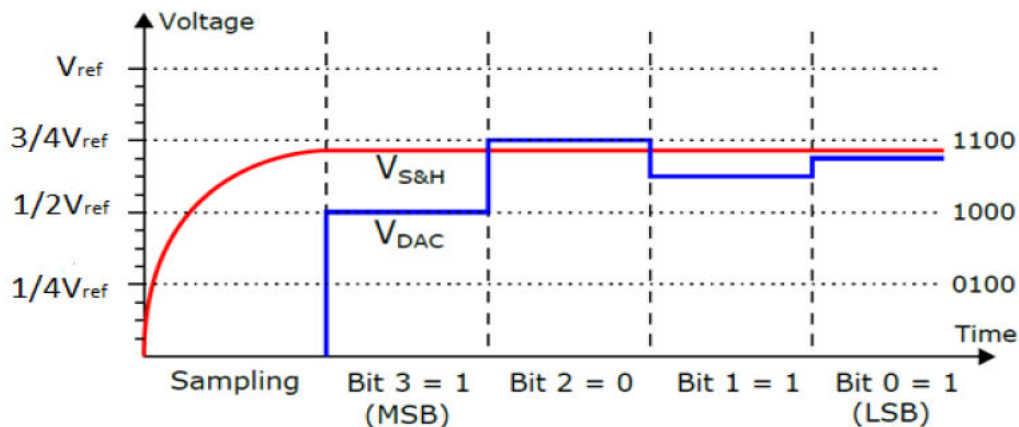


Figure 4: Binary search algorithm of SAR ADC

III. SUCCESSIVE APPROXIMATION REGISTER (SAR) LOGIC

Successive Approximation Register (SAR) control logic determines each digital bit successively. The successive approximation register contains N bit for an N-bit ADC. There are three possibilities for each bit; it can be set to '1', reset to '0', or keeps its value.

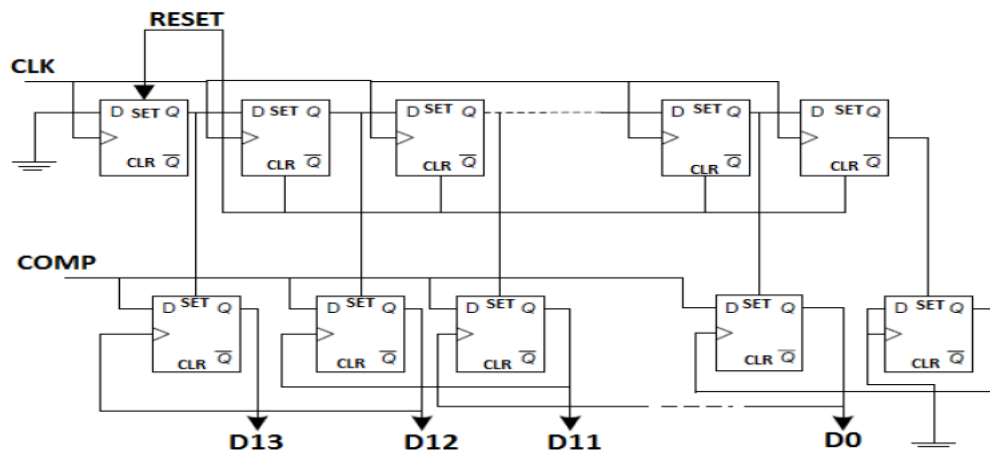


Figure 5: SAR logic circuit with D F/F

In the first step, MSB value is set to '1,' and other bits are reset to '0', the digital word is converted to the analog value through DAC. The analog signal at the DAC's output and the sampled analog input both are the input of the comparator. Based on the comparator result, the SAR controller determines the MSB value of the SAR logic. If the sampled input is higher than the DAC's output, the MSB remains at '1'. Otherwise, it is reset to '0'. The rest of the bits are determined in the same manner. In the last cycle, the converted digital word is stored. Therefore, an N-bit SAR ADC takes N+1 clock cycles to perform a conversion.

Figure 5 shows that the 14-bit SAR logic, which has been implemented by D-F/F. It is used in SARs ADC due to its straight forward design technique. This control Logic encompasses a ring counter and a code register.

For each conversion, in clock cycle 0, the end of conversion (EOC) signal is high, and all Flip Flops outputs are reset to zero, and for the rest of cycles, EOC is low. In the next clock cycle, the most significant Flip Flop is set to one which corresponds to MSB of the digital word to the DAC. Then the counter shifts '1' through the Flip Flops from MSB to LSB. In each clock cycle, one of the outputs in the ring counter sets a

Flip-Flop (F/F) in the code register. The Flip Flop's output, which is set by the ring counter, is used as the clock signal for the previous Flip Flop. At the rising edge of the clock, this Flip Flop loads the result from the comparator. At the end of each conversion, the EOC signal turns to high. This type of SAR logic converts each sample in 16 clock cycles.

Consider the above designed for 14-bit SAR ADC, then the number of D-F/F is more so the delay incorporated by its flip-flops is more.

IV. CHARGE REDISTRIBUTION DIGITAL TO ANALOG CONVERTER (DAC)

A standard circuit implementation for SAR ADCs is based on charge redistribution in a network of capacitors, acting as both S&H, DAC, and subtractor. Charge redistribution DACs operate by binarily dividing the total charge applied to a capacitor array. This configuration is straightforward and is, in effect, a digitally controlled voltage attenuator. Another advantage of the charge redistribution DAC is that it is compatible with switched capacitor circuits.

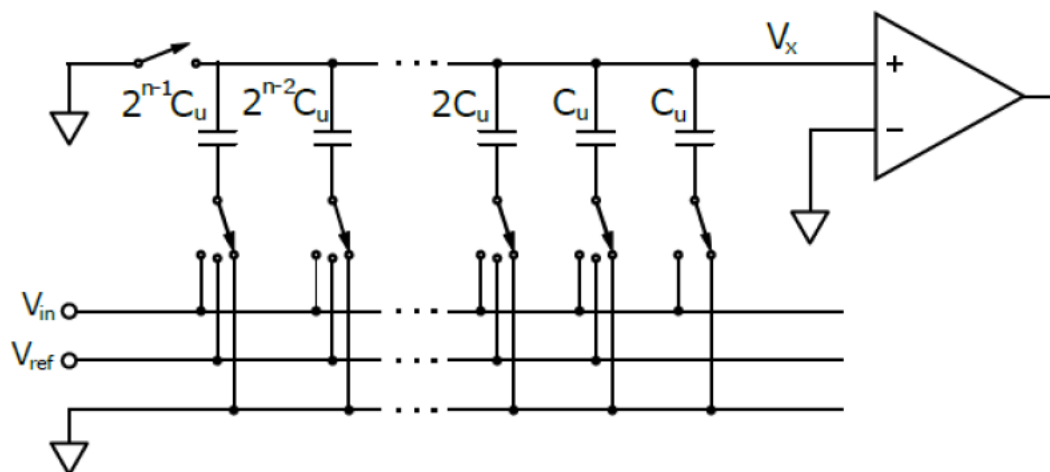


Figure 6: Charge Redistribution DAC

An advantage of this technique is that the DAC only consumes power during the charging and discharging of the capacitive circuits. The capacitors in the network are binary-weighted and range from C_u (unit capacitance) for the LSB to $2^{N-1}C_u$ for the MSB. An additional C_u (dummy) in parallel to the LSB capacitor gives a total capacitance of $2NC_u$. During the sampling phase, the top plates of the capacitors are discharged through a switch to the ground, and the bottom plates are charged with the input voltage. [4]

Given the definition of capacitance ($C = Q/V$), the total charge on the top plates of the network is calculated using the equation given below:

$$Q_{tot} = 2NC_u (0 - V_{in}) \\ = -2NC_u V_{in}$$

For the next clock cycle, the top plate switch is opened before the SAR set the MSB to '1' means MSB capacitor connected to V_{ref} and all other capacitors connected to ground. Since the top plate is only connected to the high input impedance of the comparator, the total charge remains the same. However, switching causes the charge to redistribute in all the capacitors. It results from a change in top plate potential V_x , as shown in the equation below this voltage is the difference between the DAC and input voltages.

$$Q_{tot} = Q_{MSB} + \dots + Q_{LSB} + Q_{dummy}$$

$$- 2NCuV_{in} = 2N - 1Cu(V_x - V_{ref}) + 2N - 1CuV_x \quad V_x = V_{ref} \cdot 2^{-N} - V_{in}$$

If V_x is negative means, V_{in} is greater than the $V_{ref}/2$, and the value of MSB is retained to '1'. Otherwise, it will reset to '0'. In the next conversion cycle, the second most significant bit is set to '1', generating a reference level of either $3/4V_{ref}$ or $1/4V_{ref}$ depending on the value of the MSB. And similarly, the further conversion will be done up to N-bit SAR ADC.

V. CONCLUSION

The aim of the paper is to design an ideal split capacitive DAC for the study of a SAR ADC. The performance requirement of SAR ADC can be represented in terms of static and dynamic metrics. Static metrics include differential-non-linearity (DNL) and integral-non-linearity (INL) while dynamic metric includes signal-to-noise-plus-distortion ratio (SNDR), spurious-free dynamic range (SFDR), signal-to-noise-and-distortion ratio (SINAD), and effective-number-of-bits (ENOB). All of these non-linear parameters depend mainly on the structure of the capacitive array of the feedback capacitive digital-to-analog converter (DAC). The capacitive array acts as both sampling capacitance and feedback CDAC, and its linearity affects the overall performance of ADC.

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