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### **Design and Verification of UART Communication Controller Using VHDL**

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**ABSTRACT:** The main objective of this paper is to design and verify full duplex UART module using VHDL. It is a serial communication protocol which transmits the information without clock signal. At the transmitter module the UART converts the parallel data into serial data and receives the same data at the receiver module. Designing of UART overall model includes the designing of transmitter and receiver model, with standard baud rate generator, and these modules are simulated using Modelsim. The UART designed with BIST concept where the architecture of UART will test the model for its correct ability. Verification of UART is done by using test bench in Modelsim where the different test cases of UART's were verified and its synthesis is done using XILINX ISE.

KEYWORDS: UART, Transmitter, Receiver, Serial data, Parallel data.

#### I. INTRODUCTION

Universal Asynchronous Receiver Transmitter (UART) is a kind of serial communication protocol; mostly used for shortdistance, low speed, low-cost data exchange between computer and peripherals. UARTs are used for asynchronous serial data communication by converting data from parallel to serial at transmitter with some extra overhead bits using shift register and vice versa at receiver. It is generally connected between a processor and a peripheral, to the processor the UART appears as an 8-bit read/write parallel port.

UART is a computer hardware device that is used to convert user's data to parallel and serial forms and vice versa. The word "Universal" is used to tell that the format of the transmitted data and speed of the transmission are configurable. An UART is usually an Integrated Circuit(IC) which is used for serial communication over a computer or a peripheral device. UART's are now commonly used in microcontrollers.

The Communication may be done in three different ways.

(A) Half-Duplex: - Both the UARTs can communicate with each other, but not simultaneously. The communication is only one-direction at a time.

(B) Full-Duplex: - Both the UARTS can communicate with each other simultaneously.

(C) Loop-Back mode: - This mode is for checking the accuracy of the UART. One UART will transmitted some data, and the same UART will receive the transmitted data.

#### **II. DESIGN**

UART design include designing of transmission and receiver side to achieve the communication between two systems.

A. Data Format

Once the transmitter receives parallel data from data bus it starts to add a start bit, parity bit and a stop bit. At the receiver part UART reads the data packet bit by bit at its receiver pin.

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Fig 1. Data Frame of UART

#### B. Wishbone interface

It is a standard bus interface it allows the parts of integrated circuits to communicate with each other.

#### C. Baud Rate Generator

A generic VHDL parameter allow the user to introduce a divisor between baud rate clock input (BR\_CLK\_I )and the bitstream frequency. In addition, the core insert a 4 divisor for sampling purpose at the receiver. Thus:

Baudrate = Freq(BR\_CLK\_I) / BRDIVISOR / 4

Where BRDIVISOR is the generic parameter.

#### D. RS-232 Communication Protocol

It is a peripheral device which allows to exchange serial data between the transmitter and receiver.

#### **III. METHODOLOGY**

#### IMPLEMENTATION OF TRANSMITTER AND RECEIVER



Fig 1. Block diagram of UART Device

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#### A. UART Transmitter

It consist of shift register, hold register and FIFO module. The transmitter section accepts parallel data, makes the frame of the data and transmits the data in serial form on the Transmitter Output (TXOUT) terminal. Data is loaded from the inputs TXIN0-TXIN7 into the Transmitter FIFO by applying logic high on the WR (Write) input. If words less than 8 bits are used, only the least significant bits are transmitted. FIFO is 16-byte register. When FIFO contains some data, it will send the signal to Transmitter Hold Register (THR), which is an 8-bit register. At a same time, if THR is empty it will send the signal to FIFO, which indicates that THR is ready to receive data from FIFO. If Transmitter Shift Register (TSR) is empty it will send the signal to THR and it indicates that TSR is ready to receive data from THR. TSR is a 12-bit register in which framing process occurs. In frame start bit, stop bit and parity bit will be added. Now data is transmitted from TSR to TXOUT serially.

#### B. UART Receiver

Similar to transmitter section, UART receiver also have shift register and FIFO module along with buffer registers also used to store data. Once the data frame is received if the Receiver Hold Register (RHR) is empty it sends signal to RSR so that only the data bits from RSR goes to RHR which is an 8 bit register. The remaining bits in the RSR are used by the Error logic block. Now if receiver FIFO is empty it send the signal to RHR so that the data bits goes to FIFO. Before de-framing the data receiver checks the parity bit for errors and then removes the start and stop bit .When RD signal is asserted the data is available in parallel form on the RXOUT0-RXOUT7 pins.

#### C. UART WITH BIST-BILBO

BILBO (Built in Logic Block Observer) is a scan register that can be modified to serve as a state register, a pattern generator, a signature register, or a shift register. In summary the BILBO operating modes are represented in TABLEI.

The test starts with the initialization of the BILBO by applying a "seed" to its serial-in (si) pin. The initialization can be obtained by configuring BILBO's operating mode ("bilbo\_mode") to "00" (shift register mode). Following the initialization, the bilbo\_mode is set to "01" so that "Register A" is configured as LFSR ("bilbo\_mode" = "01") and Register B as MISR ("bilbo\_mode" = "11" (Note: XOR force "01" to "11")). "Register A" (LFSR) produces an 8-bits pseudo random pattern data in parallel. The parallel data is then fed to the UART's transmitter.

B1B2	<b>Operating Modes</b>
00	Shift Register
01	LFSR/PRPG
10	Normal
11	MISR

#### **IV. VERIFICATION OF UART**

The major focus of the verification is to create verification environment to verify the design with different test cases. To verify the functional correctness of the design test case are developed where the design includes the transmitter and receiver. The test cases involves the verification of data from transmitter to receiver and also from the receiver to transmitter that is the parallel data from transmitter is converted to serial data at the transmitter module and same parallel data received at the receiver. Data from the Transmitter is transmitted simultaneously to the receiver.

#### V. RESULT

- 1. Designing a transmitter and receiver model of UART using VHDL code.
- The transmission of data with standard Baud Rate Using RS-232 Communication protocol.
  Increasing the speed of data transmission with appropriate baud rate.
- 4. Identifying the error in the transmission using Parity error Bits.
- 5. Verification of transmitter and receiver module.
- 6. The Overall UART module is designed and simulated Using Modelsim.

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a. Simulation result of Transmitter

The Fig 3 shows the serial transmission of data with standard baud rate 9600 bits per second. Here data word length taken as 8-bits and odd parity is selected. Whenever the reset is high it begins to transmit the data. Data to be transmitted are 00000000 and they are applied to the transmitter pin. The serial transmission is observed at the data out pin.

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Fig 2. Simulation Result of Transmitter

#### b. Simulation result of Receiver

The fig 4 shows the reception of serial data. The data is received at the receiver pin. Once the data is received the start and stop bits are discarded the complete frame is received and data is converted into parallel internally and it is stored at the FIFO register. By making load high the parallel data is made available at receiver output.

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/txunit/clk	1								
/txunit/reset	1								
/txunit/enable	1								
/txunit/load	0								
/txunit/txd	0								
/txunit/trege	0								
/txunit/tbufe	1								
/txunit/datao	0	0							
/txunit/tbuff	0	X 10							
/txunit/treg	255	X	χo	128 (192 )224	4 )240 )248	252 (254 )	255		
/txunit/bitcnt	9	0	<u>ľ</u> 1	2)3/4	)5 )6	(7 )(8 )(	<u>) 10</u>		
/txunit/tmptrege	0								
/txunit/tmptbufe	1								

Fig 3. Simulation Result of Receiver

c. Simulation result of Combined UART

Fig 4 shows the simulation result of UART as single entity. It shows the functioning of receiver and transmitter sections. Where the transmitter section of UARt converts the paralel data into serial data before its transmission through transmitter output pin at the same time the receiver can receive the serial data through receiver input pin, and covert into parallel form and makes available at receiver output pin.



Fig 4.Simulation Result of UART

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#### c. Simulation Result of Test bench

The fig shows the simulation result for test bench which is written to verify wheather the desgin is working properly or not. The waveform shows that the received output is same as the input data



Fig 5. Simulation Result of Testbench

#### VI. CONCLUSION

This paper describes the designing of UART using VHDL. The design part involves the designing of all the submodules of transmitter and receiver section, baud rate generator and also registers. The overall UART module is designed and verified using Modelsim. In verification, different test cases are used to verify the working operation of the design. The simulation of each module shows that the design is working efficiently.

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