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Review on High Performance Sigma-Delta ADC for AudioDecoder

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ABSTRACT:-This paper gives a high performance sigma delta Analog to Digital Converter (ADC) applied in computer audio decoder chip. In this design, a 3rd-order single-loop CIFF topology is chosen to achieve the high performance ADC. Its signal bandwidth is 20 KHz, sampling frequency is 10.24MHz and oversampling ratio is 256. Local feedback coefficient 1 g is used to reduce quantization noise. The nonlinear model of modulator is given and the stability is analyzed. It is got that when quantizer gain is bigger than 0.322 the system is stable. According to simulation, Signal to Noise Ratio (SNR) is 123.1dB and Effective Number of Bits (ENOB) is 20.15bits. When input level is bigger than -3dBfs, the modulator is overload and becomes unstable. Then the integrator, quantizer and feed forward summation in ADC circuit are designed. Then the ADC is implemented in 0.6um CMOS process, and the test result shows that its performance is 99.28dB.

I. INTRODUCTION

Sensors are ubiquitous devices, including audio, temperature, light, magnetic, capacitive sensing, as well as bio-potential acquisition and biometrics identification for wearable devices. It usually processes narrow-band signals with frequencies from DC to tens of kHz [1]–[4]. For battery-powered sensor systems, energy-efficient analog-to-digital converter (ADCs) are especially important and are usually customized to meet the sensor's requirements. Such ADCs must also be robust against offset and flicker noise. In addition, the integrated ADC often needs to be multiplexed across many channels and applications requiring a large number of channels, such as image sensors or bio-potential acquisition [3]–[6]. These must be very efficient in terms of energy and area. Among all categories of ADCs, delta-sigma ADCs utilizing oversampling and noise-shaping are widely used for achieving high resolution. The ADCs are often operated in incremental mode for sensor interfaces, and the incremental ADCs (IADCs) offer the best choice for achieving high energy efficiency [1]–[6]. Since the modulators of the IADCs usually have finite impulse response (FIR), the corresponding decimation filter can be as simple as a cascade of integrators (CoIs), much simpler than their counterparts that use an infinite impulse response (IIR) decimation filters. The other advantages of the IADCs include easy multiplexing and low latency and are also less subject to idle tones [10]. A first-order IADC requires a long conversion time, resulting in poor energy efficiency. To shorten the conversion time and thereby improve energy efficiency, higher-order IADCs can be used. However, they are more prone to instability and have a reduced input range. Hence, multi-stage noise-shaping (MASH) IADCs [11], and hybrid IADCs incorporating with Nyquist-rate ADCs have been investigated. This paper reviews energy-efficient IADC architectures, such as extended counting [6], [9], two-step, multi-step and zoom structures. The circuit techniques for implementing energy-efficient IADCs are also reviewed. Several important energy-efficient amplifier topologies have been proposed in the past decade, including inverter-based amplifiers and its improved versions with optimal gm/Id are also described in this paper. Another important amplifier topology, the ring amplifier which benefits from high gain and fast settling is also reviewed. In recent years, dynamic amplifiers have drawn attention, because they exhibit the lowest bandwidth for a target speed due to their class-B operation. The principles of several dynamic amplifiers are described in this paper. Other useful techniques for implementing energy-efficient IADCs such as chopping, FIR DAC [7], integrator slicing, and 1st integrator optimization are also discussed.

II. ADC

Depending on the sampling rate, analog-to-digital converters are categorized into two types namely Nyquist rate converters and oversampling converters. Nyquist rate ADCs sample the analog input at the Nyquist frequency, f_n such that $f_s = f_n = 2 \times f_b$, where f_s is the sampling frequency and f_b is the bandwidth of the input signal. Oversampling ADCs sample the analog input at much higher frequencies than the Nyquist frequency. Sigma-delta ADCs come under this category. In a sigma-delta ADC, the input signal is sampled at an oversampling frequency $f_s = K \times f_n$ where K is defined as the oversampling ratio and is given by

$$K = f_s / 2f_b$$

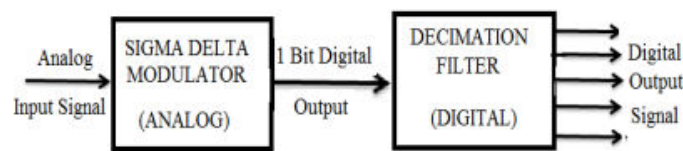


Figure 1: Block Diagram of Sigma-Delta ADC

Figure 1 depicts the basic blocks of a sigma-delta ADC. It consists of a sigma-delta modulator and a decimation filter. The modulator will be implemented with analog technique to produce a single bit stream and a digital Decimation filter will be implemented to achieve a multi bit digital output thus completing the process of analog to digital conversion.

2.1. Quantization Noise

The analog input signal can take any continuous value. But a digital n -bit signal can only settle to 2^n discrete values. It is this difference between the analog value and its digital representation, which causes the distortion known as the quantization noise. Quantization error is defined as a measure of an n -bit converter's failure to represent precisely an analog signal in the digital domain.

2.2. Oversampling, Noise shaping and Digital Filtering

Oversampling is a process of sampling the input signal at a frequency much greater than the Nyquist frequency (Nyquist frequency, f_n is defined as twice the input signal bandwidth, f_b). This process greatly reduces the quantization noise in the required band. The sampling theorem or the basic Nyquist sample theory states that the sampling frequency of a signal must be at least twice the input signal frequency in order to reconstruct the sampled signal without distortion. Figure 2(a) shows the spectrum of an under sampled signal [8]. Here the sampling frequency, f_s is less than twice the input signal frequency $2f_o$. The shaded portion of the figure shows the aliasing which occurs when the sampling theorem is not followed. We get a distorted signal at the output when a signal contaminated with aliasing is recovered. Figure 2(b) shows the spectrum of an oversampled signal [4]. Here the sampled signal in the frequency domain appears as a series of band-limited signals at multiples of sampling frequency that are widely spaced. This process puts the entire input bandwidth at less than $f_s/2$ which reduces the aliasing.

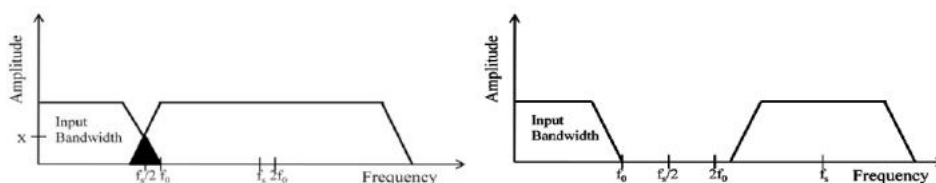


Figure 2(a): Under sampled signal 2(b) Oversampled signal spectrum

Noise shaping is a property of sigma-delta ADCs resulting from the application of feedback that extends dynamic range. A closed loop modulator works as a high-pass filter for quantization noise and as a low-pass filter for the input signal. When the signal is oversampled, the quantization noise power in the Nyquist bandwidth ($f_s/2$) spreads over the wider bandwidth, $Kf_s/2$ where; K is the oversampling ratio, which is shown in Figure 3. The total quantization noise is

still the same but the quantization noise in the bandwidth of interest is greatly reduced. The figure also illustrates the noise shaping achieved by using the oversampled sigma-delta modulator. In a sigma-delta ADC, the analog modulator samples the input at oversampling ratio and after the input signal passes through the modulator it is fed into the digital filter or a decimator. The function of the digital filter is to provide a sharp cutoff at the bandwidth of interest, which essentially removes out of band quantization noise and signals [5] as shown in Figure 3.

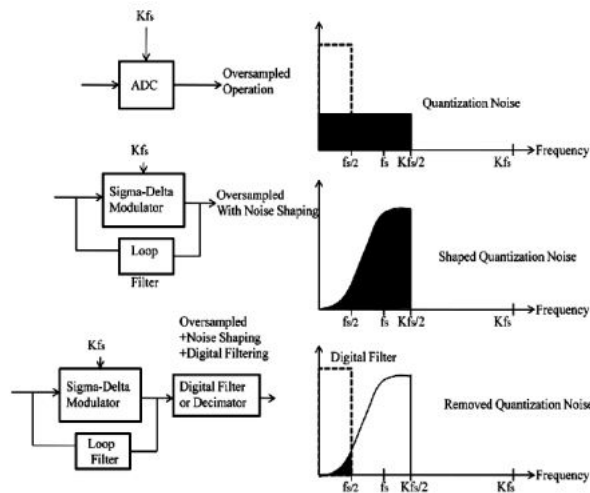


Figure 3: Effect of Noise shaping and Digital Filtering

The CIC filter first performs the averaging operation then follows it with the decimation. A simple block diagram of a first order CIC filter is shown in Figure 4. In Figure 4(a), the differentiator circuit needs K (oversampling ratio) delay elements, which are implemented using registers. The number of delay elements increases as oversampling ratio increases, and as well the number of registers bits that are used to store the data. This type of implementation becomes complex and requires more area as we go for higher order and higher sampling rates. This problem can be overcome by implementing a decimation stage between the integrator and differentiator stages as shown in Figure 4(b). Here the clock divider circuit divides the oversampling clock signal by the oversampling ratio, K after the integrator stage. The same output can be achieved by having the decimation stage between integrator stage and comb stage. By dividing the clock frequency by K the delay buffer depth requirement of the comb section is reduced. In Figure 4(b), the integrator operates at the sampling clock frequency, f_s while the differentiator operates at down sampled clock frequency of f_s/K [9]. By operating the differentiator at lower frequencies, a reduction in the power consumption is achieved.

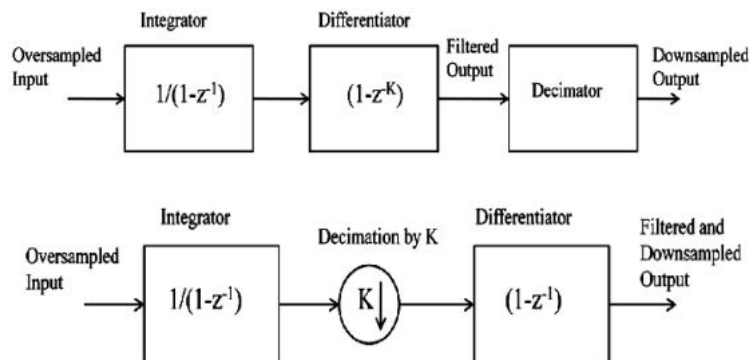


Figure 4: Block Diagram of CIC filter with (a) External decimator (b) Internal decimation

III. SYSTEM-LEVEL ANALYSIS AND DESIGN

For sigma-delta ADC, there are two traditional structures: single loop structure and Multi-stage noise Shaping (MASH) structure. Each of these structures can be realized with one-bit quantizer or multi-bit quantizer. For single loop sigma delta modulator, it is not sensitive to mismatch of capacitances and charge leaking. In order to increase the precision

high order is needed. But this would make the system conditional stable. MASH modulator is always stable. But mismatch of capacitances and charge leaking have big influence on MASH modulator. This requires a very good manufacturing process. And MASH modulator has digital part, which would increase the complexity of the circuit. In this design, single loop structure is chose [9].

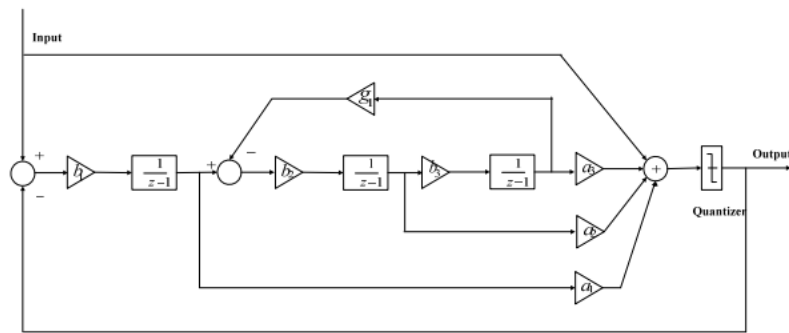


Figure 5: Block Diagram of 3rd-order $\Sigma\Delta$ ADC System

Single loop modulator has two main structures: Chain of Integrators with weighted FeedForward summation (CIFF structure) and Cascade of Integrators with distributed FeedBack (CIFB structure). CIFF structure is a wonderful structure to realize Butterworth filter and its signal transfer function is flat in signal bandwidth. In CIFB structure the input and output of integrators include signal and quantizer output, so the amplitude of integrators' input and output is very big. Little gains are required in CIFB structure. The gain in switch-capacitor circuit is realized by proportional capacitors. Little gains means big capacitors which would lead to more power consumption and bad output settle. CIFF structure has more advantages than CIFB structure [15-17]. So this paper also chooses the CIFF structure. For sigma-delta ADC, the higher order and higher oversampling ratio achieve higher precision. In computer audio application, 16 bit precision is needed. So in this paper a thirdorder single loop CIFF structure modulator is designed. The signal bandwidth is 20KHz, oversampling ratio is 256, and the sampling clock is 10.24MHz. The third-order sigma-delta ADC topology is shown as Figure 5. There are three integrators, a one bit quantizer and gains.

IV. CONCLUSION

This paper presents design of high performance sigma-delta ADC applied in audio decoder chip. The CIFF third-order sigma-delta modulator system is analyzed. The Butterworth filter function is used to realize the NTF of modulator. Based on nonlinear model, it is got that when the quantizer is bigger than 0.322 the system is stable. Through Simulink simulation, the SNR of system is 123.1dB and ENOB is 20.15bits. The performance satisfies the demand of computer ADC decoder. From the output histograms of three integrators, it is gotten that the output ranges of three integrators satisfy the limit of integrators. And SNR is almost linear with input level. When input level is bigger than -3dBfs, the modulator is overload. The test result shows that the SNR of this ADC is 99.28dB and ENOB is 16.2bits. The single-end amplifier in this ADC brings up the harmonic in signal bandwidth.

REFERENCES

- [1] LinCW, LeeYP, ChenWT. A 1.5bit 5th Order CT/DT Delta Sigma Class D Amplifier with Power Efficiency Improvement. Proceedings of Circuits and Systems. Washington. 2008; 280-283.
- [2] BaridRT, FiezTS, KulahH. Linearity Enhancement of Multibit Delta-Sigma A/D and D/A Converters Using Data Weighted Averaging. Proceedings of Circuits and Systems 1995; 753-762.
- [3] MillerMR, PetrieCS. A Multibit Sigma-Delta ADC for Multimode Receivers. IEEE Journal of Solid-State Circuits. 2003; 38(3): 475-482.
- [4] BorkowskiMJ, RileyTAD, HakkinenJ. A Practical delta-Sigma Modulator design Method Based on periodical Behavior Analysis. IEEE Transactions on circuits and system. 2005; 52(10): 626-630.
- [5] JensS, TomasT, DorisSL. A 0.7V MOSFET-Only Switched-



OpampDeltaSigmaModulatorinStandardDigitalCMOSTechnology.IEEEJournalofSolid-StateCircuits.2002;37(12):1662-1669.

- [6] MichielAP, AntonB, JohanHH. A Second-order Sigma-Delta ADC using MOS Capacitors for Smart Sensor Applications. Proceedings of IEEE Sensors .2004;421-424.
- [7] Simona Brigati, Fabrizio Francesconi, Piero Malcovati, Franco Maloberti, "A Fourth-Order Single-Bit Switched-Capacitor $\Sigma\Delta$ Modulator for Distributed Sensor Applications" 2004
- [8] R. Schreier and G. C. Temes, Understanding Delta-Sigma Data Converters. New York: Wiley-IEEE Press, 2004.
- [9] Shashant Jaykar, Prachi Palsodkar, Pravin Dakhole, Shashant Jaykar, "Modeling of Sigma-Delta Modulator Non-Idealities in MATLAB/SIMULINK" July 2011.
- [10] Khalid K. Mohammed, "Design and Implementation of Decimation Filter for 15-bit Sigma-Delta ADC Based on FBGA" April 2014.
- [11] Anna S. Kuncheva, Thibault Mougél, Lukas Fucik, Blagomir Donchev, Marin Hristov, "Design of a Decimation Filter for Novel Sigma-Delta Modulator" July 2006.
- [12] Youngkil Choi, Jeongjin Roh, Hyungdong Roh, Hyunseok Nam, "A 99-dB DR Fourth-Order Delta-Sigma Modulator for 20-kHz Bandwidth Sensor Applications" Feb 2009.
- [13] https://inst.eecs.berkeley.edu/~ee247/fa08/files07/lectures/L15_f08.pdf
- [14] J. S. Wilson, Sensor Technology Handbook. New York: Elsevier, 2005



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