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### Designing a Self-Programmable Multipurpose Digital Filter Based on FPGA

Shubham Suryavanshi<sup>1</sup>, Satyarth Tiwari<sup>2</sup>

P.G. Student, Department of Electronics & Communication Engineering, Bhabha University, Bhopal,

Madhya Pradesh, India<sup>1</sup>

Assistant Professor, Department of Electronics & Communication Engineering, Bhabha University, Bhopal,

Madhya Pradesh, India<sup>2</sup>

**ABSTRACT:** Conventional digital filter can only obtain fixed frequency domain characteristics at a time. In order to obtain variable characteristics, the digital filter's type, number of taps and coefficients should be changed constantly such that the desired frequency-domain characteristics can be obtained. This paper proposes a method for self-programmable Variable Digital Filter (VDF) design based on FPGA. Taking finite impulse response (FIR) digital filter as an example, we implement a digital filter system by using Custom embedded Micro-Processor, programmable FIR macro module, coefficient-loader, clock manager and A/D or D/A controller and other modules. The self-programmable VDF can provide the best solution for realization of digital filter algorithms, which are the low-pass, high-pass, band-pass and band-stop filter algorithms with variable frequency domain characteristics. The design examples with minimum 1 to maximum 32 taps FIR filter, based on Modelsim post-routed simulation and onboard running on XUPV5-LX110T, are provided to demonstrate the effectiveness of the proposed method and the online-adaptability of variable digital filters.

**KEYWORDS**: Self-programmable Digital Filter; Variable Digital Filter; Field Programmable Gate Array; Embedded Micro-Processor

#### I. INTRODUCTION

Digital Filter has many applications in communication systems, image processing, acoustic signal processing and other fields. Because of its good features such as only zeros, linear phase, stability and design flexibility, the FIR filter is widely employed in digital signal processing (DSP). Considerable work has been done to design a FIR filter using constant coefficients, which can only obtain fixed frequency-domain characteristics at a time. Unlike conventional digital filter, Variable Digital Filters (VDFs) can change their filter-type, number of taps and coefficients constantly such that the desired frequency-domain characteristics can be obtained.

Previous researches have been proposed variable digital filter implementation using the partial reconfiguration, in which a given subset of internal components was partially reconfigured [1]. A partially self-reconfigurable adaptive FIR filter system was proposed in paper [2], in which the dynamic partial reconfiguration method and configuration memory on FPGA were used. Nowadays, the Embedded Micro-Processor (EMP) based on FPGA generates a special interest on this field [3-8].

In this paper, a design scheme of VDFs based on FPGA and EMP is presented, which plays both the Coefficientcalculation and Programmable FIR filter. The design scheme accords with the design method of system on a chip (SOC). Moreover, it is possible to update the FIR algorithm and meet the need of other digital filter systems in the future.

The rest of this paper is organized as following: Section 2 describes the system architecture of the proposed method. The Custom embedded Micro-Processor is discussed in section 3. Section 4 describes the Coefficient-load Controller. In Section 5, the programmable FIR macro module is presented. The experiments and results are presented in section 6. Finally, the conclusion is given in Section 7.

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#### **II. SYSTEM DESIGN SCHEME**

The hardware devices for the implementation of the proposed VDF based on FPGA consists of four parts. A view of the hardware structure of the VDF is shown in Fig.1.



As shown in Fig.1, the hardware structure includes a Custom embedded Micro-Processor (CeMP) which is the control-center of the system. The Programmable FIR (P-FIR) is a FIR filter whose filter-type, coefficients and number of taps can be changed to obtain the desired frequency-domain characteristic. The coefficient-load controller reloads the coefficients from CeMP into the P-FIR. The Clock-manager and A/D controller is adapted to manage the clock-generator of the modules in the system and control the external A/D or D/A converter.

The decision to adapt this kind of scheme is mainly driven by the powerful capability of computational processing, signal processing offered by the embedded micro-processor implemented in FPGA. It is possible to meet the need to update the coefficient-resolving algorithm. In addition, all functions integrated on a single chip takes the advantages of anti-interfere and reducing power consumption of the proposed system.

#### I. CUSTOM embedded MICRO-PROCESSOR

In this work, we adapt MicroBlaze to construct the custom embedded macro-processor (CeMP). MicroBlaze is an embedded soft RISC processor core with 32-bit data and address bus. The processor core is optimized for implementation in XILINX FPGAs, and supports both on-chip BlockRAM and external memory [8]. Meanwhile, it supports some peripherals and interface. In addition, Xilinx provides some soft peripheral IP for this soft processor core. At the same time, according to the need of the specific application, designer can create and add their custom IP to the application system. Because of these advanced features, all the functions related coefficient-resolving, FIR and control logic can be implemented on a single FPGA.

The block diagram of CeMP is shown in Fig.2. As shown in Fig.2, the CeMP is composed of Microblaze soft-core, BlockRAM, Interrupt Controller (IntC), Timer, DDR2/SRAM Controller (MemCntlr), Coefficient-Load Controller (CLC) and Human-machine Interface. The Processor Local Bus (PLB) allows the communication and the interchange of information between Microblaze and the peripherals. The Local Memory Bus (LMB) establishes the connection of the BlockRAM with MicroBlaze. Coefficient-Load Controller is a custom IP core that will be discussed in detail in Section IV.

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Figure.2 CeMP block diagram

We design and implement the CeMP using the Xilinx<sup>®</sup> Embedded Development Kit (EDK) which is a part of Xilinx<sup>®</sup> Integrated Software Environment (ISE) Suite 12.1. The Xilinx<sup>®</sup> EDK includes the Xilinx Platform Studio (XPS), the embedded system tool suite, the embedded processing IP cores and the Platform Studio SDK (Software development Kit). For more information about Xilinx<sup>®</sup> EDK, refer to Xilinx<sup>®</sup> Software Manuals [9-10].

CeMP in this system performs several tasks as following: 1) interfacing the external human-interface module to receive the user command and filter parameters;

2) resolving the FIR coefficients and filter taps; 3) writing coefficients into the coefficient register group of Programmable FIR filter (P-FIR); 4) sending the control signal to P-FIR so as to construct the desired digital filter; 5) managing the clock resource and controlling the external A/D or D/A converter and so on.

#### II. COEFFICIENT-LOAD CONTROLLER

In this design, a custom IP for coefficient-load namely the Coefficient-Load Controller (CLC) is designed and applied to our system. The custom IP mainly accomplishes the functions of receiving data from CeMP and loading these data into Programmable-FIR (P-FIR). Fig.5 shows the CLC block diagram.



Figure.4 Timing waveform of Coef-load controller

As shown in Fig.3, the coefficients and control signal are stored in the BlockRAM. When the filter-type and taps are needed to be updated, the CeMP writes the corresponding data into P-FIR under the control of signal 'LoadEn' and 'Write'. 'CoefAddr' is the address of the coefficient register in the register group of P-FIR. 'CoefData' is the values of the coefficients. 'Ctrl\_Bits' is the signal that is used to control the filter-type and filter taps for the P-FIR. The timing waveform of CLC is shown in Fig.4.

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#### III. FPGA-based PROGRAMMABLE FIR

A programmable FIR filter architecture is designed and developed as shown in Fig.5 and Fig.6. Fig.5 shows a macro module of the programmable symmetric FIR in our system. Here, '*xin*' is the input sequence, '*h*(*n*)' is the tap-coefficient, '*ctrl\_bits*' controls the order and type of FIR filter, '*xout*' is the shift output and 'y' is the FIR output. '*xout*', '*xin*'' and 'y'' can be used for cascaded FIR.



Figure.5	FIR	Macro	Module
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As shown in Fig.5, a symmetric FIR module is composed of two delay-units, two adders, one multiplier and four multiplexers (muxes), which can be programmed as 1 or 2 taps with cascading or non-cascading under the control of ' $ctrl_bits$ '. Table.1 shows the filter taps map for the programmable module.

Ctrl_bits		Tama	Casaadahla
bit0	bit1	Taps	Cascadable
0	0	1	Yes
0	1	1	No
1	0	2	Yes
1	1	2	No

Table.1	Filter	taps	map.
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The FIR macro module can be used to construct higher-order FIR filter by cascading. N-order FIR filter can be obtained through cascading N/2 (when N is even) or N/2+1 (when N is odd) FIR macro modules. Supposing N/2 is n, when N is even, the 1<sup>st</sup> to (n-1)th macro modules are configured as 2-taps with cascading and the last macro module is configured as 2-taps without cascading. When N is odd, the 1<sup>st</sup> to *n*th macro modules are configured as 2-taps with cascading and the (n+1)<sup>th</sup> macro module is configured as 1-tap without cascading.

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Fig.6 shows a programmable FIR filter system, which can be programmed as minimum 2 to maximum 8 taps FIR filter operation. The *ctrl\_bits* signal is 8bits as shown in Table.2. In our system, we employ eight FIR macro module to construct minimum 1 to maximum 32 taps FIR filters.



ctrl_bits	Taps	Coefficents
11xxxxxx	2	h(0)
1001xxxx	3	h(0),h(1)
1011xxxx	4	h(0),h(1)
101001xx	5	h(0), h(1), h(2)
101011xx	6	h(0), h(1), h(2)
10101001	7	h(0),h(1),h(2),h(3)
10101011	8	h(0),h(1),h(2),h(3)

Table.2 Taps map for cascaded FIR filter

#### **III. EXPERIMENTAL RESULTS**

We use Xilinx 12.1 for synthesizing purposes. The synthesis is done on Xilinx's Virtex-5 XC5VLX110T. The whole system is implemented in the ML505 Xilinx<sup>®</sup> Development Board that houses a XC5VLX110T-FF1136 Virtex-5 FPGA and a System ACE module. The CeMP is clocked at 300MHz and the peripherals run at 100MHz. In our implementation, the filter specifications: sampling.

frequency fs = 10MHz, Hamming window, the coefficient word-length is 16bit fixed point format with one fractional bit, filter order N = 32, input value word-length is 12bit, FIR output word-length is 34bit (MSB truncation to 14bit before inputted to D/A converter). The test signal is the sum of a Sine wave whose frequency is 50KHz and a linear chirp wave whose frequency is between 0.1Hz and 3MHz, which is converted to 12bit digital signal through A/D converter and serves as the FIR input.

In our system, the A/D converter is ADS805 that provides 20MHz sampling, 12bits digital output, the D/A converter is DAC5674 that provides 14bits resolution and high speed up to 400MSPS.

The post-simulation result is shown in Fig.7-Fig.10. From Fig.7-Fig.10, it can be seen that the proposed system in this paper can change its frequency domain characteristics to implement LPF, HPF, BPF and BSF and meet the design requirements.

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Figure.7 Low pass filter (Fc=1.25MHz) Fc is the upper cut-off frequency



Figure.8 High pass filter (Fc=1.25MHz) Fc is the lower cut-off frequency



Figure.9 Band pass filter (Fc1=1.0MHz, Fc2=2.0MHz)



Figure.10 Band stop filter (Fc1=1.0MHz, Fc2=2.0MHz)

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#### **IV. CONCLUSION**

A high-performance and parameterized FIR filter is presented, which is implemented by using Custom embedded Micro-processor, Coefficient- Load Controller, Programmable FIR Micro Module. All the modules are implemented in a single FPGA, which has more flexibility, power-efficiency and stability than conventional FIR filter. The proposed method can be used to realize online-reconfigurable DSP algorithms for noise removal operation.

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