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**Department of ECE, Adhiyamaan College of Engineering, Hosur, Tamilnadu, India**

# **Design and Implementation of Optimizing the Energy through DVFS Techniques in 3D NoC**

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**ABSTRACT:** As Networks-on-Chip (NoCs) continue to consume a large fraction of the total chip power budget, dynamic voltage and frequency scaling (DVFS) has evolved into an integral part of NoC designs. such as buffer occupation and channel utilization. The proposed methodology utilize highly predictable properties of cache-coherence communication to derive more specific and reliable NoC traffic predictions. 3D as well as network-on-chip (NoC), are two recent design approaches that promise to alleviate the consequences of interconnection degradation. This project introduces a new methodology for power efficient application mapping onto 3D NoC-based devices. Experimental results prove the efficiency of the proposed methodology since we achieve energy savings respectively. In our project we have implemented four routers in mesh connection in which all data flow is controlled by the HUB. Each Router is connected with some processing device which gives or requires the data to/from other devices.

**KEYWORDS:** Networks-on-Chip (NoC), Dynamic Voltage and Frequency scaling, Latency, 3D NoC, HUB.

## **I. INTRODUCTION**

The steady increase in core counts coupled with power viscosity limitations and the breakdown of Dennard spanning demand NoC that give a scalable communication fabric for connecting a large number of coffers within a chip. With the increase in the number of cores, the underpinning communication fabric called the Network-on-Chip (NoC) has come critical for data communication between the cores and the memory scale. The immense number of transistors that are packed onto multicore chips as transistor point size continues to shrink into the sub-nanometer region has caused numerous new and unique power problems to emerge. Two critical power problems facing Network-on Chips are high static power and dynamic energy. Redundant dynamic energy is the result of storing and switching data within routers and links. NoC size increases proportionally with core count to accommodate the increased data communication demands. Dynamic Voltage and Frequency Scaling is the focus of important previous exploration and may be used to reduce dynamic energy. Therefore energy effectiveness of 3D NoC would ameliorate while labors are within the respectable friction. Also, the voltage swing reduction increases the needed time to transmit the packet. By exploiting the benefit of low quiescence of 3D NoC armature and employing this scaling system in the architecture would compensate the quiescence and also the performance declination of the network.

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## II. RELATED WORK

### 1. Energy Optimization in 3D NoC through DVS Technique

As NoC's demand high power budget on the chip, DVS approaches can be applied in NoC to achieve efficient power and thermal management. DVS approaches can be applied in NoC resources to achieve energy efficiency and temperature reduction in 3D architecture. The proposed link and router architectures are respectively depicted. As some parts of the applications possess error resiliency nature, the supply voltage of the link and the routers can be reconfigured to the lower level when the approximable packet data would be mapped.

### 2. Optimizing 3D NoC Design for Energy Efficiency A machine Learning Approach

GPU NoCs are usually implemented as two separate networks to avoid protocol deadlock. Request messages are sent from many shader cores to a few memory controllers in the request network. To evaluate the performance of different NoCs, we use a cycle-accurate NoC simulator that can simulate any regular or irregular 3D architecture. Our system consists of 64 cores and 64 network routers equally partitioned in four layers.

### 3. Designing Scalable Hybrid Wireless NoC for GPGPUs

A robust design optimization methodology to improve the energy efficiency of 3D NoC architectures by combining the benefits of SW networks and machine learning techniques to intelligently explore the design space. The overlaid wireless network is implemented as 2x4 mesh. We choose mesh topology for wireless network because it has low design complexity and simple routing algorithms.

## III. METHODOLOGY

The input port models are built on a simple voltage regulator scheme that allows per router DVFS and the selection of four different voltage levels. For 8 Input 8 output architecture of Asynchronous NoC router is as shown.

The Router has four modules:

1. Input Arbiter
2. Routing Engine and Look up Table: Routing engine provides control signals to mux in crossbar matrix
3. 4x4 crossbars Matrix
4. Circular FIFO Buffer

Each router is combined based on 3D mesh topology then each router gives 8 port output signals.

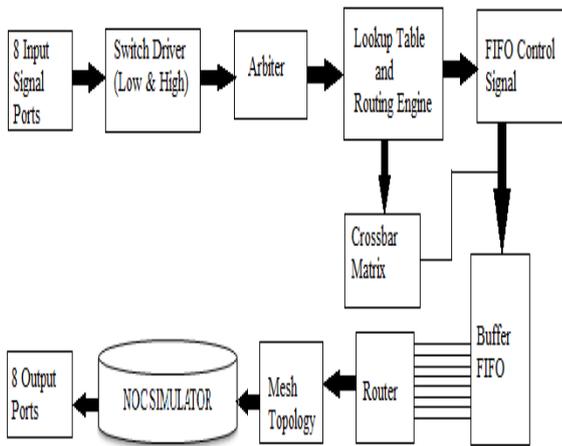


Figure 1: Block Diagram

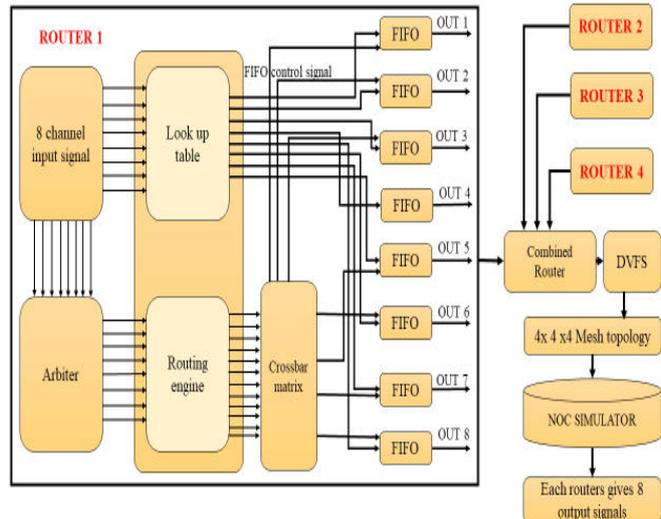


Figure 2: Architecture Design of 3D NoC

#### IV. EXPERIMENTAL RESULTS

Optimizing the energy through dynamic voltage and frequency scaling techniques in 3D NoC was successfully designed and implemented. The output screenshots is given below.

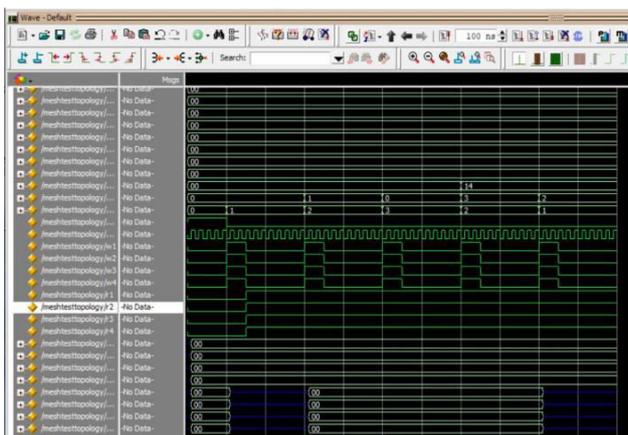


Figure 3: Simulation of Switch

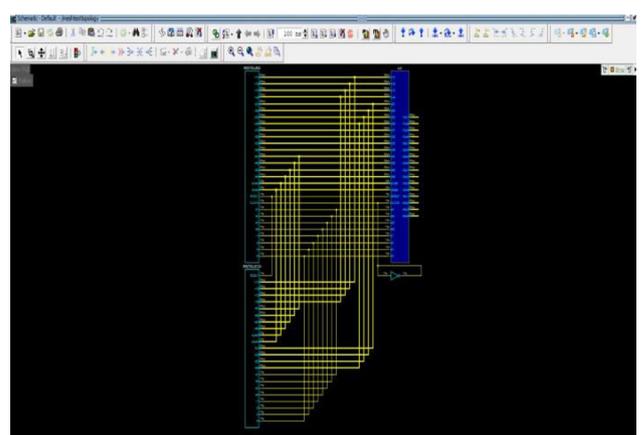
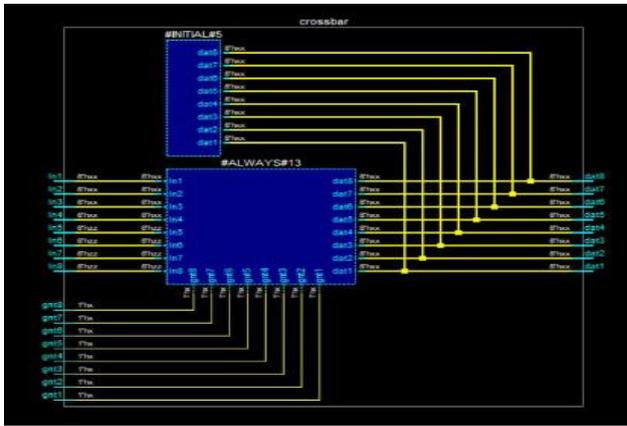
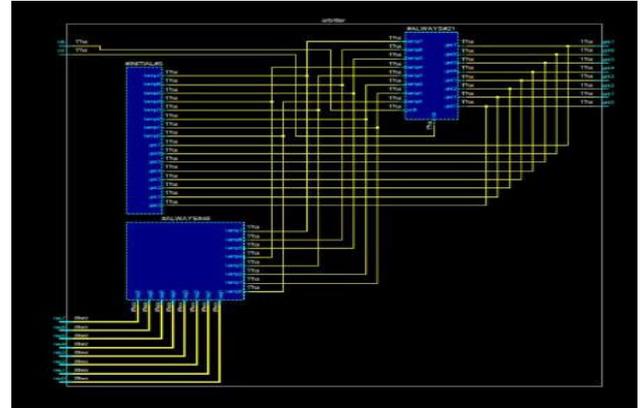


Figure 4: Simulation View of Mesh Topology



**Figure 5: Inside View of Arbiter**



**Figure 6: Inside View of Crossbar**

## V. CONCLUSION

Three-dimensional 8 x 8 Asynchronous Mesh NOC Architecture Router. In our proposed router design, we implemented mesh topology with 4 routers. All the 4 Routers are connected to the Hub, which is responsible for creating connections between routers depending upon the source and destination address. The supply voltage of the links and the routers of NoC are scaled to reduce the power consumption and thermal dissipation in 3D NoC which account as a major challenges in 3D NoC architectures. Thus, the energy efficiency of 3D NoC is significantly improved due to employing DVFS technique by trading off accuracy within an acceptable variance. Also, applying the scaling method in 3D architecture would compensate the latency increase and the performance degradation of the network.

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