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Field Programmable Gate Array Implementation Based on Lookup Tables Using Reversible and Irreversible Logic

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ABSTRACT: Reversible logic plays a prominent role in the fields of low power computation, cryptography, DSP, and emerging fields of quantum computing. Reversible logic gate is a logic device with one to one mapping between the vectors of n inputs and n outputs. Due to this, loss of information and power dissipation is zero. When CLB's of FPGA, Combinational and sequential circuits which are designed using irreversible logic gates are used, there would be disadvantages like information loss, power dissipation and delay.

This paper proposes an idea of using reversible logic gates to overcome these drawbacks. The idea where each of the components like LUT's, Sequential elements (flipflops), MUX and control circuitry which are required to design the CLB (Control Logic Block) in FPGA has been replaced with reversible logic which there by improves the performance in terms of gates, delay, garbage outputs and power dissipation is supported by providing experimental comparison.

KEYWORDS: Reversible logic gates, FPGA, CLB, Multiplexer (MUX), Flipflops, LUT (Look Up Table).

I. INTRODUCTION

In any irreversible logic circuit like AND, OR, EXOR one bit of information is lost for every computation performed. As per Landauer's principle, any irreversible logic computation results in a considerable generation of heat energy ($kT \ln 2$) for every bit of information loss observed, which makes it difficult to extract the useful information.

The heat energy loss due to n bits = $kT \ln 2$ Joules * n

where k (Boltzman constant) = 1.38×10^{-23} J/k, T - room temperature in kelvin

Hence, if Moore's law is still dominant, then the density of circuit increases which in turn magnify the energy loss. Though modern computations and fabrication process reduced heat loss, physical limitation still persists. Therefore, to overcome this disadvantage in future technology, the architecture of all the logic blocks can be implemented using REVERSIBLE LOGIC.

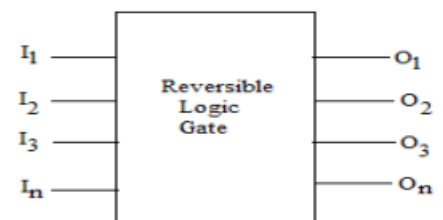
REVERSIBLE LOGIC: A logic function where there is a $n \times n$ injective (one to one) mapping between the input and output, without any repetition is called Reversible logic. So, a $n \times n$ Reversible gate is the one which has n inputs and n outputs for distinct inputs. Reversible logic does not lose information. Hence, zero energy dissipation is possible here, which aids in quantum computations. The most common reversible gates are Toffoli, Fredkin, Peres and Feynman, HNFG, Sayem. In this paper, we present the idea of designing a FPGA using reversible logic.

FPGA: Field Programmable Gate Array is a semiconductor logic chip, which contains many thousands of gates and can be programmed to perform almost any kind of digital logic similar to PLD.

CLB: Configurable Logic Block (CLB) is the basic component of FPGA which is mostly a cluster of BLE (basic logic element) connected through a local routing network. Each BLE consists of a LUT-4 and a Flip-Flop.

The optimised parameters which are used in our comparison between irreversible and reversible CLB are:

Garbage Outputs: Reversibility of the circuit is maintained by disposing the unnecessary outputs of the whole circuit into a single output i.e., garbage output which could be left unused.





Quantum Cost: The total number one-by-one (1x1) reversible gates and two-by-two (2x2) reversible gates used in the reversible circuit design. It should be as low as possible.

Number of Gates: The total number of gates used in a circuit. This should be maintained as minimum as possible.

Delay: The delay of a logic circuit is the maximum number of gates in a path from any input line to any output line, assuming that each gate performs computation in one unit time and all inputs are available before computation begins. Paper is organized as follows. Section II describes the steps involved in implementing the idea. The application of reversible logic to the basic components of CLB in FPGA is given in Section III. Section IV presents simulation results of the RTL schematic of CLB using Veri log HDL in Xilinx. Finally, Section V presents conclusion.

II. RELATED WORK

Large amount of heat is dissipated from High performance chips. This can be a practical limitation to improve the performance of the system. The only physical possible way to improve the performance of the system would be the usage of reversible circuits that conserves the information by uncomputing bits. Reversible computing will also lead to advancement in energy efficiency and also portability. As the circuit element sizes are reduced to atomic size limits in reversible computing, it makes the device more portable.

Lookup tables (LUT) are used to design the architecture of CLB's and I/O pads in FPGA using irreversible logic gates presently.

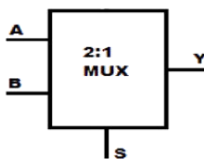
Lookup table gives us the output for the given input. It is a custom-made truth table which has the values according to our FPGA based on our requirements. According to Moore's Law, for every 24 months, the number of transistors on a chip gets doubled which will lead to massive increase in the power loss making it the main disadvantage in future technology.

The first stage of our work implements the components of CLB and I/O block using reversible logic gates. The next stage involves the development of HDL code for the elements and simulation of results in terms of delay, power using Xilinx for both reversible and irreversible CLB. The results testify the effectiveness of reversible logic over irreversible logic.

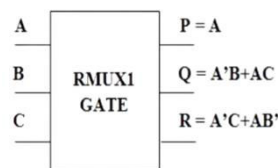
III. METHODOLOGY

The basic components of CLB are 2*1 mux, 4*1 mux, 3 input LUT, and 4 input LUT, SR latch, D flipflop. We would be designing basic components using reversible logic gates.

2*1 Mux - RMUX gate: In this proposed design, reversible multiplexers can be implemented using RMUX1 reversible logic gates. A single RMUX1 gate can be used as 2*1 mux.



Irreversible 2*1 multiplexer



RMUXgate as 2*1 multiplexer

The output expression Q which is a primary output of Reversible 2x1 Multiplexer is given by $Q = A'B + AC$.

The output terminals named with P and R are only used to satisfy the reversibility criteria.

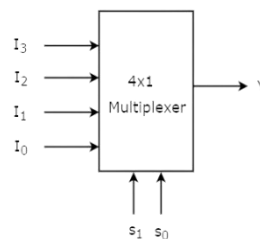
4*1 Mux - MSB gate: In this proposed design, reversible 4*1 multiplexers can be implemented using MSB reversible logic gate. The output $R = B'(A'C \wedge AD) \wedge B(A'E \wedge AF)$ is the primary output of (MSB Gate) reversible 4*1 mux.

When $A=0, B=0$ $R=1(C \wedge 0) \wedge 0=C$

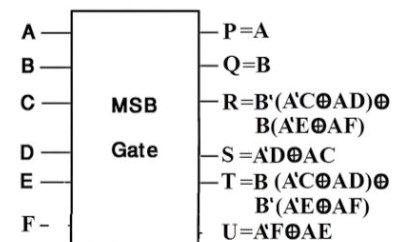
When $A=0, B=1$ $R=0 \wedge 1(E \wedge 0)=E$

When $A=1, B=0$ $R=1(0 \wedge D) \wedge 0=D$

When $A=1, B=1$ $R=0 \wedge 1(0 \wedge F)=F$



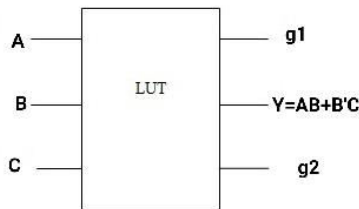
4*1 multiplexer



MSB GATE as 4*1 multiplexer



3- INPUT LUT - RMUX gate: 3 input LUT can be implemented using RMUX as proposed. Two of these can be functional generator outputs and the third input must come from outside the block. The output can be same as that of RMUX gate and the equation will be $Y=AB+B'C$

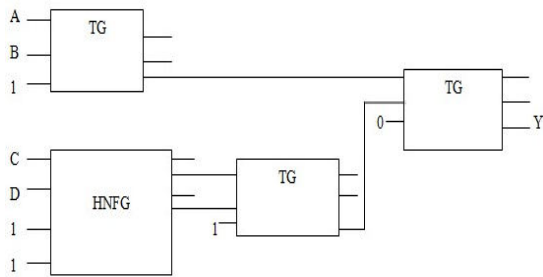


3 - INPUT LUT

A	B	C	Y
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

Truth Table of 3 -INPUT LUT

4-INPUT LUT - TG AND HNF GATE: In this proposed design, a 4 input LUT can be implemented using Toffoli,HNFG gates.The Boolean equation $Y = \sim(A\&B)(C+D)$ is implemented in CLB using LUT.



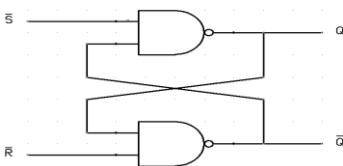
4-INPUT LUT

Input s			Output	Input s			Output		
A	B	C	D	Y	A	B	C	D	Y
0	0	0	0	0	1	0	0	0	0
0	0	0	1	1	1	0	0	1	1
0	0	1	0	1	1	1	1	0	1
0	0	1	1	1	1	0	1	1	1
0	1	0	0	0	1	1	0	0	0
0	1	0	1	1	1	1	0	1	0
0	1	1	0	1	1	1	1	0	0
0	1	1	1	1	1	1	1	1	0

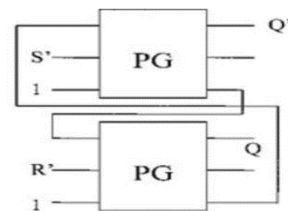
Truth Table of 4-INPUT LUT

SR latch - PERES gate: The reversible SR latch designs are not gated in nature as they donot have clock. In this proposed design. A reversible SR latch can be implemented by using two peres gates.Thecharacteristic equation is $Q+=S+R-$.

From the characteristic equation, we observe that for five input Combinations $(S=0,R=0,Q=1),(S=1,R=0,Q=0),(S=1,R=0,Q=1),(S=1,R=1,Q=0)$ and $(S=1,R=1,Q=1)$ we have $Q+=1$. When $S=1,R=1$ SR latch enters an unstable condition.

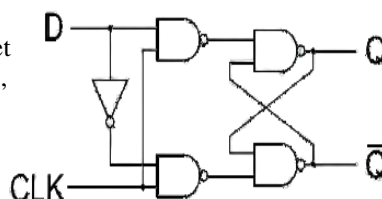


SR LATCH Reversible SR FLIPOP using Peres gates

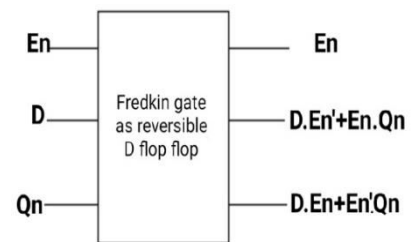


D Flip flop - Fredkin gate:The D flip- flop in digital systems are considered as the basic memory element as D is likewise considered as Delay line element.Inthis proposed design, a reversible D flipflop can be implemented by using a Fredkin gate. The Characteristic equation is $Q_{n+1} = D$.

If we consider $A=En, B=D, C=Q_n$ then we will get $P=En, Q=D, En'+ En.Q_n, R=Q_{n+1}=D.En+En'Q_n$, Where R is the primary output and the other two are garbage outputs



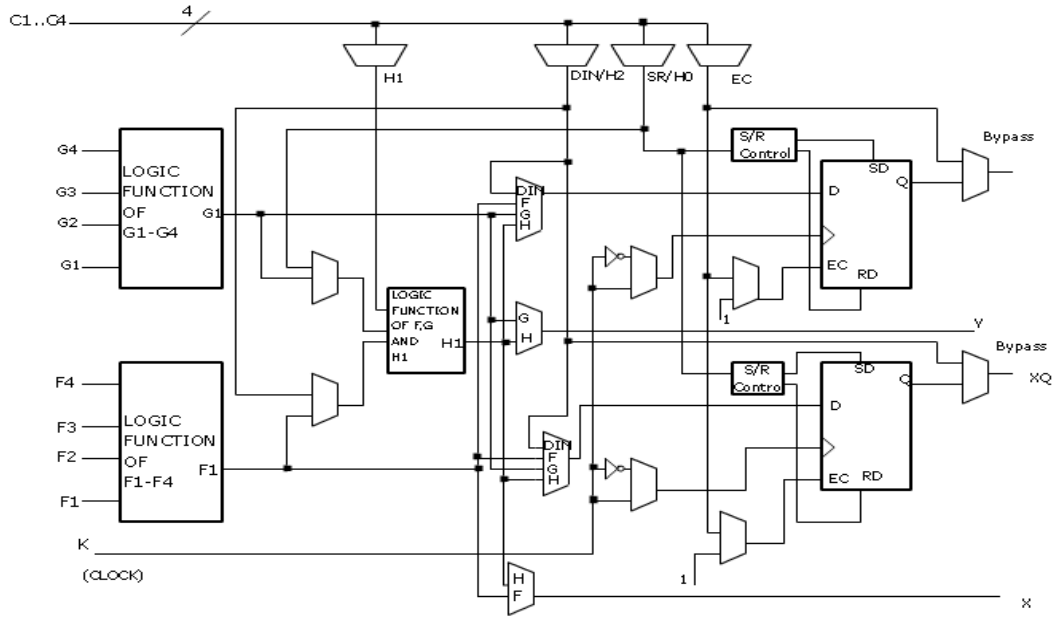
D FLIP FLOP Reversible



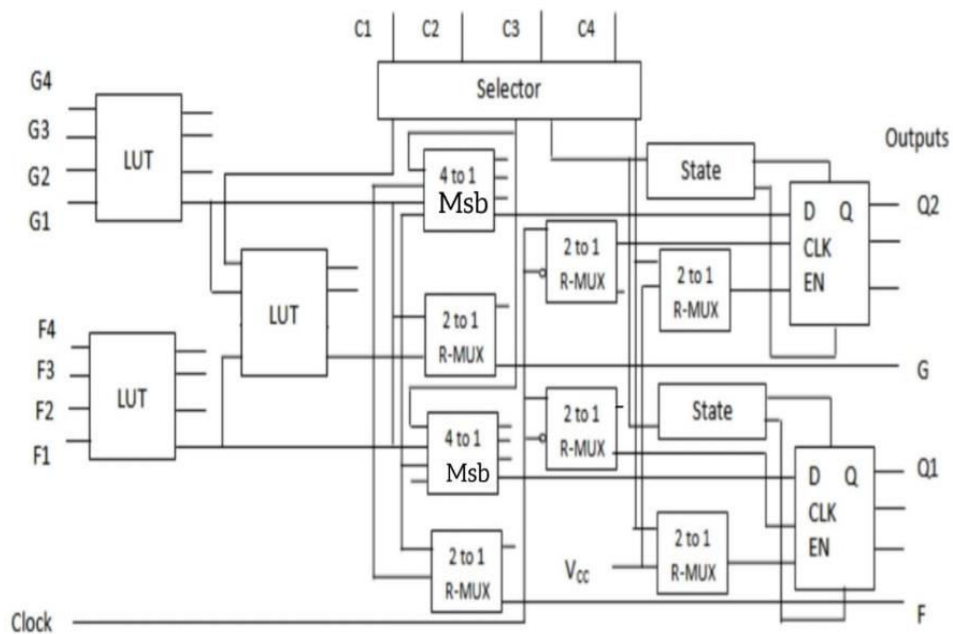
D FLIP FLOP



Reversible and Irreversible CLB: Comparison is made between reversible and irreversible CLB based on delay, power dissipation, number of gates and garbage outputs. Here we implement CLB by using reversible LUT's in the place of function generators, RMUX instead of 2*1 mux, MSB instead of 4*1, Fredkin gate as reversible D flip flop, SR latch using Peres gates.



IRREVERSIBLE CLB



REVERSIBLE CLB

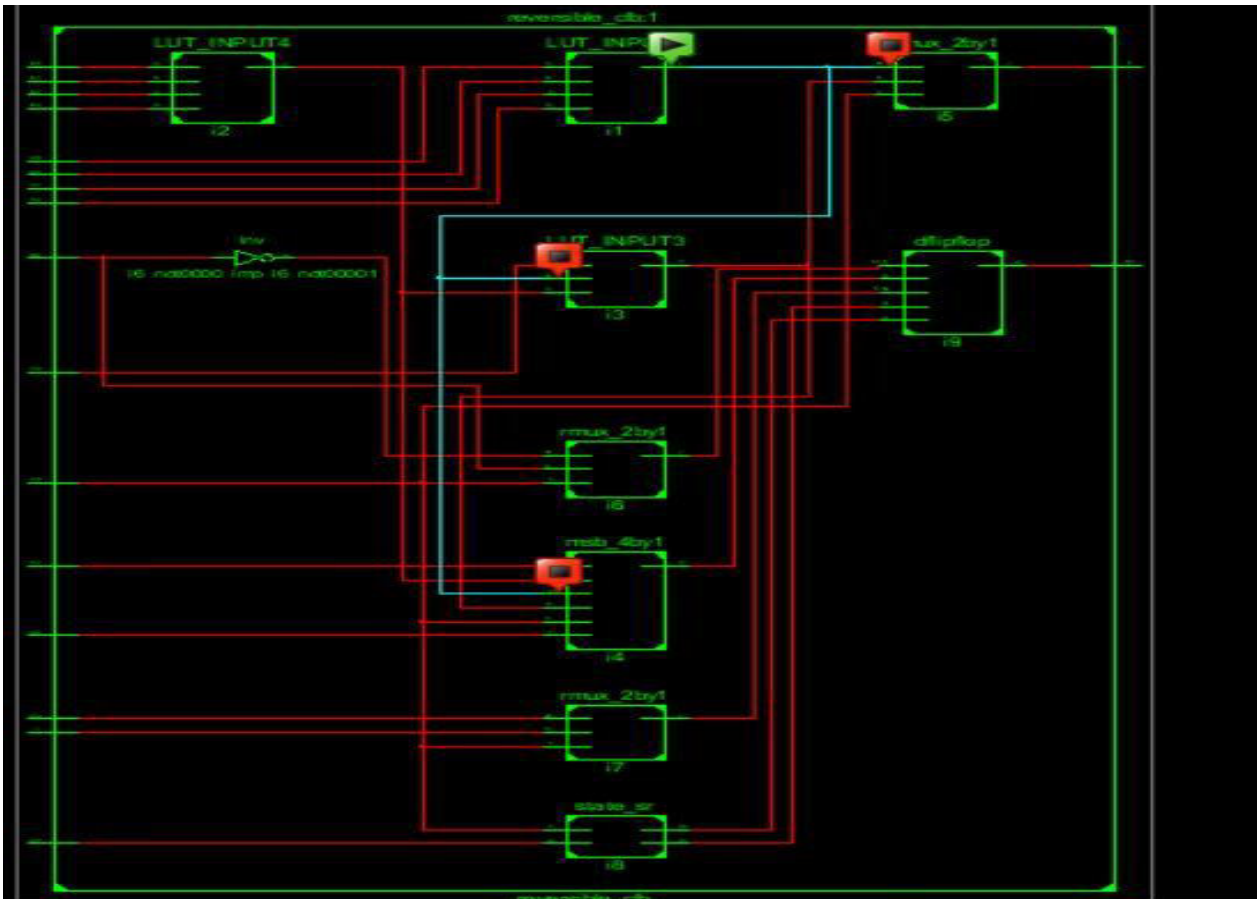


IV. EXPERIMENTAL RESULTS

Register-transfer-level (RTL) abstraction is used in hardware description languages like Verilog to create high-level representations of a circuit.

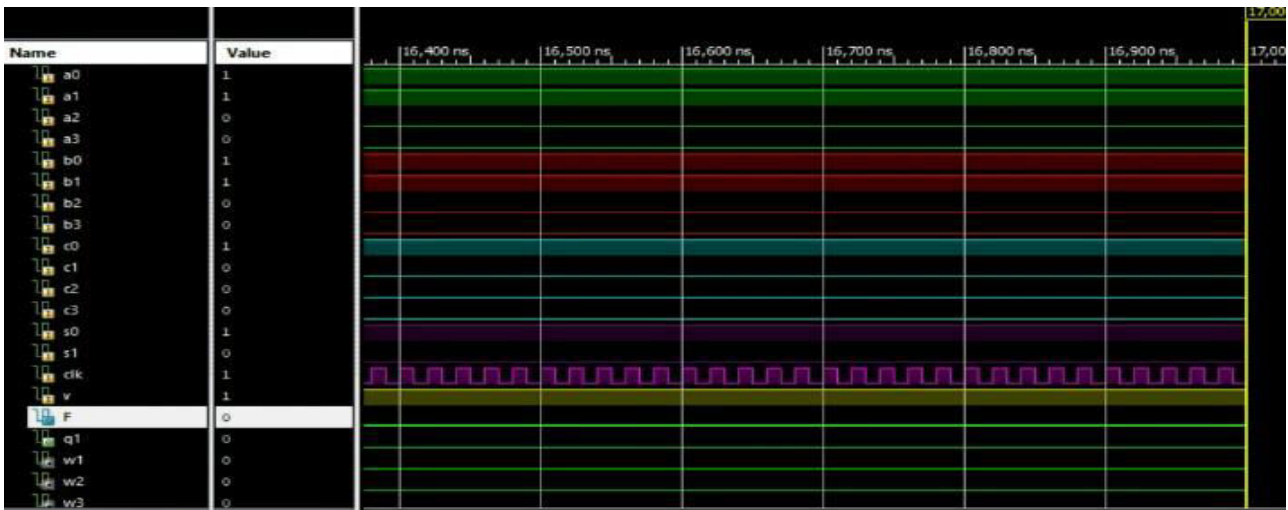
Simulation is the process of using a simulation software (simulator) to verify the functional correctness of a digital design that is modelled using a hardware description language) like Verilog. Xilinx ISE(Integrated Synthesis Environment) is the software tool used here for Synthesis and analysis of HDL designs, enabling the developer to synthesize their designs, perform timing analysis, examine RTL diagrams, simulate design's reaction to different stimuli, and configure the target device with the programmer.

The RTL Schematic of the implemented reversible Configurable Logic Block (CLB) is shown below. It is designed by using reversible 2*1 MUX ,4*1 MUX and D flip-flop and the inputs are transferred to output after performing the logic function by making necessary interconnection through logic gates. This is the final CLB block implemented in the project.



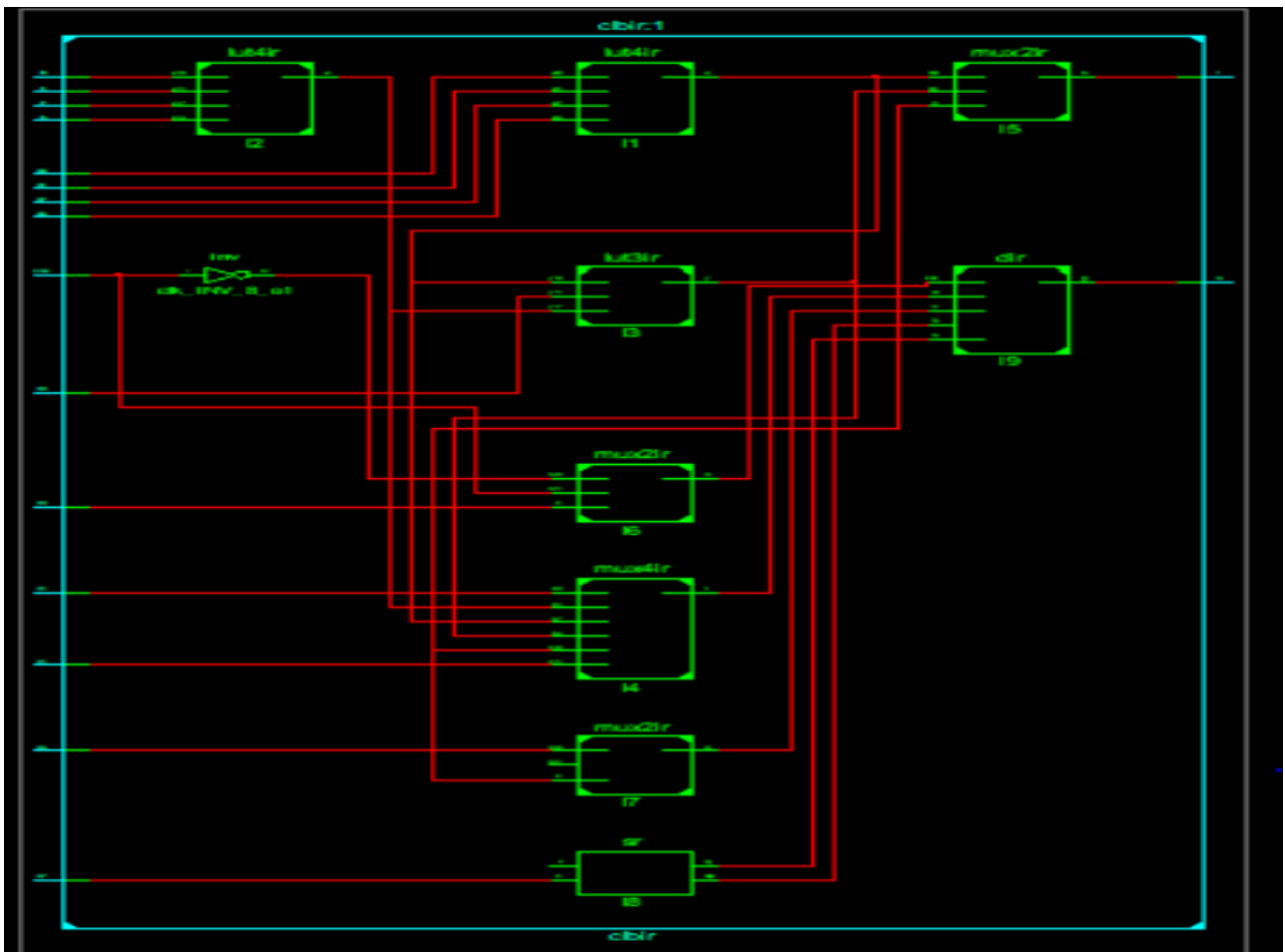
RTLSchematic of reversibleCLB

This is the final function simulation waveform of combinational function implemented in reversible CLB. A four variable Boolean equation $\sim (AB)(C+D)$ is implemented in CLB. For example the input combination A=0, B=1, C=1, D=1 produces and output y=1. It consists of input clock to set/reset the flip-flops. Based on the selection lines from the selector the output of the CLB Block is obtained

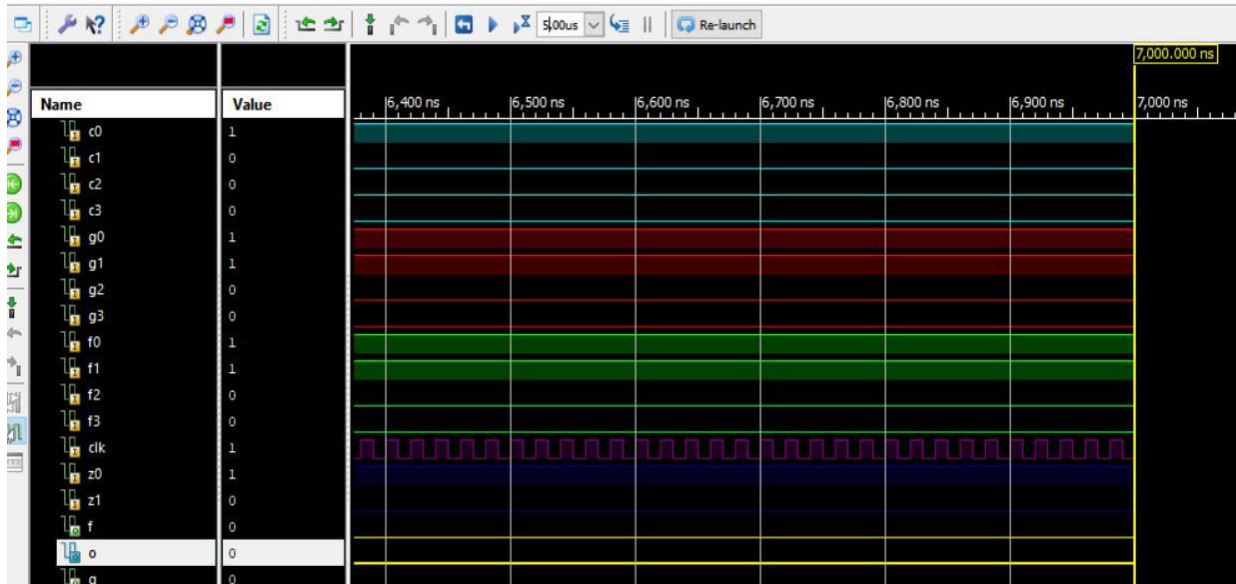


Simulation Waveform of Reversible CLB

The RTL schematic and simulation waveform of Irreversible CLB are shown below :



RTL Schematic of irreversibleCLB



Simulation Waveform of irreversible CLB

Comparison of parameters of reversible gates :

LOGIC DESIGN	GATES	NO OF GATES	GARBAGE OUTPUTS	NO OF LUTS	DELAY(ns)
2*1 MUX	RMUX	1	2	2	6.209
4*1 MUX	MSB	1	5	2	6.55
SR FLIPFLOP	PERES	2	2	2	6.236
JK FLIPFLOP	FREDKIN	2	2	2	6.209
D FLIPFLOP	FREDKIN	1	3	1	4.283
T FLIPFLOP	CNOT FREDKIN	1 1	3	2	6.03
4-INPUT LUT	TG HNF	3 1	8	2	6.209
3-INPUT LUT	RMUX	1	2	1	6.209
CLB			27	2	7.523

TABLE 7.1 COMPARISON PARAMETERS OF REVERSIBLE GATES

Comparison Parameters Of Irreversible Gates :

LOGIC DESIGN	NO OF 4 INPUT LUTS	DELAY(ns)
2*1 MUX	2	7.20
4*1 MUX	2	6.557
SR FLIPFLOP	1	6.39
JK FLIPFLOP	2	7.40
D FLIPFLOP	3	7.383
T FLIPFLOP	2	7.44
4-INPUT LUT	1	6.209
3-INPUT LUT	1	6.209
CLB	2	7.579

TABLE 7.2 COMPARISON PARAMETERS OF IRREVERSIBLE GATES



V. CONCLUSION

We have successfully implemented the FPGA based on Look Up Table using Reversible logic which thereby will reduce the known drawbacks we face when irreversible logic is used. We have compared the performance of Reversible CLB with irreversible CLB and reached the conclusion that delay, power dissipation and information loss is greatly minimized when reversible logic devices are used.

Thus, Reversible logic computing is considered as a great advancement in the field of VLSI. Therefore, Reversible computing may have applications in those areas which require high energy efficiency, speed and performance, like

- Low power CMOS.
- Quantum computer.
- Nanotechnology.
- Optical computing.
- DNA computing.
- Computer graphics.
- Communication.

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