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Self-Checking Bubble Sort using Berger Code

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ABSTRACT: The Berger code have the lowest redundancy of any separable code for detecting all possible unidirectional errors [1]. This Paper presents a design of self-checking parallel bubble sort using Berger code. discuss compare the information and reorder the bits use the Berger code for current Error detection (CED), multi magnitude comparator for two inputs comparing the entry data bits ,checks using (CED) after implementing sorting bubble algorithm for the entry data bits.

KEYWORDS: Berger code, Self-checking, Magnitude Comparator, Bubble sort, Concurrent error detection

I.INTRODUCTION

Due to the rapid development of integrated electronic circuits, and the increase in their wide use in modern industries and the small size of integrated circuits, which required the creation of a reliable error detection technique, on the line using Berger code. In this paper, we used the Berger code is to detect all undetected error in the Bubble sort.

II.CONCURRENT ERROR DETECTION (CED)

On-line error detection techniques have been widely used in commercial digital systems since the 1960's [2]. Concurrent error detection (CED) is very important in highly dependable computing systems. As technology advances to deep sub-micron levels, circuits are more susceptible to errors. CED techniques can be used to detect permanent and transient errors in these circuits. The general structure of concurrent error detection is shown in figure 1.0

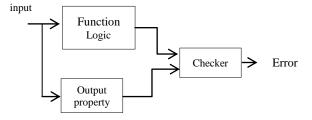


Figure 2.0 CED Circuit Structure

III.MAGNITUDE COMPARATOR

A magnitude comparator is a combinational circuit that compares two given numbers and determines whether one is equal to, less than or greater than the other [2] The outcome of the comparison is specified by three binary variables that indicate whether A>B, A=B, or A<B.

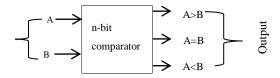


Figure 3.0 Block diagram of One Bit



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This is useful if we want to compare two variables and want to produce an output when any of the above three conditions are achieved

IV.BERGER CODE

The Berger codes can detect all unidirectional errors, The Berger code requires the fewest number of check bits amongst all the separable codes the detect unidirectional errors.[3] A Berger code word of length n has/information bits and k check bits.

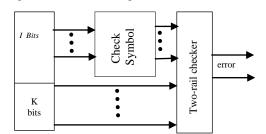


Figure (4.0) TSC Berger Code Checker

where k=[log2(l+1)]

The code word therefore has n=1+k digits.

The k check bits are formed from a binary number which corresponds to the number of ones in the information bits being complemented bit by bit.[3]

V.BUBBLE SORT ALGORITHM

Sorting is an important of many high-performance applications [5]. The main reason for sorting being so useful is that it is much easier for people to handle data when it is sorted compared with unsorted data. Bubble-sort is the slowest algorithm for sorting but it is heavily used, as it is easy to implement, it is far to use on large, unordered data sets. Donald Knuth [6]. In Bubble-sort, compare each pair of adjacent values. in increasing order if the second value is less than the first value then we swap these two values. Otherwise, will go to the next pair. [4]

VI. BUBBLE SORT PSEUDOCODE

- 1-Given with an input array which is supposed to be sorted in ascending order.
- 2-Sart with the first element index i=0 index and check if the element presents at i+1 is greater than swap the elements at index i and i+1.
- 3-If above is not the case, then no swapping will take place.
- 4- Increment the index i, and go back to step 1. Repeat this step until the array is exhausted.
- 5- Ignore the last index as it is already sorted.
- 6-Now the largest element will be at the last index of the array.
- 7-Again set i=0 and continue with the same steps that will eventually place second largest at second last place in the array. Now the last 2 indexes of the array are sorted.

Number of modules=
$$\frac{n-1}{p-1}$$
 (6.1)



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VII. TWO-RAIL CHECKER

Two-rail checker unit (TRC) is used to compare two complementary code words. The checker determines whether the output of the functional circuit is a valid or invalid code word. Two-rail checker circuit has two groups of inputs:

$$(x_n, \dots, x_2, x_1)_{\text{and}} (y_n, \dots, y_2, y_1)_{\perp}$$

It also has two outputs: f and g. The signals observed on the outputs should always be complementary, that is a1-out-of-2 code, if and only if every pair (x_j, y_j) is also complementary for all $(1 \le j \le n)_{[7,8]}$. Consider a two-rail checker with n=2, as shown in Figure (3.0). The two input groups are (x_2, x_1) and (y_2, y_1) . In a non-error situation where $(y_1 = x_1)_{and} (y_2 = x_2)_{and} (y_2 = x_2)_{and}$

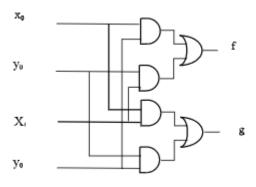


Figure 7.0: Check Symbol Generator

Although a two-rail checker for an arbitrary number of input pairs may be designed using two-level AND-OR logic, it is more efficiently realized as a tree by interconnecting the checker modules with two input pairs. In general a multilevel tree realization for a checker with n input pairs formed by interconnecting checker modules with p input pairs [8].

Number of module levels $\lceil \log_2 n \rceil$. (7.1)

Figure (5.3) shows as an example a two-rail checker with two input groups $(a_5, a_4, a_3, a_2, a_1)$ and $(b_5, b_4, b_3, b_2, b_1)$, that means n=5. It is formed by interconnecting checker modules with p=2 input pairs. Number of modules and module levels could be obtained from:

Number of modules =
$$\frac{5-1}{2-1} = 4$$

Number of module levels = $\lceil \log_2 5 \rceil = 3$



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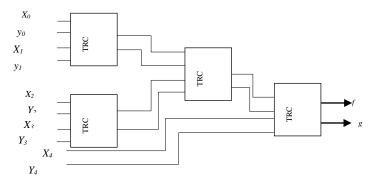


Figure (7.1) Check Symbol Generator

VIII. PARALLEL BUBBLE SORT CIRCUIT

Bubble sort Algorithm implemented in hardware the circuit was designed as shown in figure (7.0) for five bit inputs where each cell have two bit inputs, every cell consist of two comparator and two 2:1 Mux, comparator that compare between two input bits in our circuit we use greater than A>B comparator output connected with select pins of two Mux, one of select pins will be high that pointed to the greater value vice versa.

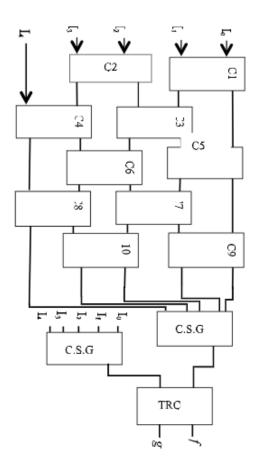


Figure 8.0 Bubble sort cells data using Berger Code



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Every cell in Previousfigure 7.0 consist of the circuit shown in figure (7.1) it's consisting of one comparator connected its output line with two Muxthat is perform the compare and swapping input data. The I0,I1,I2,I3 and I4 will passed data into cells, I0 and I1 will be inputs in parallel

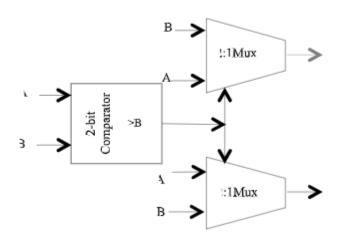


Figure 8.1 comparator and swap circuit

that I0 and I1 are connected to cell (C1). The entered data is processed inside the cell by comparison to find the largest value and a substitution, at the same time, the data entered in cell No. 2 processed first stage and I4 with the second output of cell No. 2 are processed as inputs to cell No. 4 in second stage, the first output of C No1connected with C5,upper C3 output connected to C5,C6 in stage three in every cell there is comparing the entered data and substitution up to the five stage the output lines connected (sorted bits) to C.S.G also the original data I0, I1, I2, I3 and I4 connected to another C.S.G. Outputs s of check symbol circuits are inputs of five pair Two rail circuit, if the result of Two Rail circuit 11 or 00 there is error in the data otherwise meaning there is no error in data.

IX.CONCLUSION

In this paper we presented Self-checking Bubble sort using Berger Code. The following points are concluded:

- 1. A Berger code is can detect all unidirectional errors. Unidirectional errors are errors that only flip ones into zeroes or only zeroes into ones, such as in asymmetric channels. The check bits of Berger codes are computed by counting all the zeroes in the information word, and expressing that number in natural binary.[10]. Berger codes cannot correct any error
- 2. For small inputs, bubble sort is a feasible solution and it is easy to implement. In each round, the largest(or smallest) sample is selected by series of comparisons. The algorithm requires N comparison and switching events in the first round when the input size is N,N-1 events in the second round,N-2 events in the third round and so on until the complete sorted result is generated. The main disadvantage is the amount of time it takes. It is highly inefficient for large data sets, with a running time of O(n2).
- 3. All originalentereddata (unsorted data), sorted data checkers implemented to be fault secure or totally self-checking.

REFERENCES

- [1] Chip test Architectures Nanometer Desginfor Testability by LoungTerngWang, Charles E Stroud, Nur A. Touba@2008 by Elsevier Inc
- [2] Digital Electronics Principls, Devices and Applications, By Anil K. Maini, 2007 John Wiley & Sons, Ltd .ISBN: 978-0-470-03214-5
- [3] Advanced simulation and test methodollogies for VLSI design, Gordon Russell and Lan L.Sayers
- [4] Problem Solving in Data Structures& Algorithms using C++ First Edition, by Hemant Jain Copyright 2016 by HEMANT JAIN



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- [5] Eduard Petlenkov, Neural networkbased identification and control of nonlinear systems: ANARX Model Based Approch 2007
- [6] Lea ElmikInformationa; Modelling of a Communication office.1992
- [7] Martin Omana, Daniele Rossi, Cecilia Metra," Low Cost and High Speed Embedded Two-Rail Code Checker", IEEE Transaction on computer, Vol. 54, No. 2, February 2005, pp. 153-164
- [8] Parag K. Lala, "Self checking and Fault tolerance digital Design", Morgan Kaufmann Publisher, 2001.
- [9] Martin Omana, Daniele Rossi, Cecilia Metra," Low Cost and High Speed Embedded Two-Rail Code Checker", IEEE Transaction on computer, Vol. 54, No. 2, February 2005, pp. 153-164.
- [10] J. M. Berger (March 1961). "A note on an error detection code for asymmetric channels". Information and Control. 4 (1): 68–73. doi:10.1016/S0019-9958(61)80037-5

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