



e-ISSN: 2319-8753 | p-ISSN: 2347-6710

IJIRSET

International Journal of Innovative Research in
SCIENCE | ENGINEERING | TECHNOLOGY



INTERNATIONAL JOURNAL OF INNOVATIVE RESEARCH

IN SCIENCE | ENGINEERING | TECHNOLOGY

Volume 12, Issue 2, February 2023

ISSN INTERNATIONAL
STANDARD
SERIAL
NUMBER
INDIA

Impact Factor: 8.118



9940 572 462



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Design and Analysis of High Speed Wallace Tree Multiplier using Parallel Prefix Adders for VLSI Circuit Designs

Shashi Bhushan Chauhan¹, Satyarth Tiwari²

P.G Student, Department of Electronics & Communication Engineering, Bhabha University, Madhya Pradesh, India¹

Assistant Professor, Department of Electronics & Communication Engineering, Bhabha University,
Madhya Pradesh, India²

ABSTRACT: Major operation block in any processing unit is a multiplier. There are many multiplication algorithms are proposed, by using which multiplier structure can be designed. Among various multiplication algorithms, Wallace tree multiplication algorithm is beneficial in terms of speed of operation. With the advancement of technology, demand for circuits with high speed and low area is increasing. In order to improve the speed of Wallace tree multiplier without degrading its area parameter, a new structure of Wallace tree multiplier is proposed in this paper. In the proposed structure, the final addition stage of partial products is performed by parallel prefix adders (PPAs). In this paper, five Wallace tree multiplier structures are proposed using Kogge stone adder, Sklansky adder, Brent Kung adder, Ladner Fischer adder and Han carlson adder. All the multiplier structures are designed using Verilog HDL in Xilinx 13.2 design suite. The proposed structures are simulated using ISIM simulator and synthesized using XST synthesizer. The proposed designs are analyzed with respect to traditional multiplier design in terms of area (No. of LUTs) and delay (ns).

KEYWORDS: Wallace tree multiplier, Parallel Prefix adders(PPAs), Kogge Stone adder, Sklansky adder, Brent-Kung adder, Ladner Fischer adder, Han Carlslon adder.

I. INTRODUCTION

At present, the technology is advancing very rapidly in very short duration of time. The circuits being design have some billions of components with low area, high speed and low power consumption. Hence area, speed and power plays crucial role in the design of any circuit [1], [2]. In order to satisfy the current trend demand a circuit must be designed with low area and less delay constraints. Arithmetic units are major blocks in any processing units which perform various arithmetic operations [3]. Multiplication operation is important among all arithmetic operations. Several multiplication algorithms are studied in literature survey of multiplier designs like Binary multiplier, array multiplier, Booth's multiplier, Dadda multiplier, Wallace tree multiplier [4]. Wallace tree multiplier is advantageous in different types of multipliers[5].

The operation of Wallace tree multiplier is same in the first stage of multiplication which is generating partial products. In the second stage, Wallace tree multiplier adds first three rows partial products. Then the generated sum and carry are added with the next row of partial products. This addition process continues until the generation of final products. For this row-wise addition process half and full adders are employed. Thus, adders are playing a very important role in generation of final product terms. The speed of addition is going to affect the operation of the multiplication.

In order to improve the performance of multiplication operation, the adder structure used in design of Wallace tree multiplier has a major role. In this paper, a new structure of Wallace tree multiplier is proposed in which PPAs are used to add final row of partial products with the previous stage generated sum and carry out terms to generate final product terms. The PPAs are designs which are originally derived from carry look ahead adder concept of generating and propagating of carry bits.

In PPAs, a carry generation tree is present which generates carry for all preceding stages which improves the speed of operation. The carry generation tree mainly consists of two components-black cell and grey cell. The black cell and grey cell are interconnected to form carry tree network. Carry generation tree block is also called as parallel carry generation block as it generates carry bits for all stages at a time parallel[6]. There are different types of PPAs[7] whose classification mainly depends on two factors-

- i) Number of black and grey cells in carry generation tree

ii) Interconnection of black and grey cells in carry generation tree.

Kogge stone adder, Sklansky adder, Brent-Kung adder, Ladner-Fischer adder and Han Carlson adder are some of the PPAs used in the design of proposed Wallace tree multiplier in this paper. This paper is organized as into various sections—section II explains the in detailed operation of traditional Wallace tree multiplier. Section III is composed of many sub sections which describes in depth operation of PPA, different PPAs used in the design of multiplier and the structure of proposed multiplier using PPAs. The result analysis is clearly explained in section IV. Section V is conclusion and future scope of design proposed in this paper.

II. TRADITIONAL WALLACE TREE MULTIPLIER

Most extensively used multiplier design in many processors and memory units is Wallace tree structure[4]. The Wallace tree multiplication process majorly has two phases. In phase 1, the input numbers are applied to AND gate to produce partial products. These partial products are added in step by step process by using half and full adders in phase 2 to obtain final product output. In detailed multiplication process of Wallace tree multiplier is explained through Fig.1 for input size of 4-bits.

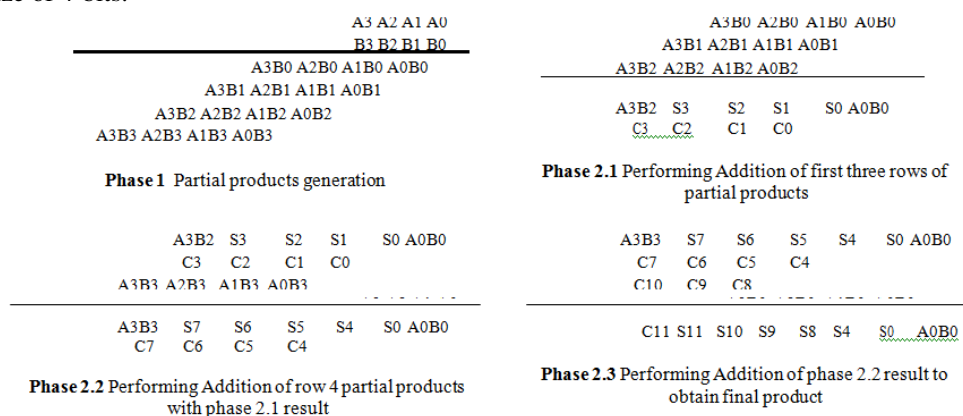


Fig.1. Various Phases of multiplication in a Wallace tree multiplier

The phase 1 comprises of generation of partial products through multiplying every bit of given input numbers with each other. Four rows of partial products are generated as the size of input is 4- bits. The phase 2 comprises of many sub phases of addition of the partial products obtained in phase. The addition operation is carried out using half and full adders. Initially in phase 2, the addition operation is performed on first three rows of partial products generated in phase 1 which generates result of two rows having sum terms in first row and carry terms in second row. Then, the last row of partial products of phase 1 result is added with the sum and carry row which again result two rows comprising of one sum row and one carry row. To acquire final product, the sum and carry row are added.

In entire process of multiplication, addition process holds major role. To perform fast addition, carry must be propagated quickly. A Wallace tree multiplier using Carry select adder designed in [8]. But, carry propagation delay is more in this existing methodology which is the major drawback. To prevail over this drawback, Parallel prefix adders are used in place of half and full adders in final stage of addition in phase 2 of this multiplier. The main motivation of this proposed design is to achieve Wallace tree multiplier architecture with high speed than the existing designs.

III. PROPOSED WALLACE TREE MULTIPLIER

A. Parallel Prefix adders:

In this paper, Wallace tree multiplier structure is modified by using parallel prefix adders to add partial products in final phase addition process to obtain final product. The reason behind to use PPA in place of full adders is to improve the speed of operation. In PPA, the carry input for the next bits is generated at a time with the help of parallel prefix carry tree which consists of black cells and grey cells. There are many types of PPAs are present whose basic design idea is originated from carry look ahead adder. The PPA consists of three main blocks as shown in fig 2. In first block which is also called as pre-processing block, propagate(Pi) and generate(Gi) signals are generated by

$$P_i = A \oplus B$$

$$G_i = A \text{ AND } B \quad \text{Where A and B are input bits.}$$

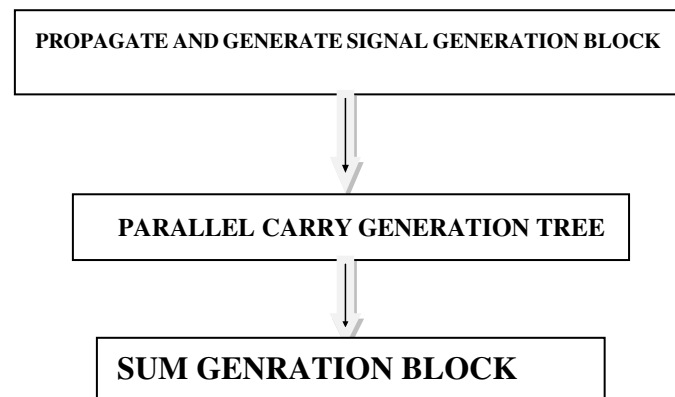


Fig. 2. Parallel prefix adder block diagram

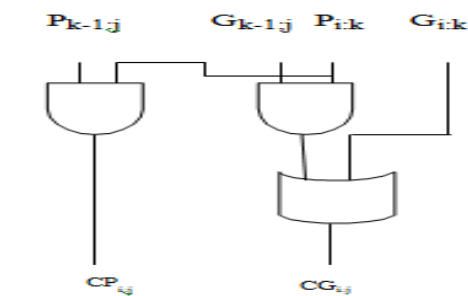


Fig.3. Black cell

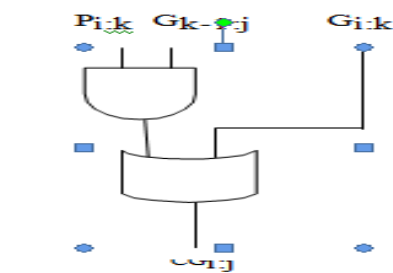


Fig.4. Grey cell

The second block is parallel carry generation tree which generates carry bits for all input bits with the help of grey and black cell to which inputs are P_i and G_i signals generated in first block. The black cell is used to calculate carry generate and propagate signals by

$$CP_{i,j} = P_{k-1,j} \text{ and } P_{i,k}$$

$$CG_{i,j} = G_{i,k+1} \text{ or } (P_{i,k} \text{ and } G_{k-1,j})$$

The grey cell used to calculate only carry generate signal by $CG_{i,j} = G_{i,k+1} \text{ or } (P_{i,k} \text{ and } G_{k-1,j})$

The third block is sum generation block used to generate sum by performing XOR operation of propagate signal and carry signal generated from the block 2 i.e.

$$S_i = P_i \text{ XOR } C_{i-1}$$

In this paper, five different PPAs are used to design Wallace tree multiplier. The five different PPAs are - 1.Kogge stone adder 2.Sklansky adder 3.Brent Kung adder 4.Han Carlson adder and 5. Ladner Fischer adder. These five adders' structures are same only the second block varies in terms of black and grey cells and their interconnections.

a) Kogge stone adder:

Kogge Stone adder is very attractive for high-speed applications which come at the cost of high area and more power [9]-[14]. The delay of the structure is given by $\log_2 n$ with $[n(\log_2 n) - n + 1]$ computation nodes. This adder has regular layout and a controlled fan-out of two. The drawback of this adder is designed circuit will be complex with large number of interconnects. Fig.6. shows 16-bit Kogge stone adder structure which consists of 34 black cells and 15 grey cells.

b) *Sklansky adder:*

The structure of carry prefix network have minimum logic depth but at the cost of high fan out for some computation nodes. The delay of the structure is given by $\log_2 n$ with $n/2 \log_2 n$ computation nodes. This adder fan out increases hugely from the inputs to outputs along the critical path leading for large amount of latency[14]. Due to this as the number of input bits increases, adder performance degrades. Fig.7. shows 16-bit Sklansky adder structure which consists of 17 black cells and 15 grey cells which implies its area also less when compared to Kogge stone adder but the fan out of computation node is increasing which increases latency in adder operation.

C) *Brent Kung adder:*

This adder has less computation nodes but hold maximum depth which accounts for increased latency[10]- [16]. The interconnection complexity of black and grey cells is less when compared to Kogge stone adder. The delay of the structure is given by $[2(\log_2 n)-2]$ with $[2n-2-\log_2 n]$ computation nodes. Fig.8. shows 16-bit Brent Kung adder structure which consists of 12 black cells and 15 grey cells which implies its area also less when compared to Kogge stone and Sklansky adders. The structure of this adder is simpler when compared to Kogge stone adder. Also fan out for this structure is also less when compared to Sklansky adder.

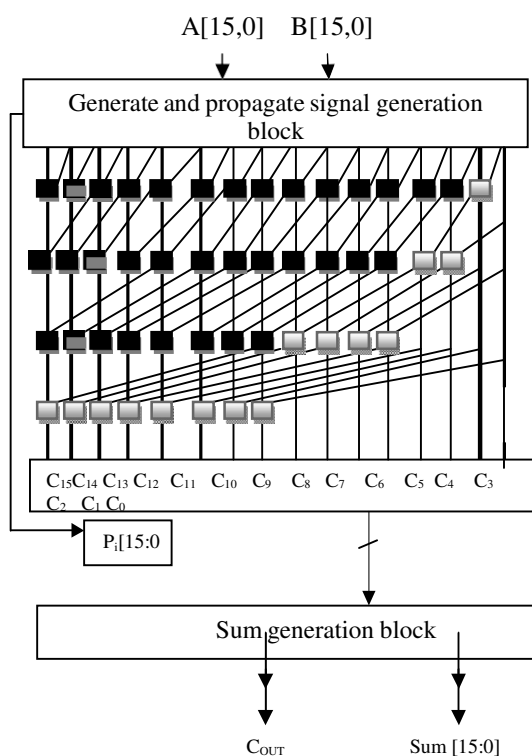


Fig 6: Kogge Stone adder

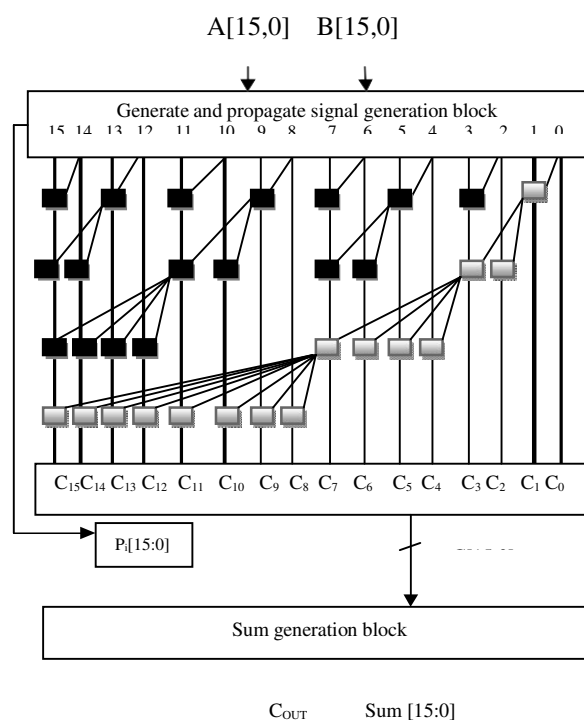


Fig 7 Sklansky Adder

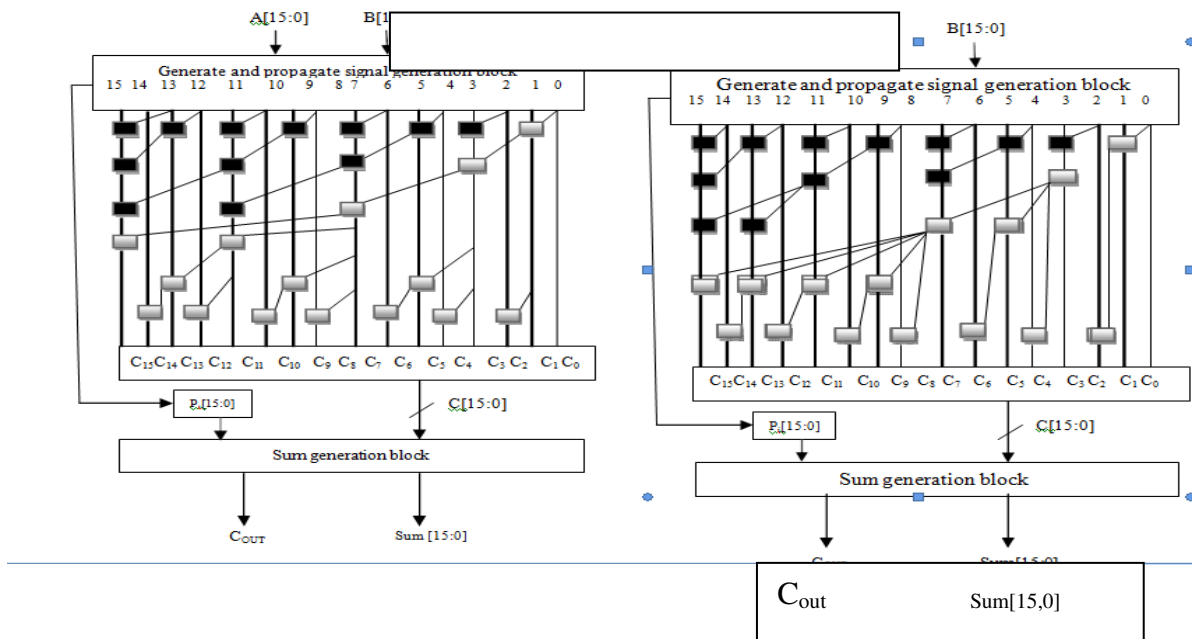


Fig.8. Structure of 16-bit Brent kung adder

Fig.10. Structure of 16-bit Ladner Fischer adder

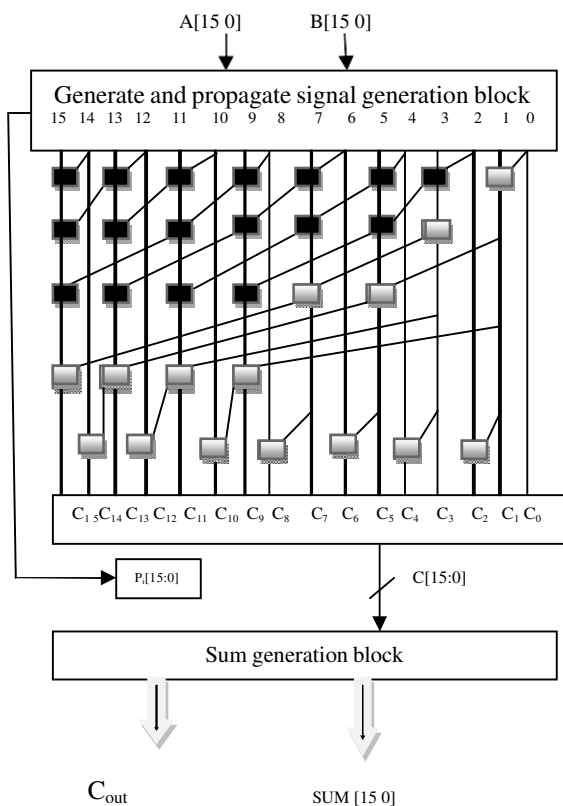


Fig 9. Structure of 16-bit Han Carlson adder

a) Ladner Fischer adder

This adder is designed from Sklansky adder design having delay of $(\log_2 n)+1$ with $[(n/2)\log_2 n]$ computation nodes[14]. Fig.10. shows 16-bit Ladner Fishner adder structure which consists of 12 black cells and 15 grey cells which is same as in case of Brent Kung adder but it has less number of stages then Brent kung adder so this adder will have more speed then brent Kung adder.

b) Han Carlson adder:

This adder is combination of Kogge stone and Brent Kung adder which is nothing but this adder is a hybrid design[17]. The second block consists of five stages in which the first stage is like Brent Kung adder and the middle three stages are like Kogge stone adder. The delay of the structure is given by $(\log_2 n)+1$ with $[(n/2)\log_2 n]$ computation nodes. Fig.9. shows 16-bit Han Carlson adder structure which consists of 17 black cells and 15 grey cells which implies its area and interconnection complexity is less then Kogge stone adder but its logic depth is more which increases delay.

B) Wallace tree multiplier using PPAs:

In this paper, four different Wallace Tree multiplier structures are designed using four different PPAs namely Kogge stone adder, Brent Kung adder, Han Carlson adder and Ladner Fischer adder. These adders are used in final addition process in phase 2 to improve the performance of the operation of the multiplier The multiplier operation is same which is performed in two phases as explained in section 2. In phase 1, partial products are generated with the help of AND gates. In Phase 2 partial products generated in phase 1 are added in step by step approach using half and full adders. In proposed design the final phase of addition of partial products in phase 2 is performed using PPA.

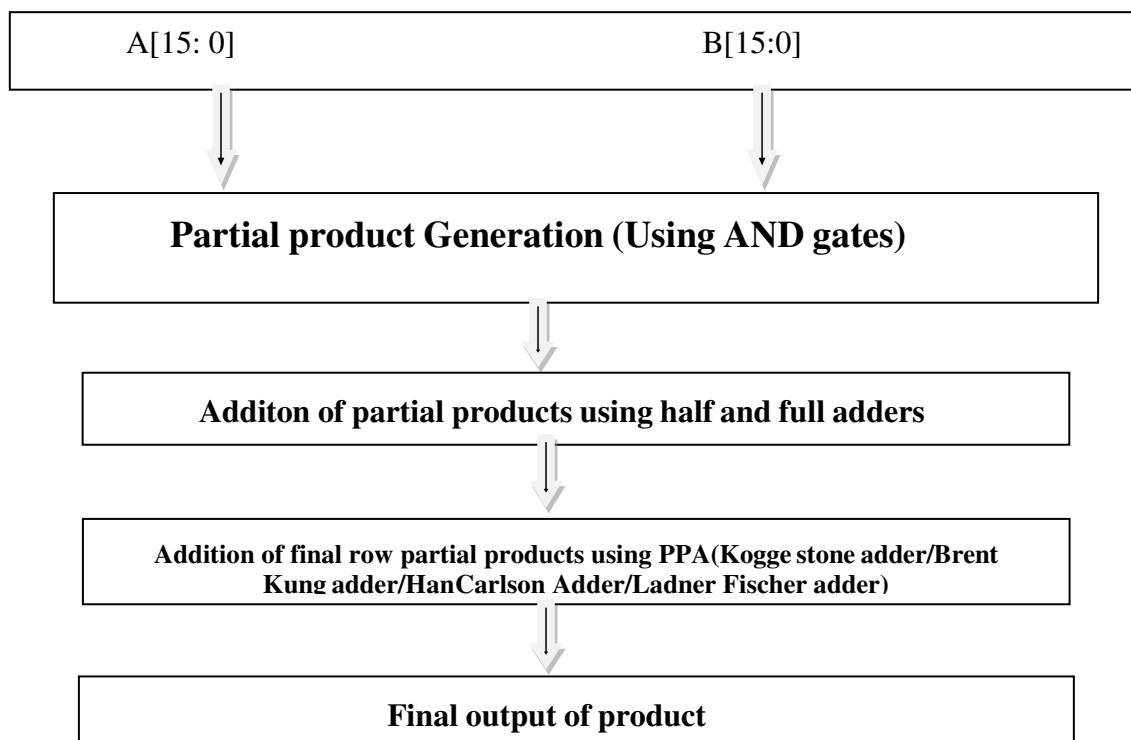


Fig.11. Block diagram of proposed Wallace tree multiplier using PPAs

IV. SIMULATED AND SYNTHESIZED RESULT ANALYSIS

Five Wallace tree multiplier structures using five different PPA's (Sklansky adder, Kogge stone adder, Brent Kung adder, Han Carlson adder and Ladner Fischer adder) are designed for input size of 16-bits in this paper using Verilog HDL. All the designed multipliers are simulated and synthesized using Xilinx ISE 13.2. The simulation waveforms for proposed multipliers are shown in fig12- fig16. The proposed multiplier's synthesis result is compared with the traditional Wallace tree multiplier in terms of area (number of LUTs) and delay (ns).

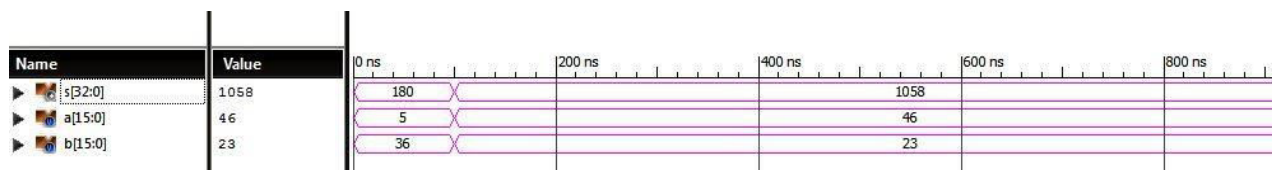


Fig.12. Simulation waveform for 16-bit Wallace tree multiplier using Kogge stone adder

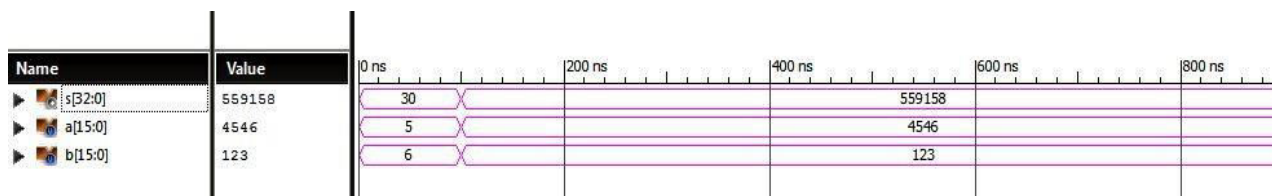


Fig.13. Simulation waveform for 16-bit Wallace tree multiplier using Sklansky adder

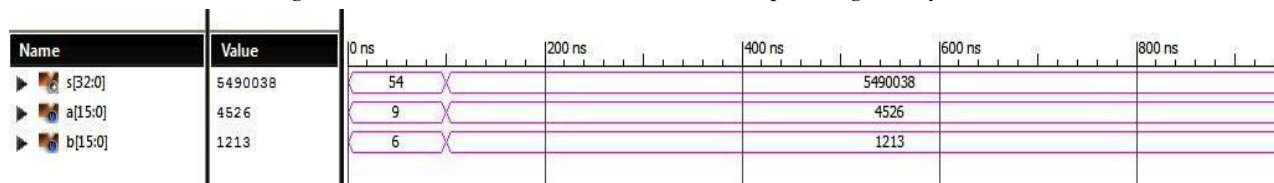


Fig.14. Simulation waveform for 16-bit Wallace tree multiplier using Brent Kung adder

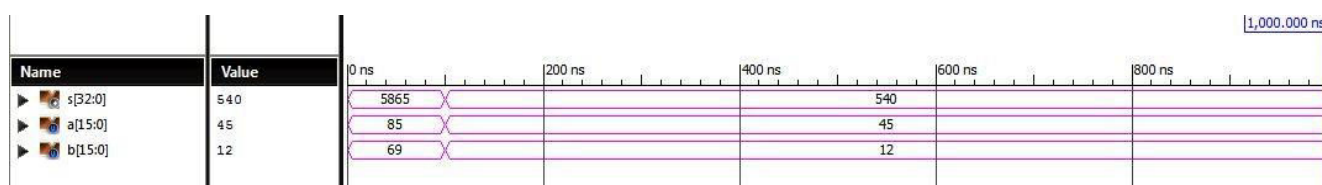


Fig.15. Simulation waveform for 16-bit Wallace tree multiplier using Ladner Fischer adder

Table 1. Area(No. of LUTs) and delay(ns) of different Wallace tree multiplier structures using different PPAs

Input size	Multiplier structure	Area(No. of LUTs)	Delay(ns)
16-bit	Traditional Wallace tree multiplier	590	36.7
	Wallace tree multiplier using Kogge stone adder	634	29.44
	Wallace tree multiplier using Sklansky adder	599	30
	Wallace tree multiplier using Brent kung adder	598	32.37
	Wallace tree multiplier using Ladner fischer adder	596	31.57
	Wallace tree multiplier using Han carlson adder	601	30.19

As shown in table 1, total six multipliers i.e., the proposed multipliers using PPAs in this paper are five and one is traditional multiplier are synthesized using Xilinx XST synthesizer. The synthesis report consists of area details in terms of number of LUTs occupied and delay in terms of nano seconds. From table 1, it can be seen that Wallace tree multiplier using Kogge stone adder is having least delay but it has more number of LUTs occupied when compared to other structures. The traditional multiplier is having highest delay and number of LUTs occupied is less when compared to other adders but the

difference of LUTs of proposed and traditional structure is not more which can be ignored. The Wallace tree multiplier using ladner fischer adder is having least number of LUTs occupied where as its delay is medium i.e, 31.57ns which is less when compared with the traditional structure

V. CONCLUSION AND FUTURESOCPE

Total six multiplier structures are designed in this paper in which five are proposed Wallace tree multipliers using five different PPAs and one is traditional Wallace tree multiplier. In terms of delay parameter it is achieved where as for area parameter the difference of LUTs occupied by traditional and proposed structures is not more which intend that area parameter is also achieved up to some extent which can be seen in table 1. In proposed multipliers, Wallace tree multiplier using Kogge stone adder is having least delay but its area parameter is high when compared to other structures of multipliers in this paper. In terms of area parameter, Wallace tree multiplier using Ladner fischer adder is having least area among proposed structures.

So it can be concluded that the proposed multipliers are better in delay and area when compared with the traditional multiplier structure. Among the proposed structures, Wallace tree multiplier using Ladner fischer adder can be used for application circuits which require less area and speed of the circuits will also be in medium. Whereas for high speed application circuits, Wallace tree multiplier using Kogge stone adder can be used but costing little bit more area when compared to other proposed structures. The proposed multiplier structures can be used in high speed and low area application circuits basing on requirement. As future scope of this work, the multiplier structures can be designed by increasing input size(I.e. 32-bit,64-bit.....). By designing the multiplier circuit with higher input size may lead to multiplier structure with less number of LUTs and also better delay value can be achieved.

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