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Design of High-Speed Fir Filter Using Ladner Fischer Adder and Hybrid Multiplier

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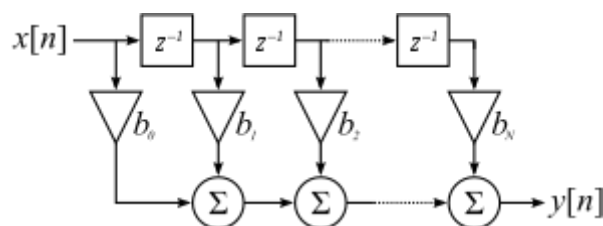
ABSTRACT: The finite impulse response (FIR) filter is a commonly used digital signal processing (DSP) algorithm for filtering and processing signals in various applications. An FIR filter is one that does not have any feedback in its equation. This can be advantageous because a FIR filter is inherently stable and also has the advantage of being able to produce linear phases. If a given application necessitates linear phases, the choice is clear: a FIR filter is required. The fundamental disadvantage of a digital FIR filter is its execution time. Because the filter does not provide feedback, the system equation requires many more coefficients to achieve the same requirements as an IIR filter. Every additional coefficient necessitates an additional multiplication and more memory requirements for the DSP. It is necessary to design the FIR filter with high speed, low cost and more efficiency. In this proposed work we Design/ improve the Propagation delay of 2 operand adder by using Ladner Fischer and the Propagation delay of Multiplication operation by using Hybrid Technology. The Implementation of the high-speed FIR filter using the Ladner Fischer adder and hybrid multiplier resulted in a significant improvement in performance, in terms of both speed and area. Thus, the proposed FIR filter architecture can achieve high-speed and low power consumption, making it suitable for various applications, including communication systems, image processing, and biomedical signal analysis.

KEYWORDS: Finite Impulse Response (FIR) Filter, High speed, Low Power Consumption, Ladner Fischer Adder, Hybrid Multiplier.

1. INTRODUCTION

In signal processing, a finite impulse response (FIR) filter is a filter whose impulse response (or response to any finite length input) is of *finite* duration, because it settles to zero in finite time. This is in contrast to infinite impulse response (IIR) filters, which have internal feedback and may continue to respond indefinitely (usually decaying).

The impulse response of an Nth-order discrete-time FIR filter (i.e., with a Kronecker delta impulse input) lasts for N + 1 samples, and then settles to zero. The output y of a linear time invariant system is determined by convolving its input signal x with its impulse response b. For a discrete-time FIR filter, the output is a weighted sum of the current and a finite number of previous values of the input. The operation is described by the following equation, which defines the output sequence y[n] in terms of its input sequence x[n]:





where:

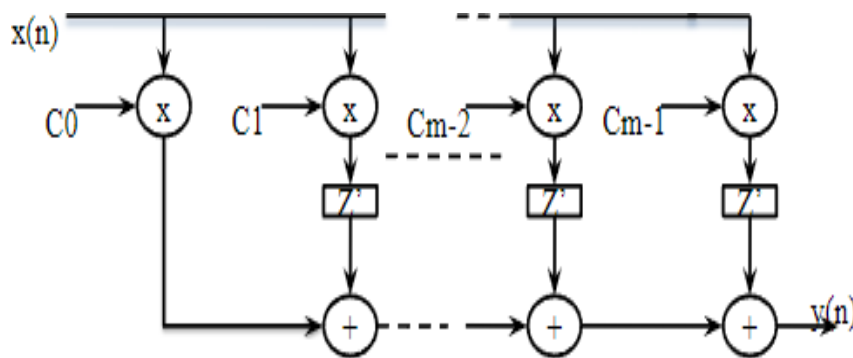
- $x[n]$ is the input signal,
- $y[n]$ is the output signal,
- z^n are the *filter coefficients*, also known as *tap weights*, that make up the impulse response,
- b_n is the filter order; an n th-order filter has n terms on the right-hand side. The n in these terms is commonly referred to as *taps*, based on the structure of a tapped delay

II. EXISTING METHOD

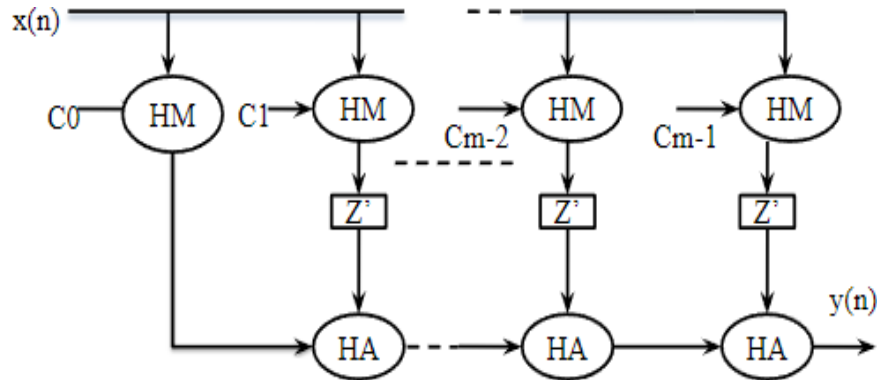
The advanced FIR channel using Variable partition hybrid structure is reduce the amount of postpone registers needed in tap cells, resulting in a substantial reduction in equipment asset use and minimise the multifaceted existence of truncation and measurement in tap cells[4].It is widely used in digital signal processing applications such as speech processing, loudspeaker equalisation, echo cancellation, adaptive noise-cancellation, and various communication applications including software defined radio(SDR) etc. The FIR Filter using approx. the adder has improvised power, delay and areareduction. WTM (Wallace Tree Multiplier) which is designed using Ladner Fischer adder improves the hardware utilisation and power consumption [5]. Filter is a frequency selective system. FIR Filter response depends on present and past input values. It has the advantages like linearity, bounded-input-bounded-output (BIBO) stability, and low sensitivity over IIR filters, which have made them suitable for many real time applications. FIR Filter created using booth multiplier and Hybrid adder combination has less delay compared to others and used in signal processing applications for set of frequencies. FIR filter makes it useful for constructing efficient stable filters and those characteristics are linear phase and unconditional stability, ease of implementation, non-existence of overflow oscillations, greater computational efficiency and the capability to implement filters with coefficient less than one FIR filter using Han Carlson adder has less area and quicker operation lesser cell area make it efficient when compared with other adders. FIR filters are one of the most widely used in FPGA implementations owing to its linear phase Property and stability. The main focus of FIR filter implementation is towards noise and performance constraints. Filters mainly, signal separation and restoration. Separation is required when interference of noise or other signals pollutes the signal and restoration is helpful when a signal is deformed by some means.

III. PROPOSED WORK

The proposed FIR Filter created using Hybrid multiplier and Hybrid adder and delay element D Flip Flop. It follows the conventional FIR Structure and the proposed structure changed by Hybrid multiplier which is designed using Ladner Fischer adders.



Conventional FIR Structure



Proposed Structure

IV. LADNER FISCHER ADDER

Ladner –Fischer adder is one of the parallel prefix adders. Parallel prefix adders are used to speed up the process of arithmetic operation. These adders are introduced to eliminate the carry propagation delay that rises in ripple carry adder. Ladner-Fischer adder is a parallel prefix adder that performs the addition operation. It consists of three stages: pre-processing stage, carry propagation and generation and post propagation.

Pre-Processing Stage:

In this stage generate and propagate are done for each stage of inputs. Propagate is done through XOR operation and generate is done through AND operation.

$$P_i = A_i \text{ XOR } B_i \quad G_i = A_i \text{ AND } B_i$$

Carry Generation:

In this stage, carry is generated for each bit and this is called as carry generate (Cg). The carry propagates and carry generate is generated for the further operation but the final cell present in each bit operation gives carry. The last bit carry will help to produce the sum of the next bit simultaneously till the last bit. The carry generates and carry propagate are given in the equations below.

$$C_p = P_i \text{ AND } P_{i-1}$$

$$C_g = G_i \text{ OR } (P_i \text{ AND } G_{i-1})$$

The above carry propagates C_p and carry generation C_g in equations above is black cell and the below shown carry generation in equation is grey cell. The carry propagate is generated for the further operation but the final cell present in each bit operation gives carry. The last bit carry will help to produce the sum of the next bit simultaneously till the last bit. This carry is used for the next bit sum operation, the carry generated is given in below equations.

Post processing stage:

The first input bit goes under the pre-processing stage and it will propagate and generate. These propagate and generate undergoes carry generation stage produces carry generates and carry propagates, these undergoes post processing stage and gives final sum.

$$S_i = P_i \text{ AND } C_{i-1}$$

V. HYBRID MULTIPLIER

Multiplication involves two operands: the multiplier and multiplicand. Both of these need to be of the same base. Multipliers are used for a variety of applications depending on the restraints each application holds with it. The proposed Hybrid multiplier is extremely effective for higher value numbers but less effective for lower value numbers. When there is a need for multiplying higher value numbers the proposed Hybrid



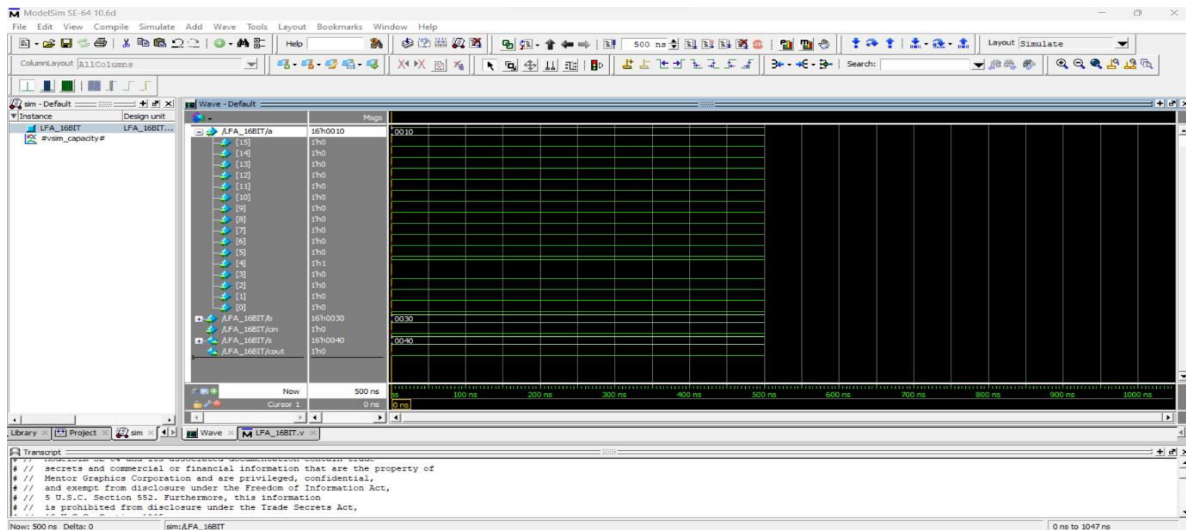
multiplier can be used. As the key length increases the Hybrid multipliers outperform over the other multipliers for higher order values.

VI. SIMULATION TOOL

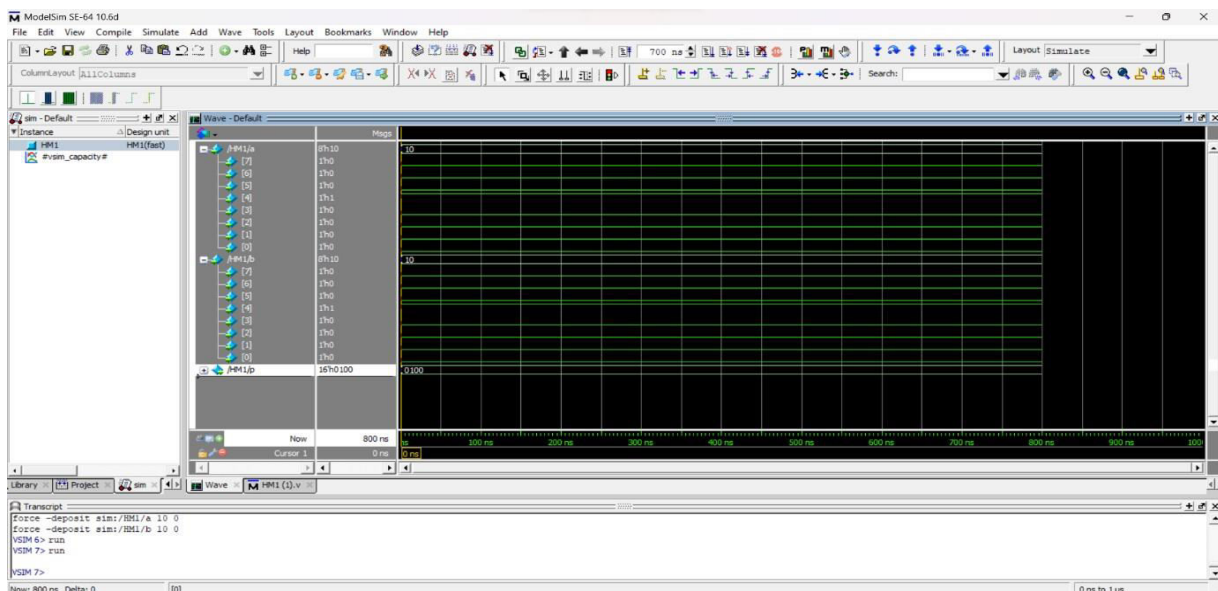
Model Sim is a multi-language environment by Mentor Graphics, for simulation of hardware description languages such as VHDL, Verilog and System, and includes a built-in C debugger. Model Sim can be used independently, or in conjunction with IntelQuartus Prime, PSIM, Xilinx ISE or Xilinx Vivado.

VII. SIMULATION RESULTS

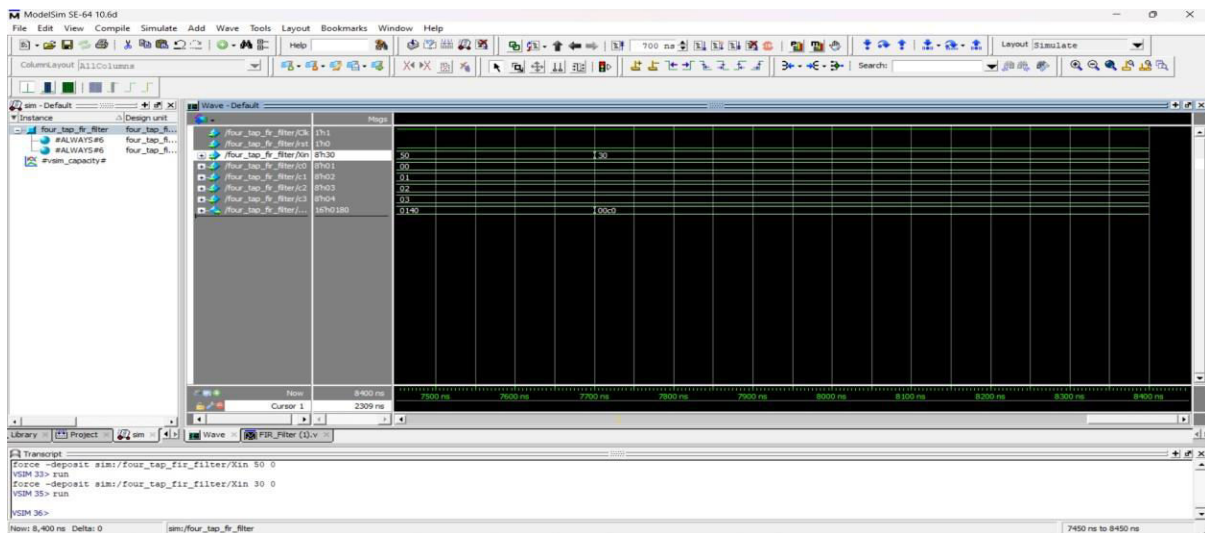
16BIT Ladner Fischer Adder



Hybrid Multiplier



Four Tap FIR Filter



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