



e-ISSN: 2319-8753 | p-ISSN: 2347-6710

# IJRSET

International Journal of Innovative Research in  
**SCIENCE | ENGINEERING | TECHNOLOGY**



# INTERNATIONAL JOURNAL OF INNOVATIVE RESEARCH

IN SCIENCE | ENGINEERING | TECHNOLOGY

Volume 12, Issue 13, April 2023

**ISSN** INTERNATIONAL  
STANDARD  
SERIAL  
NUMBER  
INDIA



# Dynamic Flip-Flop Conversion in Digital Circuits with Hybrid Time Borrowing and Critical Feedback Path Applications

Prof. M. Anitha, Masilamani.R

Asst. Professor(Sr.), Department of ECE, M.P.Nachimuthu M.Jaganathan Engineering College, Tamilnadu, India

II-M.E., Department of ECE, M.P.Nachimuthu M.Jaganathan Engineering College, Tamilnadu, India

**ABSTRACT:** The DFFC is a time borrowing method for improving the performance of digital circuits. This technique is able to mitigate the problems of successive critical and critical feedback path structures. The latch based designs shows large transparency windows and large delay elements that should be inserted in short paths to avoid Hold Time Violation (HTV).

## I. INTRODUCTION

In order to reduce the circuit compliment and critical path reduction behaviour, the circuit output will be analyzed .By using Modified Data Arrival Detector (MDAD) block and Timing Violation Predictor (TVP) the timing slack will be reduced and also the timing errors are removed in between the critical paths. The demand of high performance designs which are not susceptible to variations has been significantly increasing over the past few years. Traditionally, in worst case design methodology the Maximum Allowable Frequency (MAF), in which a circuit works correctly, is computed based on the delay of the longest paths (critical paths) in the circuit.

Such a variation makes some paths work faster or more slowly and forces the designer to include timing margins in the design which leads to the performance degradation. A simple idea to achieve better performance is to increase the operational frequency of the circuit beyond the MAF. In this case timing violations occur because critical paths would not be able to finish their job in a single clock period.

The clock stretching structure stretches the clock dynamically at the same clock period in which critical paths with short sequential depth and problematic path structures including successive critical and critical feedback structures are activated.

## II. EXISTING METHOD

The applications of synchronous circuits need more logic gate as well as critical circuits also. It will create the power consumption more even for a single circuit. Some critical Path algorithm could not be implemented due to this inconvenience. Due to this time borrowing also become difficult one.

## III. DISADVANTAGES OF EXISTING METHOD

In the fewer cases, the latch based designs suffer from large transparency windows and large delay elements. This warning signal is used to raise the supply voltage of the next stage to speed up the next stage and prevent further timing violations. It suffers from Late Conversion(LC) problem which occurs when time borrowing signals in the destination flip- flop of the critical paths are issued after the error has already happened.

## IV. PROPOSED METHOD

In DFFC Type C is not able to resolve the timing errors in Critical Feedback Path(CFP) and Successive Critical Path (SCP) hence use Type B. In addition, due to LC problem it is unable to prevent timing errors in the circuits with short sequential depths. In order to alleviate these problems we have proposed a hybrid technique which prevent the timing error by borrowing the time from the following stages.



Organized by

Dhaanish Ahmed Institute of Technology, KG Chavadi, Coimbatore, India

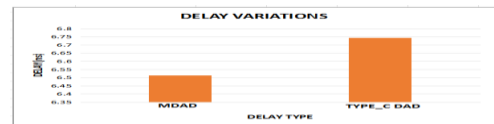
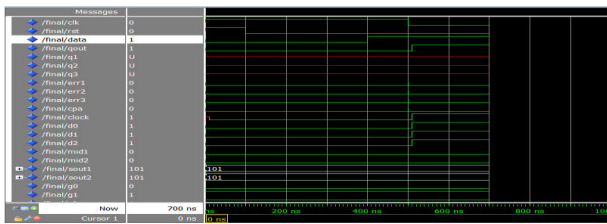
### V.SOFTWARE USED

- XILINX ISE 8.1i
- ModelSim

### ADVANTAGES

It uses in hybrid circuits for critical path elimination. To avoid the timing slack between the successive asynchronous paths. It improves the circuit performance by adding the latch instead of flip flops and reducing the chip area.

### VI.OUTPUT

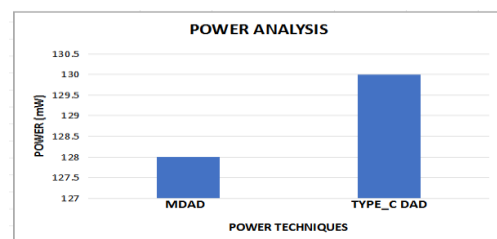
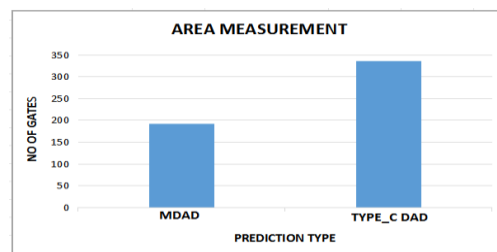
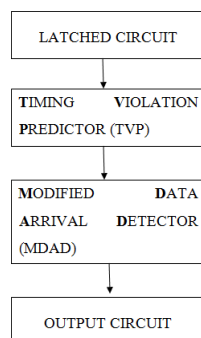


### PROPOSED METHODCOMPARISON

S.NO	METHOD	AREA	DELAY	POWER
1	TYPE CDAD	336 GATES	8.84 ns	130 mW
2	MDAD	192 GATES	2.25 ns	128 mw

### VII. COMPARISON OUTPUT

#### V. DESIGN FLOWDIAGRAM



### VIII. CONCLUSION

A new hybrid technique was presented which utilizes DCSM together with our previous TB method, i.e., DFFC Type C. DFFC allows TB in critical paths while in those critical paths that do not have enough timing slacks in their sub



sequence stages, clock stretching provides enough time to avoid timing violations. It is shown that when the circuit operating at the frequency of  $1.33 \times \text{MAF}$ , in challenging path structures, this hybrid technique is able to tolerate process variations.

### IX. SCOPE FOR FUTUREWORK

As our future work, we are going to investigate new hybrid techniques with TB mechanism and different DFFC types that utilize a combination of different techniques applicable to various critical paths. The Area, Delay and Power variations can be improved from 18% to 35% respectively.

### REFERENCES

1. Mehrnaz Ahmadi, Bijan Alizadeh (2021) "A Hybrid Time Borrowing Technique to Improve the Performance of Digital Circuits in the Presence of Variations", IEEE Trans. and Behjat Forouzandeh.
2. K. Chae, C. H. Lee, and S. Mukhopadhyay (2020) "Timing error prevention using elastic clocking", in Proc. ICICDT, pp.1–4.
3. L. Seongwan, S. Paik and Y. Shin (2020) "Retiming and time borrowing: Optimizing high-performance pulsed-latch-based circuits", in Proc. ICCAD, pp.375–380.

### BIOGRAPHY

M.Anitha completed her M.E in Mahendra Engineering College, Completed B.E Electronics and Communication Engineering in Kongu Engg College, Perundurai and have 14 years of teaching experience. Now working as an assistant professor in ECE department at M.P.Nachimuthu M.Jaganathan Engineering College, Erode, Tamilnadu, India.

R.Masilamani has pursuing M.E. VLSI Design in M.P.Nachimuthu M.Jaganathan Engineering College, Erode and Completed B.E Electronics and Communication Engineering in M.P.Nachimuthu M.Jaganathan Engineering College, Erode, Tamilnadu, India.



# INTERNATIONAL JOURNAL OF INNOVATIVE RESEARCH

IN SCIENCE | ENGINEERING | TECHNOLOGY

 9940 572 462  6381 907 438  [ijirset@gmail.com](mailto:ijirset@gmail.com)



[www.ijirset.com](http://www.ijirset.com)

Scan to save the contact details