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 [ijirset@gmail.com](mailto:ijirset@gmail.com)

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# Speed Enhancement Techniques for Clock Delay Dual Keeper Domino Logic Style

DR.C.AARTHI, M.KARTHICK

Department of ECE, Sengunthar Engineering College (Autonomous), Tiruchengode, India

ME-VLSI DESIGN, Department of ECE, Sengunthar Engineering College (Autonomous), Tiruchengode, India

**ABSTRACT:** Clock Delayed Dual Keeper domino logic style with Static Switching mechanism (CDDK\_SS) using delayed enabling of the keeper circuit and modified discharge path has been proposed in this paper. In CDDK domino circuit, the principle of delayed enabling of keeper circuit offers reduced contention between keeper circuit and Pull down Network (PDN). The modified discharge path at the output node eradicates the switching at the output node for identical TRUE inputs during the pre-charge phase. This facilitates in obtaining static like output in contrast with conventional domino logic. The simulation results of Arithmetic and Logic Unit (ALU) subsystems demonstrate 17.7% reduction in dynamic power consumption while compared to conventional domino logic. Furthermore, 62% enhancement in speed performance has been achieved with good robustness. Design and simulation have been executed using Cadence® Virtuoso, with UMC 90nm technology node library. Dynamic logic circuit occupies prominent position in digital designs due to high-speed performance and lower power consumption. The conventional domino logic circuits comprise the dynamic circuit structure with a static inverter at the output node. This makes the triggering of successive stages to be flawless. The domino logic circuit design with reduced number of transistors and NMOS transistors for evaluation makes the design to be more power efficient and offer comparatively faster performance. The keeper transistor M2 has been incorporated to replenish the dynamic node against leakage-current and charge sharing.

## I. INTRODUCTION

Design of domino logic circuits at lower technology nodes, require a keeper circuit to facilitate replenishing of dynamic node against charge leakage and charge sharing. However, this imparts reduction in operating speed and robustness. To overcome this, the proposed work focus on the design of a novel Transmission Gate based Clock Delayed Dual Keeper Domino Logic topology (TG\_CDDK) and PMOS Transmission Gate based Clock Delayed Dual Keeper Domino Logic topology (PMOS\_TG\_CDDK). The proposed keeper circuit comprises two keeper transistors in series and is controlled by a transmission gate configuration. Using this TG\_CDDK, the keeper circuit is enabled only after a delay during the initial evaluation phase. This facilitate faster discharge of the dynamic node without any contention on the pull-down network (PDN) evaluating a TRUE condition. Further, the decrease in the feedback loop gain eliminates the aggravation of the variability effects while the circuit is continuously operated. The circuit was designed and simulated using Cadence® Virtuoso with 180nm technology library. The ADEL spectre results demonstrate 39.8% and 37.7% increase in speed in the proposed designs over the conventional domino logic and an optimal delay variability of 8.02% and 7.11% while subjected to 2000 runs using ADEXL.

The keeper transistor M2 has been incorporated to replenish the dynamic node against leakage-current and charge sharing. Depending on footer transistor inclusion, the domino logic circuit variants are classified as footed domino logic and footer-less domino logic circuits [2, 3]. Domino logic circuit operation occurs in two phases as defined by the clock CLK signal. The pre-charge phase occurs when clock signal CLK is LOW and evaluation phase occurs when clock CLK is HIGH. Scaling up of keeper transistor size increases the robustness of the circuit. However, this increases the contention between keeper and PDN. This is due to the keeper circuit, which tries to retain the logic HIGH during HIGH input conditions to the pull-down network (PDN). This leads to decreased speed performance. Thereby, the switching at the output node is reduced. This paper proposes clock delayed dual keeper with static switching (CDDK-SS), a control mechanism for the keeper to reduce contention current and also provides a static output. It is based on the delayed enabling of the dual keeper transistor arrangement using, delayed inverted clock signal. The static inverter configuration at the output node prevents the discharge of the output node during the pre-charge phase. Section 2 details the domino logic operation, Section 3 elaborates the existing switching mechanism and Section 4 elaborates the CDDK domino logic design. Section 5 exhibits the design of CDDK-SS mechanism.

## II. LITERATURE SURVEY

### 2.1. Domino Logic

OR-gate standard domino logic module. It consists of a clocked PMOS device mp1, pull down network consisting of only NMOS transistors, clocked NMOS device mn1 and a static inverter producing non-inverting output, out [5]. A PMOS transistor mp2 known as keeper is added to improve noise margins and to hold the value of output node X to high state during evaluation phase. The pull down network is built exactly as that in complementary CMOS. The domino module works in two phases – precharge and evaluation. Signal clock controls the mode of operation of domino as shown below:

- Precharge Phase 1,
- Evaluation Phase 2

During precharge phase domino node X is charged to VDD by PMOS transistor mp1. The clocked NMOS transistor mn1 is off during this phase. Since the value of out becomes '0', keeper transistor mp2 turns on which charges the value of node X to VDD. During evaluation phase, transistor mp1 is off while mn1 is in on state. If the input values i1-i8 are such that pull down network conducts, then node X discharges to '0'.

### 2.2. TECHNIQUE LE SLEEP SWITCH DUAL DOMINO (SSDD)

Uses sleep switches and a dual threshold voltage in order to place an idle domino logic circuit into a low-leakage state. In Fig. 9 high  $V_{th}$  transistors mp1, mp2, mn2 and mn3 are represented with a thick line in the channel region. Another technique PMOS only sleep switch dual-domino (PSSDD) as uses PMOS only sleep switch transistors i.e. mp4, mp5 and mp7 to further reduce the leakage current in domino logic circuits [13]. In [14], work has been done to reduce the delay variation of the circuit which occur due to the feedback loop from output to input. Fig. 11 shows the circuit for reduced delay variations domino logic (RDVD). It uses a stack of PMOS transistors mp2 and mp3 as a modified keeper. The configuration of Foot Driven Stack Transistor Domino Logic (FDSTD L).

### 2.3. NOISE IMMUNITY, DELAY, AND ENERGY TRADEOFFS

Domino Logic Circuits As described in Section II-A, the keeper transistor is fully turned on as the output goes low during the precharge phase. When the clock signal transitions high, the pullup transistor turns off and the keeper transistor provides the only conductive path between the dynamic node and , preserving the logical state of the dynamic node in the evaluation phase. Provided that the necessary input combination to discharge the dynamic node is applied during the evaluation phase, the keeper transistor opposes the evaluation of the input signals, degrading the speed and power characteristics of a SD logic circuit.

### 2.4. MULTIPLE OUTPUT DOMINO CARRY GENERATOR WITH VARIABLE THRESHOLD VOLTAGE KEEPER

A four-bit multiple-output domino carry generator (CG) implemented with the proposed variable threshold voltage keeper circuit technique (CG-DVTVK) is shown in Fig. 6. A description of the multiple-output domino circuit technique is presented in [11]. The CG circuit has four dynamic nodes. Each dynamic node of the CG can be discharged independently by asserting the generate input of the corresponding node. The critical path of the CG circuit is along the - path.

## III. PROJECT DESCRIPTION

### 3.1. EXISTING SYSTEM

Wide fan-in domino logics are used in VLSI circuits and high performance microprocessors. A small PMOS keeper is required in domino logic to maintain the robustness of the circuit. If the number of inputs of domino logic increases, a large sized PMOS keeper is required. But, this in turn increases the contention current between PMOS keeper and NMOS pull down network, which degrades the performance of the circuit and increases the dynamic power loss. To eliminate this problem, a clock delayed domino logic (CDD) with keeper circuit is presented. The concept of CDD, where mp1 is the clock gated PMOS transistor and mp2 is the keeper. Although this concept eliminates the contention current between PMOS keeper and NMOS pull down network it has more power dissipation and area due to the additional nand gate.

**3.2. DISADVANTAGES**

- In order to solve the trade-off between performance and noise-margin, a high speed domino logic (HSD).
- In this technique, output signal out is connected to the keeper mp2 via NMOS transistor mn1 and PMOS transistor mp3.
- This design reduces 60% of energy consumption as compared to standard domino logic.

**3.3. PROPOSED SYSTEM**

The proposed circuit is similar to standard domino logic except an addition of NMOS transistor in the modified keeper. This NMOS transistor is used in the proposed design to keep the keeper off at the beginning of evaluation and thus to eliminate the contention current and to reduce the power dissipation. The proposed design uses single threshold voltage without any sleep signal which reduces the area as compared to above mentioned designs. The proposed domino logic with modified keeper circuit. The keeper consists of an NMOS transistor mn2 which is connected in series to PMOS transistor mp2. The gate of mn2 is connected to the clock while gate of mp2 is connected to the output terminal i.e. out. During the precharge phase (clock='0'), mp1 is on, which charges domino node X. Since transistor mn2 is off, keeper is off at the beginning of evaluation. This will eliminate the contention current.

**3.4. ADVANTAGES**

- The percentage comparison of dynamic power of proposed technique with respect to existing techniques.
- Positive percentage in Table III means that the existing technique has more dynamic power dissipation than the proposed technique.

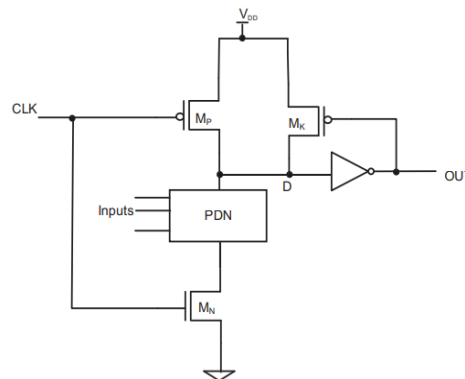


Figure 1. Conventional domino logic circuit.

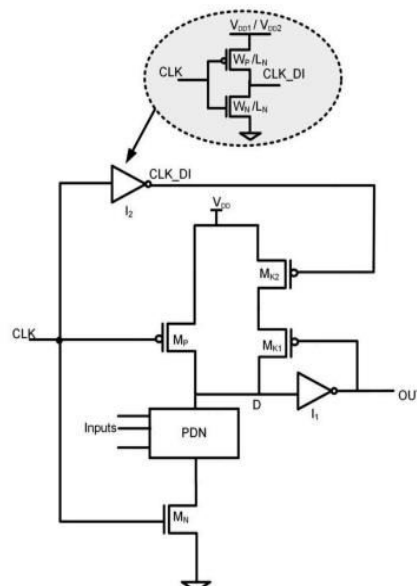


Figure 2. Clock-delayed domino keeper circuit topology

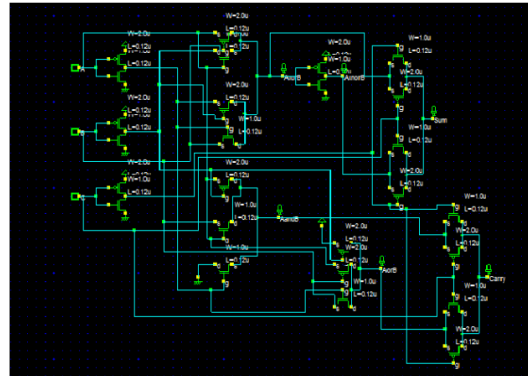


Figure.3. (a) Schematic of CLA in normal mode

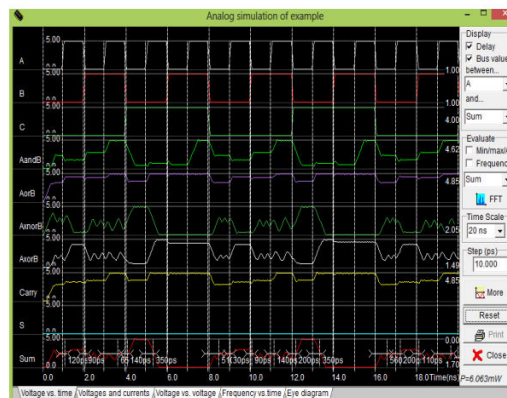


Figure.4. (b) Transient analysis of CLA in normal mode

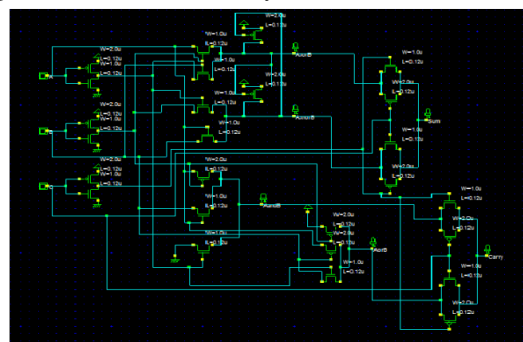


Figure. 4. (c) Schematic of CLA in standby mode

#### IV. CONCLUSION

The unnecessary switching during the pre-charge phase of the domino logic is eliminated by connecting the source terminal of NMOS transistor of the output inverter to the drain terminal of footer transistor in CDDK\_SS mechanism. This avoids discharge of the dynamic node during pre-charge operation and thereby reduced switching at the output node is reduced. The delayed enabling of the keeper circuit also reduces the contention current. The incorporation of these principles, offers increased speed performance with reduced power consumption. It is observed that for a 128 bit OR gate the power consumed has decreased from 27.4 $\mu$ W to 22.7 $\mu$ W and the delay has been reduced from 307.3ps to 271.9ps. These results confirm that the proposed clock delayed dual keeper with static switching mechanism offers high speed with low power consumption.

## V. FUTURE ENHANCEMENT

Since the contention current is significantly reduced with the proposed variable threshold voltage keeper technique, the keeper transistor in a DVTVK circuit can be sized larger, offering greater noise immunity with the same delay and power characteristics as compared to a SD logic circuit. The DVTVK and SD circuit techniques are compared in terms of the noise immunity that the two circuit techniques offer with the same evaluation delay, power dissipation, or power-delay product characteristics. For the same evaluation delay characteristics, DVTVK (with a zero biased keeper) offers 14.1% higher noise immunity as compared to SD. Under the same power dissipation conditions, DVTVK (with a zero biased keeper) improves the noise immunity by 8.9% as compared to SD. Similarly, under the same PDP conditions, DVTVK (with a zero biased keeper) offers 11.9% higher noise immunity as compared to SD. Forward body biasing the keeper transistor is also proposed to improve the noise immunity as compared to a SD circuit with the same keeper size. By applying a forward body bias of 600 mV to a keeper transistor, the noise immunity is enhanced by up to 10.2%. Dynamically forward and reverse body biasing the keeper transistor simultaneously enhances the noise immunity, evaluation speed, power dissipation, and PDP characteristics of a domino logic circuit.

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