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10/100 Mbps Ethernet MAC FIFO Controller

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ABSTRACT: The 10/100 Ethernet IP core provides an 10/100 Mbps Media Independent Interface (MII) and an optional processor interface; it also supports Reduced MII (RMII) and Serial MII (SMII). The 10/100 Ethernet MAC IP is designed for SoC and mobile applications such as integrated networking devices, PCI-Express Ethernet controllers, and Ethernet adapter cards. The 10/100 Ethernet IP supports half-duplex mode and full-duplex mode at 10/100 Mbps. The 10/100 Mbps Ethernet-FIFO convertor IP core is an interface in charge of data conversion between the raw MAC frame and bit stream from one to the other. The bit stream's data rate depends on the input clk's frequency. This convertor is used in a project to connect the GSM modulator/demodulator with PC. So the data form is conformed to the GSM standard. However, the structure of Verilog HDL code is very clear and easy to understand so that can be easily changed to be used in other situations, the module is implement it using Verilog HDL and simulate or verify it using mentor graphics modelsim simulator tool.

Keywords- Ethernet , SoC , GSM module , Physical layer , Initiation module , Transmitter module , Receiver module.

I. INTRODUCTION

With the ongoing extension of technology, we are witnessing the emergence of new computing machines, which will bring us far beyond the desktop PC. Devices featuring advanced connectivity and Internet functionality will soon become the standard in computing. In fact, we're on the verge of a revolution that will bring us a wave of smart, electronic devices that can be controlled, gather information, and distribute data via the web. Virtually every embedded designer is looking to use Internet, to enhance or expand the reach of embedded systems. This need for connecting devices directly into Internet has lead many great manufacturers to implement ASICs (Application Specific Integrated Circuits) or reusable libraries for microcontrollers, specially designed for this purpose. As essential elements of design reuse, IP cores are part of the growing electronic design automation (EDA) industry trend towards repeated use of previously designed components. Ethernet continues to be one of the most popular LAN technologies.

The 10/100/1000 Mbps Ethernet MAC IP is designed for Embedded Applications, SoC and mobile applications such as integrated networking devices, PCI-Express Ethernet controllers, and Ethernet adapter cards. The 10/100/1000 Mbps Ethernet IP supports half-duplex mode at 10/100 Mbps and full-duplex mode at 10/100/1000 Mbps.

The 10/100 /1000 Mbps Ethernet MAC FIFO IP core consists of three modules:

The Initiation module, in charge of the power on reset.

The Transmit module.

The Receive module.

The Ethernet MAC IP Core is capable of operating at 10 or 100 /1000 Mbps for Ethernet and Fast Ethernet applications. An external PHY is needed for the complete Ethernet solution.

II. LITERATURE REVIEW

Ethernet is a mature communication technology with a sizable number of advantages for sensor networks and many other use cases. Applications interact with a media access control (MAC) sub layer to get packets from and to the network. This thesis presents the design, implementation, and test of an Ethernet MAC targeted at FPGAs in VHDL. It supports full duplex interfacing with an Ethernet physical layer integrated circuit via the standard media independent interface (MII) variants MII and GMII at link speeds of 10, 100, and 1000 Mb/s. In contrast to prior solutions, it is devised primarily with simplicity in mind, both in external usage and in internal operation. Users benefit from the straightforward FIFO interface offered while nevertheless being able to send and receive at almost full Gigabit Ethernet

speed. The MAC supports communicating with a physical layer integrated circuit via the standard media-independent interface at 10, 100, and 1000 Mb/s link speed and automatic detection of the current speed. Prior FPGA implementations of tri-mode Ethernet MAC sub layers were laden with nonessential features such as CSMA/CD for halfduplex connections, energy efficient. Ethernet support or complex on-chip bus interfaces. While beneficial for e.g. using them in combination with embedded processors, an increasing amount of features is accompanied by increasing complexity and cost. In contrast, only essential Ethernet functionality was considered for the present thesis [1].

With the conventional directed testbench, it is highly improbable to handle verification of current complex Integrated Circuit (IC) designs, because a person has to manually create every test case. The greater the complexity of the designs, the higher the probability of bugs appearing in the code. Increasing complexity of ICs has created a necessity for performing verification on designs with an advanced, automated verification environment. Ideally this would eliminate chip re-spins, minimizing the time required to enable checking of all the design specifications, ensuring 100% functional coverage. This paper deals with the design of Synchronous FIFO using Verilog. A FIFO (First-In-First-Out) is a memory queue, which controls the data flow between two modules. It has control logic embedded with it, which efficiently manages read and write operations. It has the capability to notify the concerned modules regarding its empty status and full status to help ensure no underflow or overflow of data. This FIFO design is classified as synchronous, as clocks control the read and write operations. Both read and write operations happen simultaneously using of Dual port RAM or an array of flip-flops in the design. After designing the Synchronous FIFO, its verification is carried out using the Universal Verification Methodology (UVM). A detailed discussion about the verification plan and test results is included [2].

Currently two technologies are dominant in the LAN environment: the Ethernet standardized by the IEEE as 802.3, and the Token ring, represented by norm IEEE802.5. The Ethernet technology is based on a shared environment, using protocol CSMA/CD for determination of physical network access. The standard IEEE 802.3 defines three physical media, baseband or wideband coaxial cables, as well as twisted wires. The use of the twisted wire cables, called 10BaseT, has become popular. It can connect a large number of workstations using hubs or switches, physically connected as a star network, but logically connected as a bus. The Token Ring technology uses a special frame called "Token", which determines which workstation has the right to access the wire that is physically and logically organized as a ring. However, the Ethernet is the most used due to its easiness of implementation, tolerance to errors and its production in large scale. An isolated computer, device or resource which lacks this interface does not satisfy current communication needs. It is then compelling that each device to be connected to an Ethernet Local Area Network have an Ethernet Interface [3]

III. METHODOLOGY

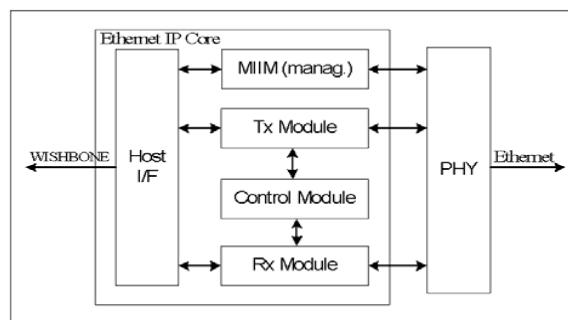
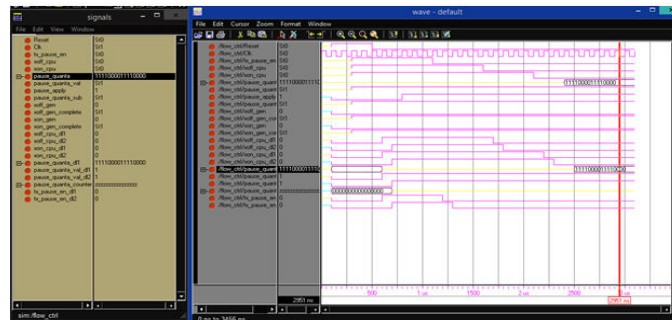


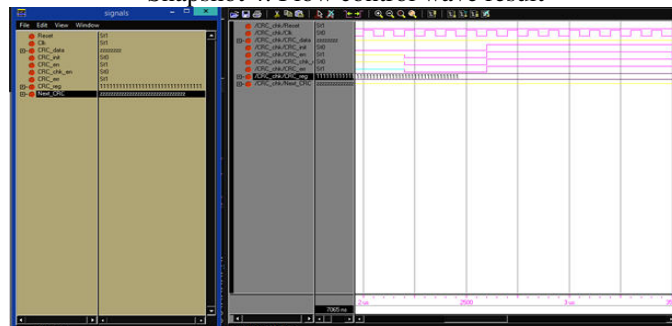
Figure 1: Ethernet MAC IP Core Architecture

The Ethernet IP Core consists of five modules (as shown in figure 4):

- └ The host interface connects the Ethernet Core to the rest of the system via the WISHBONE (using DMA transfers). Registers are also part of the host interface.
- └ The TX Ethernet MAC performs transmit functions.
- └ The RX Ethernet MAC performs receive functions.



Snapshot 4: Flow control wave result



Snapshot 5: CRC check wave result

V. FUTURE SCOPE

In future work, the MAC FIFO controller design can be enhanced in several ways, such as:

- Support for higher data rates, such as Gigabit Ethernet or 10 Gigabit Ethernet.
- Integration of advanced features, such as flow control mechanisms or VLAN (Virtual Local Area Network) support.
- Optimization for low-power operation, including power gating techniques.
- Implementation on advanced process technologies for improved performance and area efficiency.

VI. CONCLUSION

The VLSI design of the 10/100Mbps Ethernet MAC FIFO controller provides an efficient and scalable solution for managing data transmission and reception in Ethernet networks. The design meets the specifications for supporting 10/100Mbps data rates while ensuring low power consumption and adherence to Ethernet protocol standards. The performance evaluation demonstrates the effectiveness of the MAC FIFO controller in terms of throughput, latency, power consumption, and area utilization.

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