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Telecommand System using FPGA

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ABSTRACT- The main intent of this project was to create an encoder for ground stations using FPGA to send telecommands concurrently so that commands would not go sequentially. Since the signal passes through space, it gets external noise added to them naturally which may also cause damage to the spacecraft. Using BCH code in programming helps to avoid errors during encoding. A parity generator helps to nullify the noise level. And get desired response from the spacecraft.

KEYWORDS- TC- Telecommand, TM- Telemetry, GEO- Geostationary Equatorial Orbit, LEO- Low Earth Orbit, RF- Radio Frequency, BCH- Bose Chaudhury Hocquenghem, "FPGA- Field Programmable Gate Arrays", CLB- Configurable Logic Blocks, ASIC- Application Specific Integrated Circuits, IDE- Integrated Development Environment, RTL- Register Transfer Level, IC- Integrated Circuit, POR- Power-on Reset.

I. INTRODUCTION

The word Telecommand is derived from the word **tele** which means **remote** in Greek, and **command** which means the order in Latin. So, both together make the definition of Telecommand, that is the command sent to the remote system or connected without any direct medium such as wires. The main part of the TC is to convey the controlling information from the ground station to the spacecraft according to which TM can change the parameters which are given from the ground state and the same to receive from the spacecraft to the ground state. Since these are wireless or do not directly contain any medium of transferring command the only way is through signals. But the values revived from the parameter sensor such as temperature, connection, direction, etc, give the analog data to the TC which needs to be converted to share commands from both sides. Therefore, the TC in the Ground System needs Encoder, and TC in the spacecraft needs Decoder. The data is shared through the RF space link.

The transmission of the carrier wave could be by electromagnetic means. The encoder is coded with the help of cycling codes, which means any lateral shift of the code word is also a code word. This also uses Bose- Chaudhury- Hocquenghem (BCH) Codes, which means this coding design of optimum codes is to make the block size smallest for a given size of the message block to obtain desired value. When we desire to give large code, we must look for the best error-correcting capabilities. Since BCH is known as the most important and powerful error-correcting cyclic code can be used in our project. Since the security of information from both spacecraft and ground stations is very important, we need to look after their protection for them. Fig.1. shows the top basic block diagram of communication.

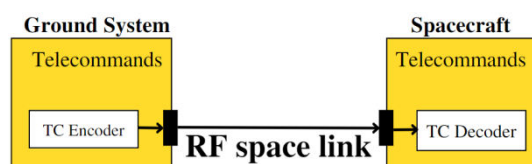


Fig. 1. Basic Block diagram of Communications with spacecraft

A parity coder is used to generate polynomial to balance the errors during encoding and decoding made by the code or external noise. The noise may change the information carrier wave to alter the data which could be harmful to both data and spacecraft, since the communication system of the spacecraft and ground stations are quite expensive the signals must be sent with high accuracy. And there might be a condition where our telemetry does not respond to our command

at that time our design helps since we use FPGA design which concurrently processes the codeso the data can be sent in the intermediate steps. While in another hand C or any language goes in sequential order, which may cause unidentified delays to our command. Since this command contains the data which needs to be secured unidentified delays may cause damage or even chances of losing data. Because of this, the command may work or may not. The telemetry measures all the physical parameters and sendsthem to the telecommand from the spacecraft which contains data on the surroundingsand health of the spacecraft and should be given to TC without any disruption.Fig.2. shows the block diagram of the Ground Segment.

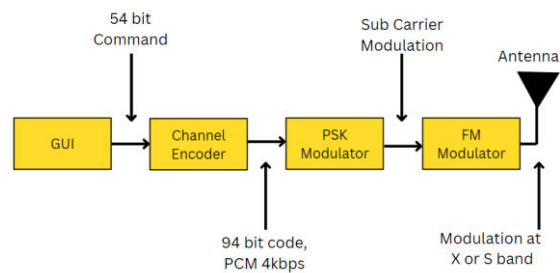


Fig. 2. Diagram of the Ground segment.

II. HARDWARE

A. FPGA (FIELD PROGRAMMABLE GATE ARRAY)

“These are semiconductor devices that are based within a matrix of CLB (configurable logic blocks) which are connected to provided programmable interconnections.” (FPGA world) This provides the function of reprogramming applications according to the functionalrequirements after manufacturing. This feature makes it different from ASICs (application-specific integrated circuits). Fig.3. shows the architecture of FPGA.

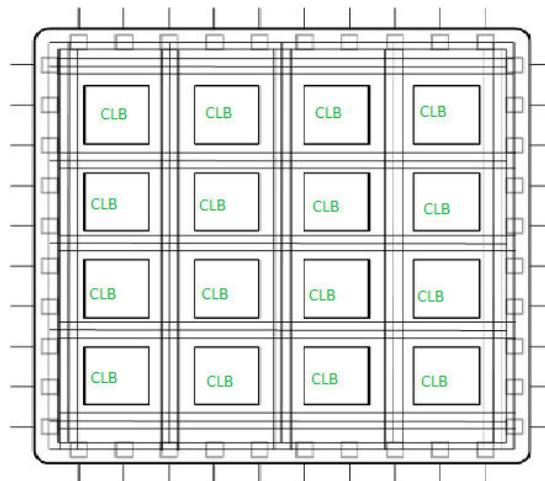


Fig. 3. FPGA Architecture (<https://www.geeksforgeeks.org>)

Everybrand has its architecture but on all terms they have variation. This architecture contains programmableinterconnect, configurable I/O blocks, and configurablelogic blocks. Spartan 2 (XC2S200PQ208AMS0345) was used in this design. The design of the chip also includes Top-Down Design, the logic that fits well with the architecture of the component we have chosen, synchronous design, avoiding bus contention and floating nodes, and protection against metastability.

The design utilizes the top-down design which means the high-level blocks are defined first and the lower-level blocks' implementation details are filled in. This method simplifies the design, allows more than one editor to design, and allows flexibility in the chip when necessary. Replacement of section with a high rate of performance design without changing other parts of the chip. The chip cannot be altered after production, simulation becomes an extremely important consideration in chip design, therefore the simulation must be done compulsorily before the chip is sent for fabrication. This method allows each module to simulate independently from the rest of the design.

III. SOFTWARE

"VHDL is generally used to edit text models that describe logic circuits. These kinds of models are processed by a synthesis program only if it is part of the logic design." This has a process to control the parallelism inherent in hardware design, but this process distinguishes syntax from the parallel process in the task. The next process is to simulate which also means testing. A program of simulation is used to check/test the logic design using simulation to represent the logic circuit design that interfaces to the design. This group of the testing of the model is called Testbench.

Anyone can design/build hardware of any design which can later be fabricated in a VHDL IDE to get the "RTL schematic" of the required circuit. After the generation of the RTL schematic, they can be verified using simulation software which allows the wave of inputs and outputs of the circuit after giving the appropriate testbench.

Xilinx is part of AMD which develops, designs, and markets programmable logic products including ICs, predefined system functions delivered as intellectual property, customer training, field engineering, and software design tool.

"Modelsim is the verification and simulation tool for the VHDL codes, Verilog, system Verilog, and mixed language designed code." The debugging environment provided by Modelsim's robust allows for tracking down the cause of the problem.

IV. VHDL CODE ARCHITECTURE

Telecommand Encoder (Top Module)

- PISO/PIPO (Parallel-In Serial-Out/ Parallel-Out Shift Register)
- Clock Divider
- Reference signal generator 1
- Input Counter
- Frame Synchronizer
- Reference Signal Generator 2
- Output Counter
- Parity Generator
 - EXOR Gate 1 & 2
 - OR Gate
 - D-Flip Flop
 - 5-Bit Shift Register
 - 6-Bit Latch

Input Data: 54-bits D₍₁₎ to D₍₅₄₎ where D₍₁₎ is MSB

Output Data: 6-bits P₀₁ (n) to P₀₆ (n) where P₀₁ is MSB, n varies from 0 to 54.

Step 1: Initialize P₀₁(0), P₀₂(0), P₀₃(0), P₀₄(0), P₀₅(0), P₀₆(0) to 0_B.

Step 2: For n=1 to 54, do

- P₀₁(n) = P₀₂(n-1)
- P₀₂(n) = P₀₃(n-1)
- P₀₃(n) = P₀₄(n-1)

- $P_{04}(n) = P_{05}(n-1)$
- $P_{05}(n) = D(n) \text{ XOR } P_{01}(n-1) \text{ XOR } P_{06}(n-1)$
- $P_{06}(n) = D(n) \text{ XOR } P_{01}(n-1)$

Step3: Parity bits $P_{01}(54)$, $P_{02}(54)$, $P_{03}(54)$, $P_{04}(54)$, $P_{05}(54)$, $P_{06}(54)$.

V. WORKING

Algorithm

Step 1: Set POR, Ready Signal, to '0'.

Step 2: Apply the 54-bit parallel data command at the input shift register.

Step 3: When 'RDY' input is 1, the parallel data will be latched into the shift register and the input counter will start to count.

Step 4: Parity will be generated on every count.

Step 5: At the count of 54, the 54-bit parallel data and 6-bit parity will be taken into frame synchronizer. 16-bit header and 20-bit trail bits are added to make a command frame of 96 bits.

Step 6: At the counter of 55, the frame synchronizer produces a ready pulse for the output shift register. Counter 1 is set to '0'.

Step 7: When the PISO finds a ready pulse at the input, the parallel 96-bit command is latched into the register and the output counter will start to count.

Step 8: For count (in output counter) >96, the serial data would be transmitted out of the shift register at speed of 4kbps.

Step 9: At the count of 96 (at the output counter), the shift register transfers its last bit out and the output counter is set to '0'.

Step 10: The PIPO (input shift register) is enabled to accept the next command. Fig. 4. Shows the block diagram of interconnects and pin diagram.

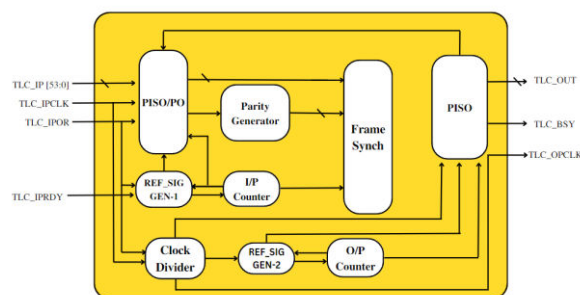


Fig. 4. Block Diagram

Practical Working.

Since the health of the spacecraft is very necessary, we have to look for a good communication medium. Therefore, the proposed project deals with communication system design from the ground station to the spacecraft. TC and TM are the two major working parts when it comes to unchangeable or non-replaceable parts. TM sends measured parameters such as temperature, speed, direction, voltage control, etc., according to which the ground station changes and sends the data

to change accordingly. Since the data or signals must be sent in an air medium there would be some loss of signal which may damage to spacecraft. Therefore, the parity generator is kept nullifying the loss. The BCH code allows the optimization of the errors during the encoding. Data shared by any spacecraft also includes several security data which need to be secured and sent to the respective ground station.

VI. CONCLUSION

A 4kbps TC encoder has been designed and understood. This TC uses PSK modulation with a 44-kHz sub-carrier so that it does not intervene with 32 kHz of TM by which several errors can be reduced which were caused by cross talks. This project can be implemented for the spacecraft which are in GEO which means points toward one place of approximately 36,000 km from the earth's surface, or the altitude of the GEO is about 5.6 times the radius.

Direct-broadcast Televisions satellites are the best examples of GEO satellites. Earth-surveillance missions including military and weather tracking missions could be done by GEO. Not only in GEO but in the LEO as well. Which is approximately 2,000km of its altitude. Finally, it explores the utilization of data within a particular place by involving another spacecraft. As time changes this may get improved.

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