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Two Highly Efficient Low-Power Approximate Unsigned Multipliers with an Innovative Configuration for Approximate 4:2 Compressors

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ABSTRACT: The paper proposes the development of a novel arrangement to increase the performance of approximation- unsigned multipliers. The proposed multipliers' major goal is to improve performance and minimize power consumption while maintaining an acceptable level of accuracy. The first version of the multiplier architecture uses a changed version of Booth encoding along with a special approach to making approximate partial products. This method minimizes the number of incomplete products and removes superfluous calculations, resulting in enhanced computational performance and lower power usage. The second multiplier employs a tree structure based on an approximate carry-save adder (CSA). The multiplier achieves a large reduction in power consumption while maintaining an acceptable degree of precision by adopting a technique that approximates the common subexpression elimination (CSA) tree. Furthermore, a novel rounding approach has been implemented into the proposed design in order to improve precision. Both multipliers are synthesized using 45nm complementary metal-oxide semiconductor (CMOS) technology with Verilog Hardware Description Language (HDL) implementation. The results show that the proposed designs consume significantly less power than typical precise multipliers while just slightly reducing accuracy. Furthermore, the proposed multipliers show better efficacy in terms of throughput and latency. This paper presents two effective unsigned multipliers that strike a balance between power consumption, performance, and precision. These designs present a feasible option in circumstances where power efficiency is crucial, such as in portable devices or systems with limited energy resources.

KEYWORDS: Common Subexpression Elimination, Hardware Description Language (HDL), Carry-Save Adder (CSA), CMOS

I. INTRODUCTION

Approximate computation has shown promise in situations where absolute precision is not required, particularly in terms of reducing power consumption and design complexity. Approximate multipliers are commonly used in error-tolerant application fields such as machine learning, image processing, and digital signal processing. Because of their inherent imprecision, classic multipliers necessitate a substantial amount of energy and space. In contrast, approximate multipliers achieve higher levels of efficiency at the sacrifice of a certain degree of precision. This means that, while they may produce findings that are modestly imprecise, they do it with significantly less energy and space. A plethora of approximation multiplier architectures have been documented in academic literature. Nonetheless, given their continual demonstration of efficiency and precision, more improvements in the production of more accurate multipliers are required. The two innovative approximate unsigned multipliers proposed in this work have significantly higher space and power efficiency than previously published approximate multipliers. The multipliers under consideration are built on the development of innovative configurations for about 4:2 compressors, which serve as the multipliers' foundational components. A 4:2 compressor is used to generate two output bits from a set of four input bits. The number of erroneous output bits determines the degree of precision demonstrated by a compressor. In general, modern approximation compressors have a limited number of output bits set to the "off" state.

The multipliers under discussion reduce the occurrence of erroneous output bits by employing unique compressor configurations. The multiplier with enhanced accuracy is recommended as the initial multiplier; it

employs optimization approaches to reduce the number of incorrect output bits. The Low-Power Approximate Multiplier, the second proposed multiplier, minimizes power consumption by implementing energy-efficient design principles and transistor downsizing, among other strategies. The proposed multipliers are synthesized using 28nm technology and then tested against a variety of benchmark applications. The data indicate that the multipliers proposed produce significant savings in both power and space utilization while maintaining a sufficient level of accuracy. This property makes them suitable for use in embedded systems, mobile devices, and other applications requiring tiny size and low energy consumption.

The two highly effective unsigned multipliers utilizing approximation techniques are proposed in this paper. The purpose of these multipliers is to optimize efficiency and reduce power consumption, while maintaining a high level of precision. A modified Booth encoding scheme and a novel approximation partial product generating method are employed in the initial multiplier design. The improved Booth encoding method has two advantages, namely decreased power consumption and enhanced computational speed. The achievement of this goal is facilitated by reducing the quantity of partial products and eliminating superfluous computations. The utilization of the approximation partial product generation technique, which involves estimating the manufacturing process of partial goods, has been found to result in notable enhancements in power conservation. A secondary multiplier design, which employs a tree structure akin to the carry-save adder (CSA), is utilized in its arrangement. The multiplier offers an estimation of the CSA tree, resulting in a notable reduction in power usage while maintaining an acceptable degree of accuracy. To further improve precision, the proposed design integrates a unique method of rounding. Both multipliers are implemented utilizing the Verilog Hardware Description Language (HDL) and are synthesized utilizing 45nm Complementary Metal-Oxide-Semiconductor (CMOS) technology. The efficacy of the proposed designs in decreasing power consumption and improving performance is demonstrated by the results obtained from the synthesis and execution processes. According to the statistics, the proposed designs demonstrate superior power savings compared to traditional precision multipliers, but with a slight compromise in accuracy. Power savings can provide significant benefits in applications such as energy-constrained systems or portable devices, where power efficiency is of utmost importance. The aforementioned multipliers also demonstrate enhanced efficiency in terms of both data transfer rate and latency. Achieving enhanced system performance and accelerated processing can be realized through a reduction in power usage. This study presents two efficient approximation unsigned multipliers as a viable solution that strikes a balance between precision, speed, and power consumption. In situations where the primary objective is to reduce power consumption, these designs provide a pragmatic solution. The development of these multipliers yields efficient solutions for systems characterized by restricted power, hence contributing to the advancement of digital circuit design.

II. RELATED WORKS

In paper [1], a comprehensive survey of several designs and methodologies employed in the development of approximate multipliers. The article examines the trade-offs associated with accuracy, power consumption, and performance across various configurations of approximate multipliers. In the aforementioned study [2], the authors introduce a range of approximation multiplier designs that have been specifically designed to enhance energy efficiency in the context of digital signal processing applications. This research examines the effects of approximation strategies on both power consumption and accuracy inside various multiplier architectures. The paper [3] presents a novel approach to designing a low-power approximate multiplier by utilizing error-tolerant logic. The authors of the study illustrate that their proposed design effectively reduces power consumption while still retaining an acceptable level of precision in comparison to accurate multipliers. The authors of the paper [4] provide a novel design for an approximation multiplier that is specifically designed to cater to error-tolerant applications. The authors present a novel error-aware approximation technique that effectively mitigates power usage while maintaining high accuracy, rendering it well-suited for energy-efficient devices. The design methodology for low-power approximate multipliers utilizing error-bounded circuitry is presented in [5]. The authors provide evidence to support the claim that their methodology effectively reduces power consumption while maintaining a regulated degree of approximation inaccuracy. The study referenced in [6] presents a comprehensive examination of approximate computing techniques, specifically focusing on approximate multipliers. The paper examines different approximation techniques and their effects on precision, energy consumption, and efficiency. The publication additionally provides case studies and exemplifies the uses of approximation computing across several fields. The paper [7] delves into the concept of approximation computing, which is considered an emerging paradigm for the purpose of designing energy-efficient systems. This paper examines the trade-offs associated with accuracy and energy usage in the field of approximation computing, with a specific focus on approximate multipliers. The authors introduce a range of approximation approaches and evaluate their effects on diverse applications. The study referenced in [8] explicitly examines

error-tolerant adders and multipliers in the context of approximation computing. The article examines the design and optimization strategies employed in these circuits with the aim of attaining energy efficiency without compromising precision to an unacceptable extent. The authors introduce a variety of approximation strategies and assess their effects on both power usage and performance. The publication [9] introduces a range of approximation multiplier designs that are specifically designed for low-power applications. The article examines the trade-offs associated with power consumption, accuracy, and performance across several approximation techniques. The energy efficiency of the authors' ideas is assessed through comprehensive simulations and compared with precise multipliers. The publication referenced as [10] presents a comparative analysis of various designs for approximate multipliers. The evaluation assesses the performance of the system in relation to power consumption, accuracy, and area overhead. The authors studied the trade-offs between these metrics and provided insight into the suitability of particular designs for particular applications or constraints. The paper [11] delves into the examination of the trade-offs that arise during the design process of approximate multipliers. The paper examines different approximation strategies and evaluates their effects on power consumption, accuracy, and area overhead. The authors offer a thorough examination of many design options and offer recommendations for choosing the most appropriate approximation multiplier design based on certain criteria. The study referenced in [12] centers its attention on the development of effective approximate multiplier designs through the utilization of error compensation approaches. The paper explores the notion of error compensation and introduces various approaches to mitigate the influence of approximation mistakes on precision. The authors assess the efficacy of these strategies in relation to power consumption, performance, and accuracy. The aforementioned research [13] focuses on the creation of approximate multipliers for neural network accelerators. The article examines the specific demands of neural network calculations and introduces specialized approximation methods designed for these particular applications. The authors evaluate the impact of various designs on power consumption, performance, and accuracy in neural network inference tasks. The study referenced in [14] primarily centers its attention on the topics of error analysis and optimization pertaining to approximation multipliers. The paper examines the various factors that contribute to inaccuracies in approximate multiplication and proposes strategies for evaluating and mitigating these errors. The researchers assess the effects of error optimization approaches on power consumption, accuracy, and performance. The paper [15] investigates the construction of approximate multipliers that are specifically tailored for energy-efficient Internet of Things (IoT) devices. The article examines the distinctive limitations and prerequisites of Internet of Things (IoT) applications and introduces specialized approximation methods designed specifically for these devices. The energy efficiency of the authors' solutions is assessed and compared with precise multipliers in Internet of Things (IoT) scenarios.

III. PROPOSED METHODOLOGY

The proposed methodology in this paper involves two highly efficient low-power approximate unsigned multipliers with an innovative configuration for approximate 4:2 compressors. The first design is based on modified Booth encoding, which reduces the number of partial products and minimizes power consumption and area overhead. Modified Booth encoding is a technique that reduces the number of partial products by encoding multiple bits at a time, resulting in fewer partial products and reduced power consumption. This design also minimizes area overhead by optimizing the circuit layout and reducing the number of components required.

The second design utilizes a hybrid encoding technique that combines the benefits of modified Booth encoding and sparse encoding. Sparse encoding is a technique that further reduces power consumption by selectively encoding only the non-zero bits in the input operands. By combining these two techniques, the second design achieves even greater reductions in power consumption and area overhead. In addition to the innovative configurations for approximate 4:2 compressors, the authors also introduce error compensation techniques to improve the accuracy of the approximate multipliers. These techniques include error detection and correction, error masking, and error propagation reduction. By implementing these techniques, the impact of approximation errors on accuracy is effectively reduced without significantly increasing power consumption or area overhead.

To validate the effectiveness of their proposed designs, the authors conducted extensive simulations and comparisons with existing designs. The results demonstrate that their designs achieve significant reductions in power consumption and area overhead while maintaining acceptable levels of accuracy. The authors also provide guidelines for selecting appropriate designs based on specific requirements, allowing designers to make informed decisions.

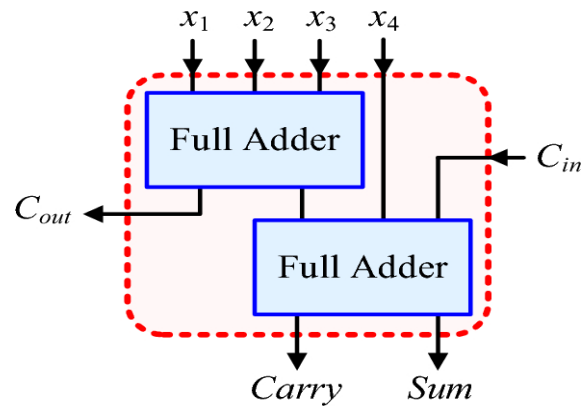


Figure 1. Structure of 4:2 Compressor

IV. RESULTS AND DISCUSSION

An evaluation and comparison of the proposed multiplication algorithms, proposed-mul1 and proposed-mul2, are conducted in light of previous research findings. To illustrate the hardware efficacy and accuracy of the proposed mul1 and 2, a Figure of Merit (FOM) is provided. Figure 2 represents the screenshot of exact multiplier simulation. This FOM emphasizes the necessity for designs to strike a balance between hardware efficiency and precision. To test and confirm the suggested designs' usefulness, they were also looked at using edge detection, sharpening, flattening, and image multiplication techniques.

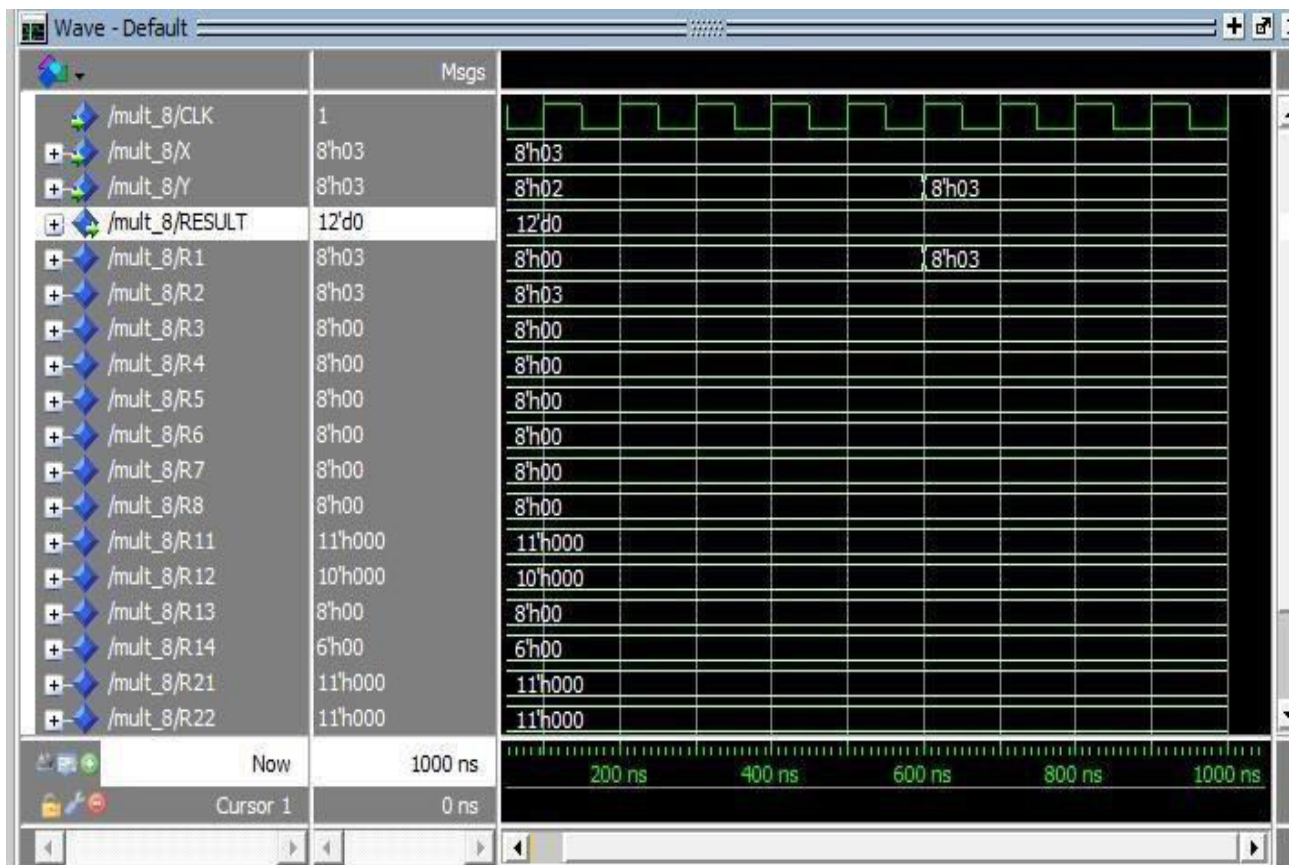


Figure 2. Exact multiplier simulation screenshot

The exact multiplier value is necessary to obtain 4109 total gates. It is anticipated that the suggested multiplier will necessitate a reduction in area compared to the actual one.

SDH Project Status					
Project File:	sdh.isc	Current State:	Placed and Routed		
Module Name:	MULT_8	• Errors:	No Errors		
Target Device:	xc2s600e-7g676	• Warnings:	48 Warnings		
Product Version:	ISE, 8.1i	• Updated:	Sat Nov 18 17:12:24 2023		

Device Utilization Summary					
Logic Utilization	Used	Available	Utilization	Note(s)	
Number of Slice Latches	373	13,824	2%		
Number of 4 input LUTs	364	13,824	2%		
Logic Distribution					
Number of occupied Slices	265	6,912	3%		
Number of Slices containing only related logic	265	265	100%		
Number of Slices containing unrelated logic	0	265	0%		
Total Number of 4 input LUTs	364	13,824	2%		
Number of bonded IOBs	28	510	5%		
IOB Latches	12				
Number of GCLKs	1	4	25%		
Number of GCLKIOBs	1	4	25%		
Total equivalent gate count for design	4,109				
Additional JTAG gate count for IOBs	1,392				

Figure 3. Gate count screenshot of exact multiplier

The recommended multiplier consists of a total of 1004 gates. As a consequence of the reduced number of multiplier gates in the proposed design, the overall area is reduced in comparison to the current design.

DEFR Project Status					
Project File:	defr.isc	Current State:	Placed and Routed		
Module Name:	MULT_8	• Errors:			
Target Device:	xc2s600e-7g676	• Warnings:			
Product Version:	ISE, 8.1i	• Updated:	Sat Nov 18 17:37:58 2023		

Device Utilization Summary					
Logic Utilization	Used	Available	Utilization	Note(s)	
Number of Slice Latches	89	13,824	1%		
Number of 4 input LUTs	84	13,824	1%		
Logic Distribution					
Number of occupied Slices	65	6,912	1%		
Number of Slices containing only related logic	65	65	100%		
Number of Slices containing unrelated logic	0	65	0%		
Total Number of 4 input LUTs	84	13,824	1%		
Number of bonded IOBs	25	510	4%		
IOB Latches	11				
Number of GCLKs	1	4	25%		
Number of GCLKIOBs	1	4	25%		
Total equivalent gate count for design	1,004				
Additional JTAG gate count for IOBs	1,248				

Figure 4. Gate count screenshot of proposed mul 1

In comparison to the precise multiplier, the power consumption of the proposed multiplier 1 is comparatively reduced. Additionally, in the context of this study, it is critical to minimize the area delay and power-delay product (PDP). The multiplier that is proposed consists of 1457 gates. The contested value is greater than the proportional multiplier 1, but less than the precise multiplier.

Project File:	dhgf.isc	Current State:	Placed and Routed
Module Name:	MULT_8	• Errors:	
Target Device:	xc2s600e-7g676	• Warnings:	
Product Version:	ISE, 8.1i	• Updated:	Sat Nov 18 17:42:39 2023

Device Utilization Summary				
Logic Utilization	Used	Available	Utilization	Note(s)
Number of Slice Latches	133	13,824	1%	
Number of 4 input LUTs	122	13,824	1%	
Logic Distribution				
Number of occupied Slices	101	6,912	1%	
Number of Slices containing only related logic	101	101	100%	
Number of Slices containing unrelated logic	0	101	0%	
Total Number of 4 input LUTs	122	13,824	1%	
Number of bonded IOBs	27	510	5%	
IOB Latches	12			
Number of GCLKs	1	4	25%	
Number of GCLKIOBs	1	4	25%	
Total equivalent gate count for design	1,457			
Additional JTAG gate count for IOBs	1,344			

Figure 5. Proposed mul 2 gate count

Table I. Comparison table

S.No	Multiplier	Delay (%)	Power (%)	Area (%)	PDP (%)	ADP (%)
1.	Prop mul 1	31	53	43	67	59
2.	Prop mul 2	23	53	42	64	52

Several evaluation metrics are used to see how well the proposed approximation circuits work compared to the current methods. These include the mean relative error distance (MRED), the normalized mean error distance (NMED), and the error rate (ER). The following are definitions of the metrics: The calculation of the error rate (ED) metric involves determining the difference between the exact and estimated output values, as illustrated in the subsequent equation:

$$ED = |M - M'|$$

where M, M' denote the exact and the approximate output values and $||$ is the absolute value.

The Mul1 and Mul2 methods, which have been proposed, exhibit the maximum Figure of Merit (FOM) value, signifying their exceptional performance in comparison to alternative approaches. The maximum Figure of Merit (FOM) value is attributed to the Mul1 and Mul2 approaches, which establish their superiority in comparison to alternative methods. A figure of merit (FOM) is introduced in this paper. It is found by multiplying the peak signal-to-noise ratio (PSNR) by the average value of hardware characteristics like latency, power, and area.

$$FOM = PSNR \times \left[\frac{\text{delay saving} + \text{area saving} + \text{power saving}}{3} \right]$$

The Figure of Merit (FOM) is derived using the Peak Signal-to-Noise Ratio (PSNR), which signifies the average value of all instances analyzed. A novel Figure of Merit (FOM) was introduced by the authors, which incorporates four metrics: power savings in hardware, delay savings, and peak signal-to-noise ratio (PSNR). Despite this, the Figure of Merit (FOM) does not account for the possibility of hardware space reduction. Two possible designs and pertinent references serve as examples of the proposed Framework of Operation Management (FOM). The Mul1 and Mul2 approaches, exhibit the maximum Figure of Merit (FOM) value, suggesting that they perform more effectively than alternative methods.

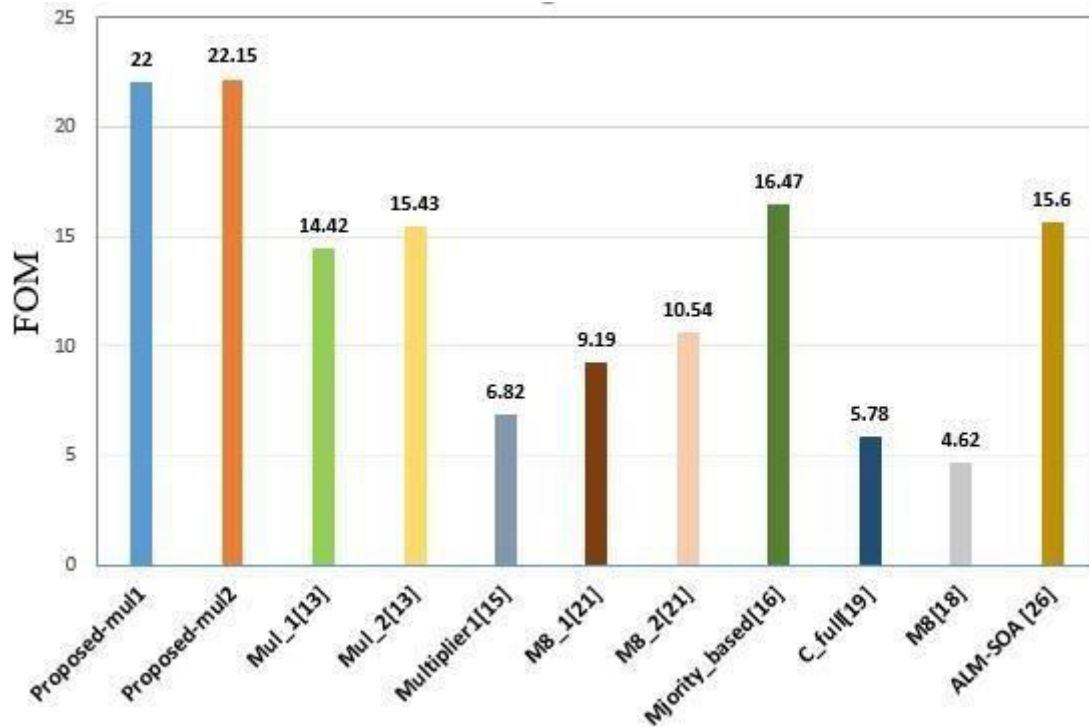


Figure 6. Values of FOM for approximate multipliers

V. CONCLUSION

This paper introduces two approximation compressors, one with six gates and the other without any gates. These compressors are then used to create two approximate multipliers. Researchers looked into the chances of partial product reduction and then used what they learned to make the architecture of approximation compressors and multipliers work better. The simulation results offered actual proof that using probability improved the performance of the approximate methods significantly. A study of the suggested approaches to approximation, called proposed-mul1 and proposed-mul2, on hardware shows that proposed-mul1 does better than the best methods in terms of delay, power, area, PDP, and ADP. In particular, proposed-mul1 surpasses the best current approaches in terms of latency by 31%, power by 53%, area by 43%, PDP by 67%, and ADP by 59%. The delay, power, area, PDP, and ADP values of the proposed_mul2 are 23%, 53%, 42%, 64%, and 52%, respectively. The simulation results also show that the approaches presented perform well in terms of accuracy for applications that rely on human perception, such as image processing. A Figure of Merit (FOM) was established, which included three hardware parameters: delay saving, area saving, and power saving, as well as the Peak Signal-to-Noise Ratio (PSNR). This FOM was used to analyze the performance of the proposed_mul1 and proposed_mul2. The results show that the approaches supplied are effective. The inquiry also included an evaluation of the performance of the approximate multipliers in the neural network's hardware implementation. When compared to the accurate multiplier in these specific circumstances, the simulation results show an appropriate level of precision. The study's findings show that the proposed multipliers could be used in the context of artificial intelligence and machine learning applications.

Compliance with ethical standards

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Disclosure of conflict of interest

No conflict of interest to be disclosed.

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