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# VLSI Architecture for Combined $R_2B$ , $R_4B$ & $R_8B$ FFT using Programmable Reversible Gate

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**ABSTRACT:** The advent of new technology in the fields of VLSI and communication, there is also an ever-growing demand for high speed processing and low area design. It is also a well-known fact that the multiplier unit forms an integral part of processor design. Due to this regard, high speed multiplier architectures become the need of the day. The FFT is enumerate is DFT and DFT is enumerate is consecutive way, it accomplishes continuous application with constant preparing when the information is persistently taken care of through the processor. In this paper, design 8-point, 16-point and 32-point FFT using combined is butterfly ( $R_2B$ ,  $R_4B$  &  $R_8B$ ) components based single path delay feedback (SDF) technique, for diminishing the computational stages and for decreasing the equipment use than the  $R_2B$  and  $R_4B$  FFT. The butterfly ( $R_2B$ ,  $R_4B$  &  $R_8B$ ) is consisting of DKG reversible gate. DKG gate is used for addition/sub-tractor of two numbers. DKG gate is depend on first input i.e. the first input is '0' then DKG is working of addition otherwise sub-tractor. The all structure is usage vertex-4 device family Xilinx programming and calculated simulation parameter i.e. number of slices, look up table and delay.

**KEYWORDS:** Reversible Gates, Adder/ Sub tractor, Fast Fourier Transform, DKG Gate

## I. INTRODUCTION

The Fourier Transform is an inevitable approach in signal processing [1], the Discrete Fourier Transform decomposes a set of values into different components of frequency. The Fast Fourier transform (FFT) is an appropriate technique to do manipulation of DFT. The algorithm of FFT was devised by Cooley and Tukey in order to decrease the amount of complexity with respect to time and computations [2].

The hardware of FFT can be implemented by two types of classifications- memory architecture and pipeline architecture. The memory architecture comprises a single processing element and various units of memory [3]. The merits of memory architecture include low power and low cost when compared to that of other styles. The specific demerits are greater latency and lower throughput. The above demerits of the memory architecture are totally eliminated by pipeline architecture at the expense of extra hardware in an acceptable way. The various types of pipeline architecture include Single delay feedback (SDF), Single delay commutator (SDC) and multiple delay commutators (MDC). The pipeline architecture is a regular structure which can be adopted by using hardware description language in an easy manner.

The algorithms of FFT can be grouped into fixed-radix, mixed-radix and split radix algorithms in a rough manner [5]. The basic categories of algorithms of FFT include - Decimation in-frequency (DIF) and the Decimation-in-time (DIT) as shown in Figure 1. Both of these algorithms depend on disintegration of transformation of an N-point sequence into many subsequences in a successive manner. There is no major difference between them as far as complexity of computation is concerned. Generally DIT deals with the input and output in reverse sequence and normal sequence respectively, while DIF deals with input and output in normal sequence and reverse sequence respectively. Only Decimation-in-Time (DIT) algorithm is taken into consideration. In this paper for implementation & result comparison, however DIT algorithm can also be use the proposed methodology.

The FFT is a run of the mill computation where the memory gets to seriously and the high parallelism is required. FFT calculation ought to have pipelined design and parallel design, be ordinary and measured. At calculation level, it should come to the multiplicative multifaceted nature as low as practical. At the structural dimension, utilize the deferral –

criticism buffering methodology to lessen the memory measure. It ought to have measured and ordinary modules, neighborhood directing and low control intricacy [5]. FFT is used to change over time space flag to recurrence area flag. It is utilized to figure the DFT adequately. To meet the superior, high speed and ongoing prerequisites of present day applications, equipment fashioners have continuously attempted to perform proficient structures for the estimation of the FFT. The pipelined equipment models are generally utilized, in light of the fact that they give high throughputs and low latencies appropriate for continuous, just as a sensibly low region what's more, control utilization.

Hence it is not possible to determine a unique input that resulted in the output zero. In order to make a gate reversible additional input and output lines are added so that a one to one mapping exists between the input and output. This prevents the loss of information that is main cause of power dissipation in irreversible circuits. The input that is added to an  $m \times n$  function to make it reversible is known as constant input (CI). All the outputs of a reversible circuit need not be used in the circuit. Those outputs that are not used in the circuit is called as garbage output (GO). The number of garbage output for a particular reversible gate is not fixed.

### II. FAST FOURIER TRANSFORM

There are two sorts concerning FFT calculation formulated by Cooley and Tukey - Decimation-in-Time calculation (DIT) and Decimation-in-Frequency calculation (DIF). The calculation of an arrangement of N-point can be acquired by methods for a double methodology. The info succession  $x(n)$  of size 'N' is disintegrated into tests of odd and even and the comparing sub-groupings  $f_1(n)$  and  $f_2(n)$  are given by:

$$f_1(n) = x(2n) \tag{1}$$

$$f_2(n) = x(2n + 1), \quad n = 0, 1, \dots, \frac{N}{2} - 1 \tag{2}$$

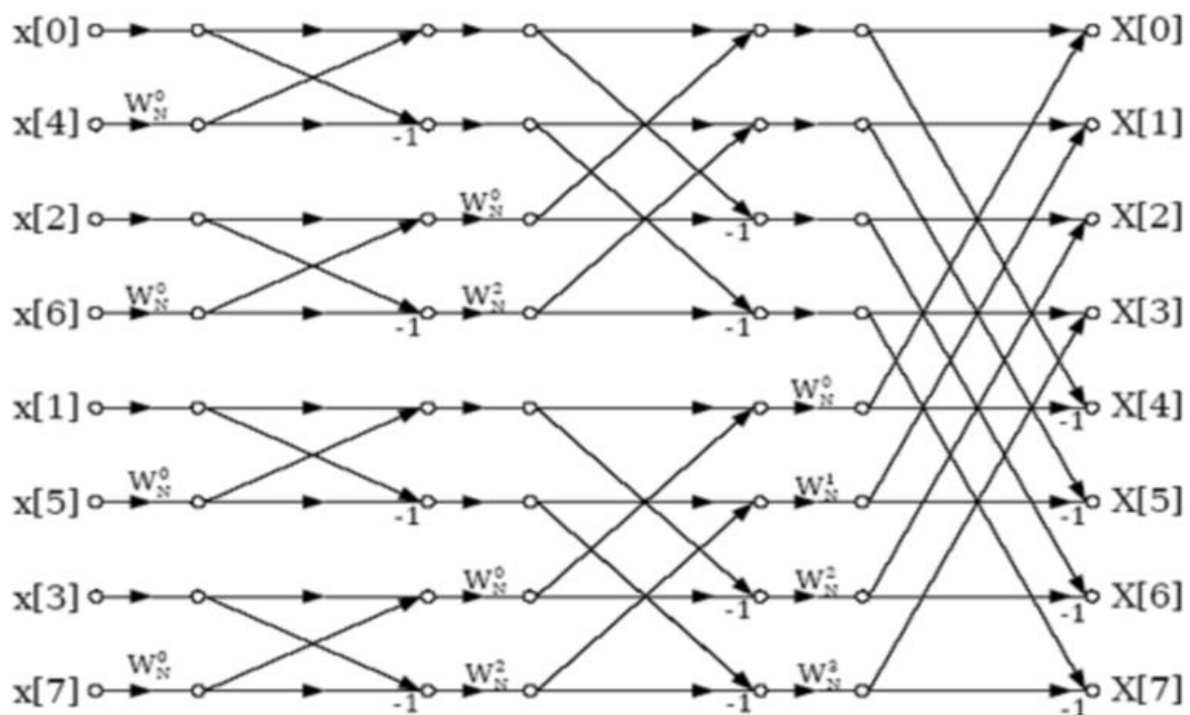


Figure 1: 8-point DIT-FFT Radix-2 Butterfly

In represent figure 1, demonstrate the termite of radix-2 DIT FFT calculation. In this figure we utilized eight sources of info and eight yields. If there should be an occurrence of DIT the info test is utilized piece inversion arrange while the yield of DIT FFT coadjuvant is produced in normal request. In represent Figure 2, demonstrate the termite of radix-2



DIF-FFT calculation. In the event of DIF the information test is utilized in common request while the yield of DIF FFT coadjutant is produced in bit turned around request.

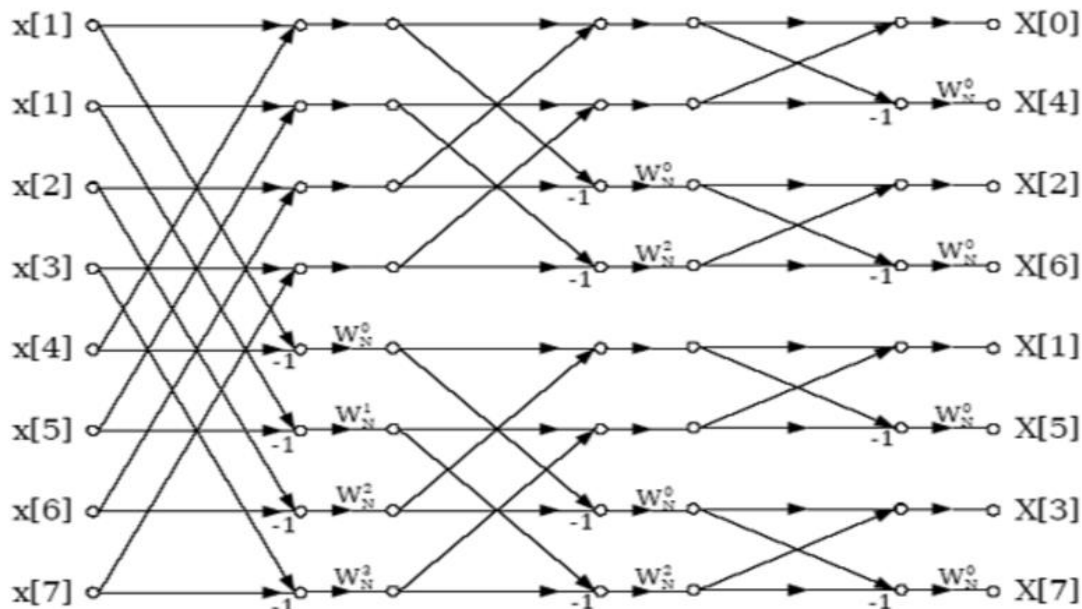


Figure 2: 8-point DIF-FFT Radix-2 Butterfly

### III. REVERSIBLE GATES

Several reversible logic gate (RLG) are utilized in past structure. Figure 3 demonstrates the Peres door (PG). A bit of the 3x3 entryways are planned for executing some basic combinational limits despite the basic limits.

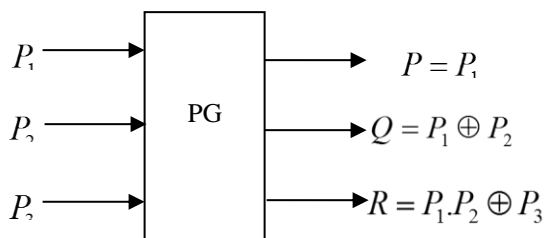


Figure 3: Block Diagram of PG

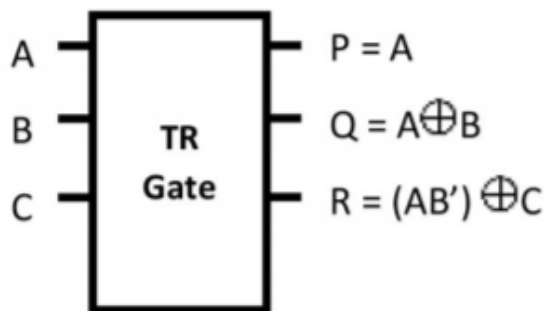


Figure 4: Block Diagram of TRG

Figure 4, shows the TRG with 3x3 system. TRG gate as working of half sub-tractor, when third input assume '0'. The RDKG is presented by figure 5. RDKG is 4x4 system representation. RDKG is working on full adder and full sub-tractor when first input assumes '0' and '1'.

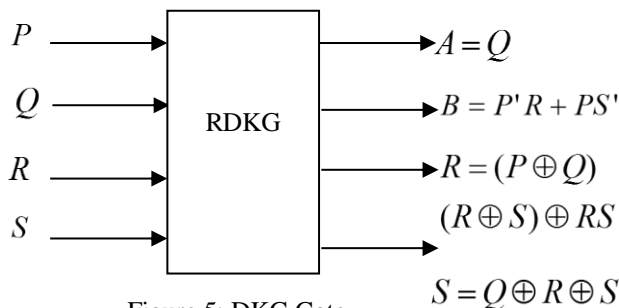


Figure 5: DKG Gate

#### IV. PROPOSED METHODOLOGY

The combined R<sub>2</sub>B, R<sub>4</sub>B and R<sub>8</sub>B based SDF FFT has been arranged in this proposed work. The united Radix of FFT configuration has a lesser proportion of computational way and moreover works on the displays of FFT processor. SDF plan, the data progressions are going through one single way. The butterfly planning part plays out the computation on the data. The extension and derivation movement is finished in butterfly parts. The changed convey select snake circuit is used for snake movement in this designing. This snake structure is very useful in this plan. The design of joined R<sub>2</sub>B, R<sub>4</sub>B and R<sub>8</sub>B FFT is showed up in Figure 6.

Figure 6 shows the 16 point SDF designing. The procedural movement of this designing is according to the accompanying; most importantly the data with documents 0 to 7 is taken care of in the move register. The R<sub>2</sub>B parts work on this data and the remainder of the data with records 8 to15.

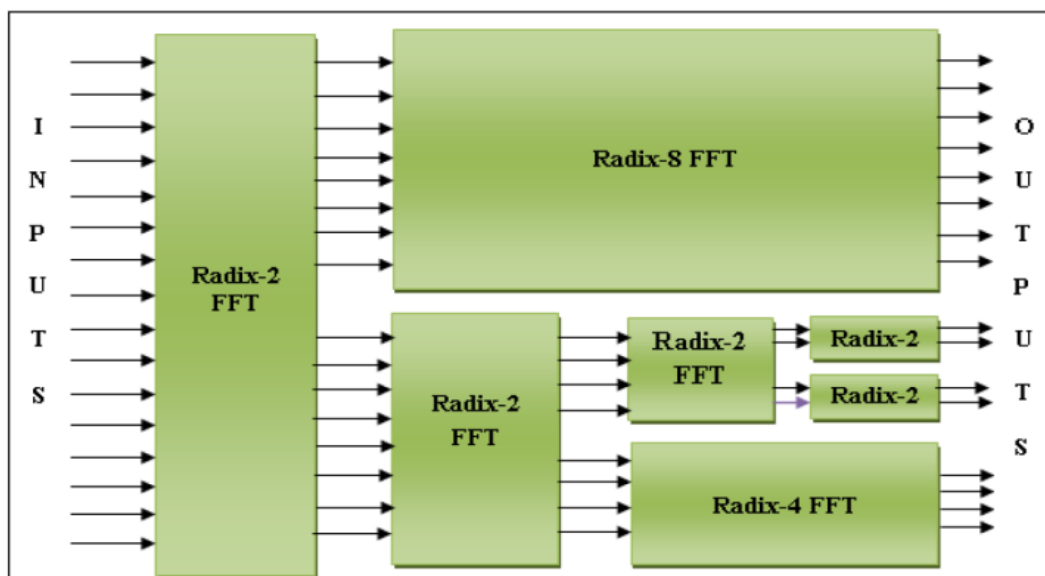


Figure 6: Structure of Combined R<sub>2</sub>B, R<sub>4</sub>B & R<sub>8</sub>B FFT

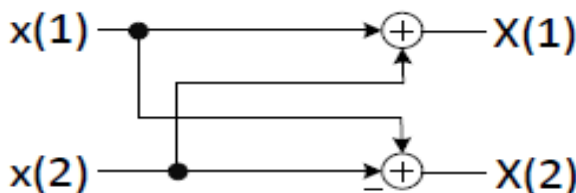


Figure 7: Radix-2 Butterfly

The expense and defer figurings are indistinguishable to the 4-bitb snake/sub tractor in figure 8. We have design 4-bit full sub-tractor/adder with the help of DKG Gate. If the fourth input of the DKG Gate is ‘0’ then output of the DKG Gate as a adder and fourth input of the DKG Gate is ‘1’ then output of the DKG Gate as a sub-tractor.

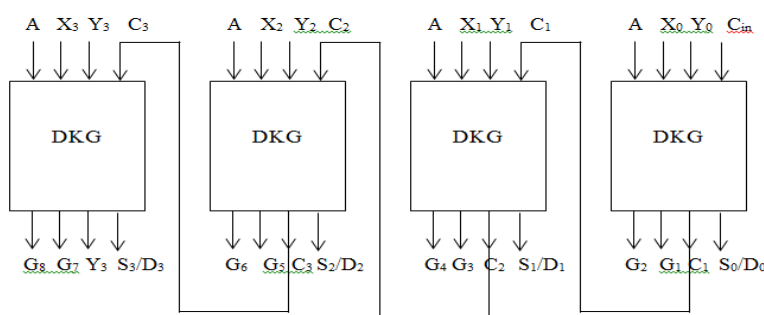


Figure 8: Reversible 4-bit Adder/ Sub tractor using DKG Gate

### V. SIMULATION RESULT

All the designing and experiment regarding algorithm that we have mentioned in this paper is being developed on Xilinx 14.5i updated version. Xilinx 14.5i has couple of the striking features such as low memory requirement, fast debugging, and low cost. The latest release of ISE™ (Integrated Software Environment) design tool provides the low memory requirement approximate 27 percentage low. ISE 14.5i that provides advanced tools like smart compile technology with better usage of their computing hardware provides faster timing closure and higher quality of results for a better time to designing solution.



Figure 9: View Technology Schematic of 8-point DIT-FFT algorithm

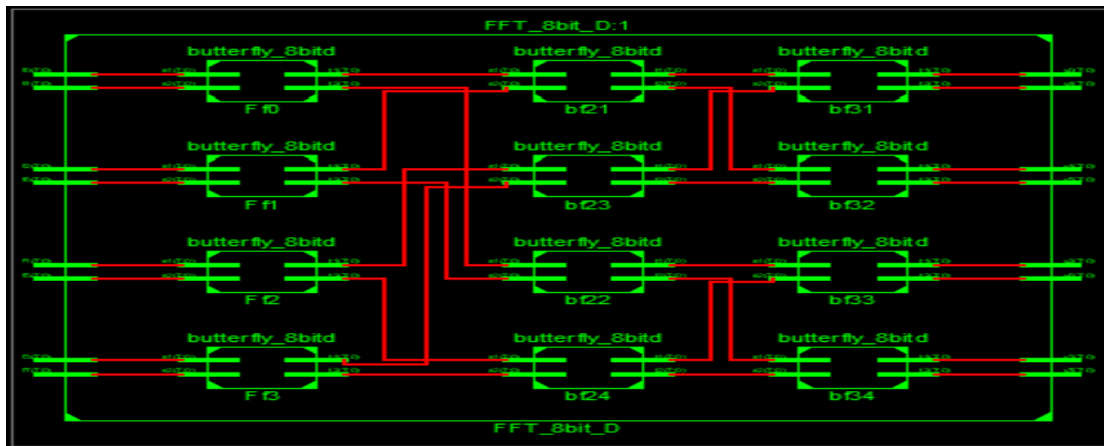


Figure 10: RTL View of DIT 8-point DIT-FFT algorithm

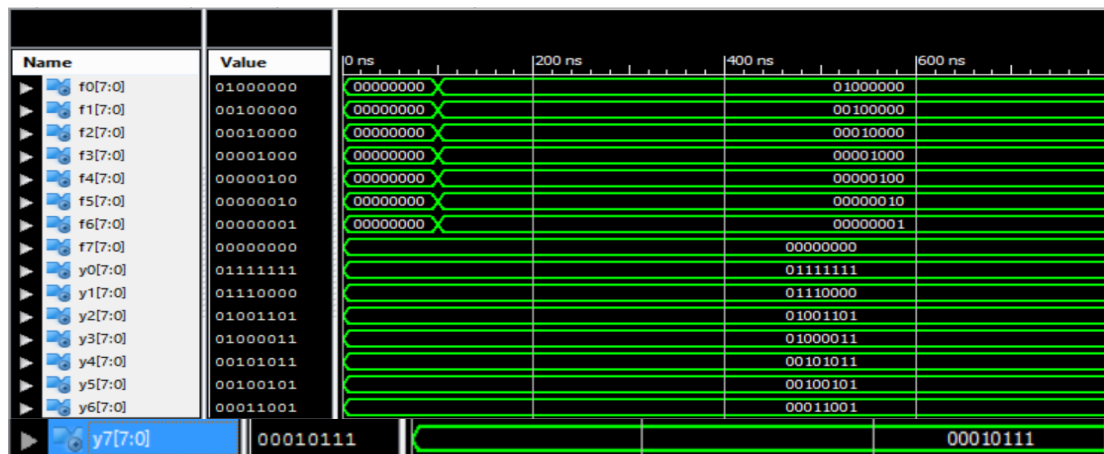


Figure 11: Output Waveform of DIT 8-point FFT using DKG Gate



Figure 12: VTS of 16-point DIT-FFT algorithm

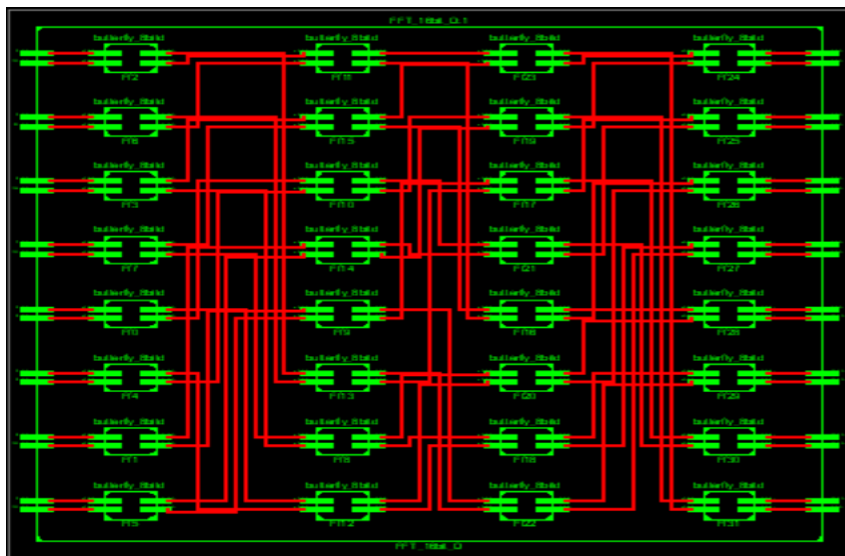


Figure 13: RTL View of DIT 16-point DIT-FFT algorithm

```

Device utilization summary:
-----
Selected Device : 4vlx200ff1513-11

Number of Slices:                514 out of 89088    0%
Number of 4 input LUTs:         923 out of 178176   0%
Number of IOs:                  256
Number of bonded IOBs:          256 out of 960    26%

Timing Summary:
-----
Speed Grade: -11

Minimum period: No path found
Minimum input arrival time before clock: No path found
Maximum output required time after clock: No path found
Maximum combinational path delay: 12.994ns
    
```

Figure 14: Device Utilization Summary of DIT 16-point DIT-FFT algorithm

```

Device utilization summary:
-----
Selected Device : 4vlx200ff1513-11

Number of Slices:                1158 out of 89088    1%
Number of 4 input LUTs:         2069 out of 178176   1%
Number of IOs:                  512
Number of bonded IOBs:          512 out of 960    53%

Timing Summary:
-----
Speed Grade: -11

Minimum period: No path found
Minimum input arrival time before clock: No path found
Maximum output required time after clock: No path found
Maximum combinational path delay: 15.278ns
    
```

Figure 15: Device Utilization Summary of DIT 32-point DIT-FFT algorithm



## VI. CONCLUSION

This research work involves the Implementation of radix-2 DIT FFT algorithm using 8-point, 16-point and 32-point algorithm by using combine  $R_2B$ ,  $R_4B$  and  $R_8B$  and programmable reversible gate for obtaining minimum delay and low area efficient in terms of LUT, Slices and MCPD.

## REFERENCES

- [1] Syeda Farhat Sultana and Basavarja Patil, "Area efficient VLSI architecture for reversible radix\_2 FFT algorithm", International Conference on Emerging Smart Computing and Informatics (ESCI), IEEE 2021.
- [2] Navin Nadar, Moksha Mehta, Kaushal Bhat, Joshua Mendes and Dr. Ravindra Chaudhari, "Hardware Implementation of Pipelined FFT using Polyphase Decomposition", International Conference on Recent Trends on Electronics, Information, Communication & Technology (RTEICT), IEEE 2021.
- [3] Shashidhara. K. S and H.C. Srinivasaiah, "Low Power and Area efficient FFT architecture through decomposition technique", International Conference on Computer Communication and Informatics (ICCCI -2017), Jan. 05 – 07, 2019, Coimbatore, INDIA.
- [4] Fahad Qureshi, Jarmo Takala, Anastasia Volkova, Thibault Hilaire, "Multiplier-less Unified Architecture for Mixed Radix-2/3/4 FFTs", 2017 25th European Signal Processing Conference (EUSIPCO), IEEE 2019.
- [5] Guilherme Ferreira; Leandro M. G. Rocha; Eduardo Costa and Sergio Bampi, "Combining  $m=2$  Multipliers and Adder Compressors for Power Efficient Radix-4 Butterfly", 63rd International Midwest Symposium on Circuits and Systems (MWSCAS), IEEE 2019.
- [6] S. Aseeri "State-of-the-Art FFT: Algorithms Implementations and Applications" Reflections on the 2018 SIAM Conference on Parallel Processing for Scientific Computing pp. 1-3 Jun 2018.
- [7] E. Konguvel and M. Kannan "A Survey on FFT/IFFT Processors for Next Generation Telecommunication Systems" Journal of Circuits Systems and Computers vol. 27 no. 03 pp. 1830001 2018.
- [8] W. Choi Kang and J. Park "Embedded DRAM- Based Memory Customization for Low-Cost FFT Processor Design" IEEE Transactions on Very Large Scale Integration (VLSI) Systems 2017.
- [9] Fahad Qureshi, Muazam Ali, and Jarmo Takala, "Multiplierless Reconfigurable Processing Element for Mixed Radix-2/3/4/5 FFTs", 978-1-5386-0446-5/17/\$31.00 ©2017 IEEE.
- [10] R. H. Neuenfeld M. B. Fonseca E. A. C. da Costa and J. P. Osés "Exploiting addition schemes for the improvement of optimized radix-2 and radix-4 fft butterflies" 2017 IEEE 8th Latin American Symposium on Circuits Systems (LASCAS) pp. 1-4 2017.
- [11] B. Silveira G. Paim B. Abreu M. Grellert C. M. Diniz E. A. C. da Costa et al. "Power-Efficient Sum of Absolute Differences Hardware Architecture Using Adder Compressors for Integer Motion Estimation Design" IEEE Transactions on Circuits and Systems I: Regular Papers vol. PP no. 99 pp. 1-12 2017.
- [12] M. Najem T. Bollengier J. C. Le Lann and L. Lagadec "A Cost Effective Approach for Efficient Time-Sharing of Reconfigurable Architectures" 2017 International Conference on FPGA Reconfiguration for General-Purpose Computing (FPGA4GPC) May 2017.
- [13] M. Z. A. Khan and S. Qadeer "A new variant of Radix-4 FFT" 2016 Thirteenth International Conference on Wireless and Optical Communications Networks (WOCN) pp. 1-4 2016.
- [14] C. A. Arun and P. Prakasam "A mathematical approach on various radix- 2i FFT algorithms" 2016 International Conference on Electrical Electronics and Optimization Techniques (ICEEOT) pp. 1040-1045 2016.
- [15] Rauf M. A. Pasha and S. Masud "A Novel split radix fast fourier transform design for an adaptive and scalable implementation" 2016 3rd International Symposium on Wireless Systems within the Conferences on Intelligent Data Acquisition and Advanced Computing Systems (IDAACS-SWS) pp. 116-121 2016.



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