



e-ISSN: 2319-8753 | p-ISSN: 2347-6710

IJRSET

International Journal of Innovative Research in
SCIENCE | ENGINEERING | TECHNOLOGY



INTERNATIONAL JOURNAL OF INNOVATIVE RESEARCH

IN SCIENCE | ENGINEERING | TECHNOLOGY

Volume 13, Issue 4, April 2024

ISSN INTERNATIONAL
STANDARD
SERIAL
NUMBER
INDIA

Impact Factor: 8.423

 9940 572 462

 6381 907 438

 ijirset@gmail.com

 www.ijirset.com

Design of Automated Coffee Making Machine Using Verilog HDL

Mr. M. Imthiaz Basha M.Tech, B. Anil Kumar Reddy, M. Dhanya Sree, M. Dinesh,

T. Ganga Prasad, N. Bindu Priya

Asst. Professor, Dept. of ECE, GATES Institute of Technology, Gooty, India

Dept. of ECE, GATES Institute of Technology, Gooty, India

ABSTRACT: A control algorithm of automated coffee machine is developed and discussed in this paper. On this basis, the control program is synthesized and implemented in the software ISE Design Suite of Xilinx. The conducted simulation studies prove the reliability of the proposed algorithm. This study and the results obtained can be used in the synthesis and implementation of the considered coffee machine.

KEYWORDS: FPGA, coffee machine, Verilog HDL, ISE Design Suite Vending Machine, Finite State Machine, Behavioural model, CAD

I. INTRODUCTION

The use of automated machines in people's daily lives allows them to save time, provide comfort and increase the quality of relevant products and services. One of the most commonly used machines is the coffee machine, which offers different types of products depending on the customer's wishes. Very often customers want coffee machines to offer a variety of different types of drinks. In this regard, it is often necessary to use and upgrade the functionality and beverages offered by a particular coffee machine. The use of programmable logic allows you to quickly and easily be able to offer this functionality and to develop coffee machines according to customer needs and thus save time in development and subsequent implementation [1].

There are different coffee machines on the market, which are realized by means of different technologies, allowing maintenance of different modes (fully automatic, semi-automatic and fully manual coffee machines). The current development proposes the control of an automated coffee machine allowing operation in 6 modes, and the modes can be increased thanks to the adopted parallel control, which allows the addition of additional products without disrupting the functionality of other products or to replace the supply of one type of product with another that does not impair the integrity and functionality of the overall block management type [1], [2].

In recent years, the large-scale introduction of programmable matrices (fpga and cpld) has allowed the construction of such devices that can be reprogrammable and can increase their functionality [3]. These devices have managed to significantly reduce development time and implement various management algorithms, while allowing troubleshooting for management problems [4].

In this paper, control algorithm for an automated coffee machine using the hardware language Verilog HDL is proposed and discussed. On this basic the developed program is successfully synthesized and implemented in the software ISE Design Suite of Xilinx. The generalized model of the synthesized coffee machine using the function RTL Schematic is illustrated. [5], [6], [7].

This paper offers an easy, convenient and inexpensive approach to synthesizing management, which allows it to be upgraded with additional programs to ensure easier application on new developments as desired by customers.

II. CONTROL ALGORITHM

A block diagram of the algorithm for control of one automated coffee machine is presented in fig. 1. The coffee machine has six modes of operations:

- Milk with sugar;
- Milk without sugar;
- Espresso with sugar;
- Espresso without sugar;
- Cappuccino with sugar;
- Cappuccino without sugar.

In each mode a certain set of processes will be performed, depending on the selected program. These processes can be as follows:

1. The machine performs a cycle, during which a cup is placed in the stand where the finished product will be;
2. Serves coffee, through which water or milk can pass, respectively;
3. A jet of milk is fed to fill the already placed glass;
4. A jet of water is fed to fill the already placed glass;
5. Putting a certain amount of sugar in the cup with the product in it;
6. Putting a stirrer in the cup with the product in it;
7. After finishing work, the vending machine signals the end and switches off, ready for the next start.

Each of the individual processes activates a corresponding timer, which is taken into account when developing the control program.

Every program is independent from other program and when is not necessary, it is make to remove

III. LITERATURE SURVEY

Based on the developed control algorithm of the proposed coffee machine (Figure 1), the design program is successfully synthesized and implemented in the ISE Design Suite software, version 14.6 of Xilinx using the hardware language Verilog HDL. The selected parameters in the design are as follows:

- Family – Spartan 6 FPGA;
- Device – XC6SLX4;
- Package – TQG144;
- Synthesis tool – XST;
- Simulator – ISim Simulator.

The input signals are as follows: clk – global timer for the different operations; btn_start – start button for setting of on/off; Espresso_without_sugar, Espresso_with_sugar, Milk_without_sugar, Milk_with_sugar, Cappuccino_without_sugar Cappuccino_with_sugar – the different modes of the machine; rst – reset; T1 ÷ T6 – timers for the different operations.

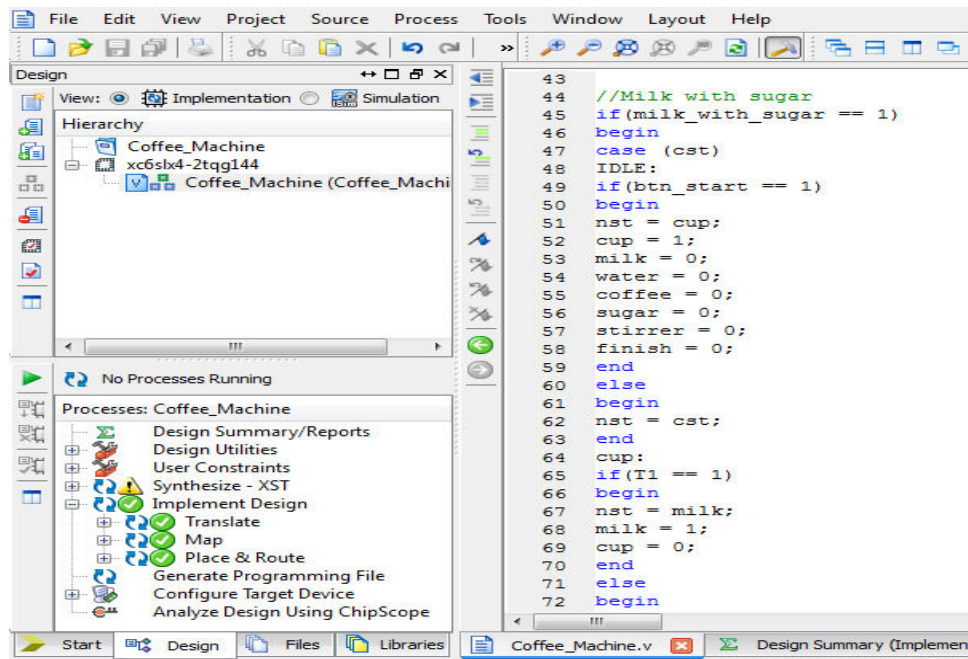
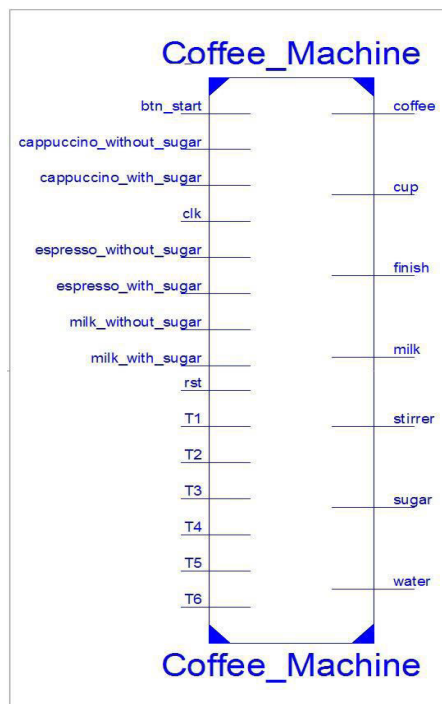


Fig. 2. Implement design of “Milk with sugar” mode in ISE Design Suite. The outputs used are: cup, water, milk, coffee, sugar, stirrer – start the different operations of the coffee system; finish – for indicates the finish process. The registers cst and nst are used for the current and next states respectively.

In fig. 2 is presented a part of the developed Verilog code for the mode of “Milk with sugar”. Similar approaches are applied for the synthesis and implementation of the other operating modes of the coffee machine.



In fig. 3 is demonstrated the model of the coffee machine using the function RTL Schematic in

IV. METHODOLOGY

Vending machines which are a common thing to be seen in shopping malls or metro stations, kind of operate by themselves. It's different from other systems since it is not a distributed system used by millions of people. It is concurrently used by one person at a time and may be used by a few thousand people a day. So we won't need features like load balancing and caching that we normally use in a system design.

Vending machine's requirements:

- Ability to select an item.
- Ability to pay for an item (Ask the interviewer which mode of payment they prefer. In this example, we will stick with cash payment).
- Dispense the item once payment is made.
- Notify the owner (serving agent) about inventory data. in case the vending machine runs low on any of the items, the owner can refill that item in the vending machine.

Design of Vending Machine

So in the system design diagram, on one side, we have our user. On the other hand, we have our vending machine which consists of two to three key components. We will split these components:

Item Selection

This component has a mapping of an item to a number so that when we select an item, it knows which item to dispense based on that mapping. We can use a **hashmap** for this purpose so that the selected button is mapped to the correct item. We can also store the items in a **matrix** format with a cards row number suggesting the button the user needs to press to get the corresponding item in that column

V. RESULT AND DISCUSSION

Some simulation results in the different modes are demonstrated in the next figures (undetected states before system activation are marked in red). After selecting the appropriate mode, press the start button (activates input signal btn_start with which the cup is placed in the stand) and start sequential execution of the set processes (fig. 1). The set times (with timers T1 ÷ T6) are random and can be changed.

Fig. 4 shows simulation results when selecting the mode "Milk with sugar". After activation of the start signal, the following processes take place in succession: adding of milk (milk – determined by T1); adding sugar (sugar – determined by T2); start the stirrer (stirrer – determined by T3) and completed mode (finish – determined by T4).

When working in mode "Espresso with sugar" (fig. 5), the following processes are performed: filling with coffee (coffee – determined by T1); running a jet of water (water – determined by T2); adding sugar (sugar – determined by T3); start the stirrer (stirrer – determined by T4) and completed mode (finish – determined by T5).

Fig. 6 demonstrates the mode "Cappuccino with sugar". The following processes take place sequentially: filling with coffee (coffee – determined by T1); adding of milk and sugar (milk and sugar – determined by T2 and T3 respectively); start the stirrer (stirrer – determined by T4) and completed mode (finish – determined by T5).



Fig. 4. Simulation results in mode of “Milk with sugar”.

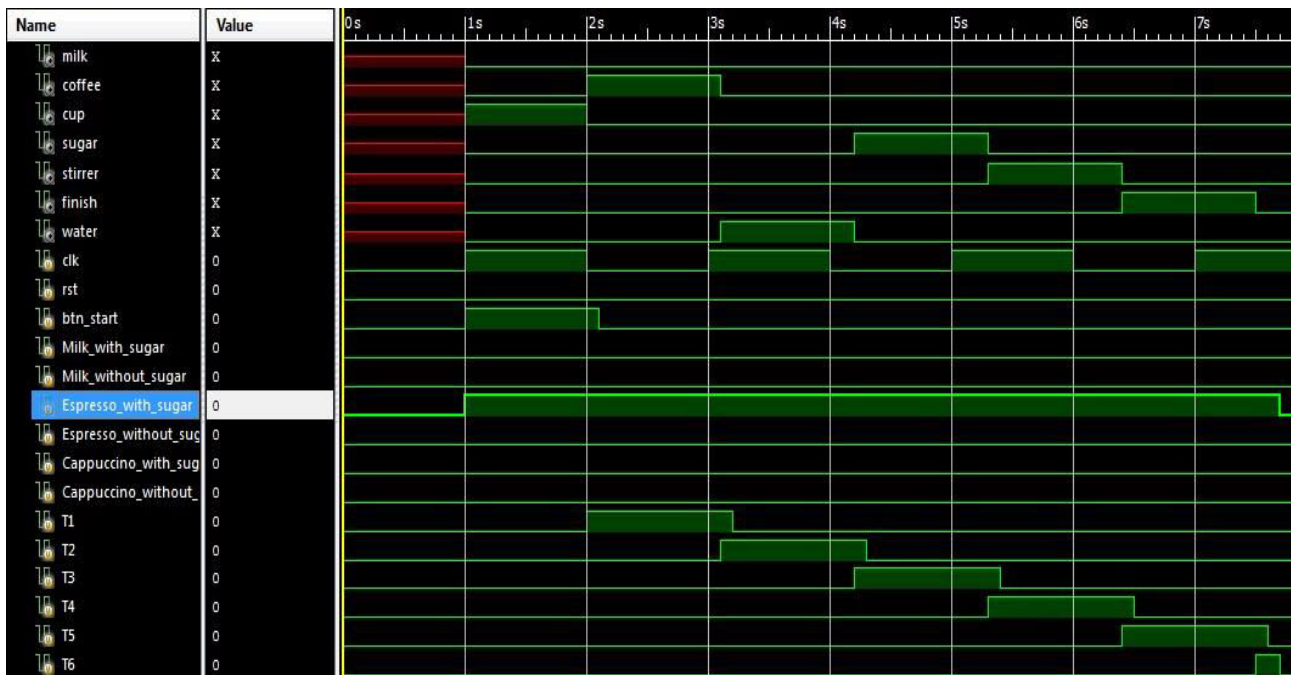


Fig. 5. Results in mode of “Espresso with sugar”.



Fig. 6. Results in mode of “Cappuccino with sugar”.

Similar approaches have been applied in the development of the control program and in other modes of operation (“Milk without sugar”; Espresso without sugar”; Cappuccino without sugar”).

VI. CONCLUSION

A control algorithm of automated coffee machine with six modes of operations is proposed and discussed. On this basis, the control program is synthesized and implemented using the hardware description language Verilog HDL. The results of the simulations show that the control has been successfully synthesized on the FPGA platform, which allows it to be successfully implemented in the production of coffee machines.

REFERENCES

[1] M. Zhilevski, V. Hristov, Design of an Automated Car Washing System with Verilog HD, HORA - 3rd International Congress on Human-Computer Interaction, Optimization and Robotic Applications, Proceedings, 2021, ISBN: 978-166544058-5

[2] M. Zhilevski, V. Hristov, Design of an automated railway crossing system with Verilog language in CPLD, IOP Conference Series: Materials Science and Engineering, 2020, Conference paper ISSN: 1757899X 17578981

[3] V. Hristov and M. Zhilevski, "Approach for Implementation of Vending Machine through Verilog HDL," 2022 International Congress on Human-Computer Interaction, Optimization and Robotic Applications (HORA), 2022, pp. 1-4

[4] V. Taraate, Digital logic design using Verilog: Coding and RTL synthesis, ISBN: 978-813222791-5, 2016, pp. 1-416.

[5] S. Ramachandran, Digital VLSI systems design: A design manual for implementation of projects on FPGAs and ASICs using verilog, 2007, DOI: 10.1007/978-81-322-2791-5

[6] Qureshi, Muhammad Ali, et al. “Design and Implementation of Vending Machine using Verilog HDL.” 2011 2nd International Conference on Networking and Information Technology, IPCSIT. Vol. 17. 2011.

[7] Minns, Peter D., and Ian Elliott. FSM-based digital design using Verilog HDL. John Wiley & Sons, 2008.



INTERNATIONAL
STANDARD
SERIAL
NUMBER
INDIA



INTERNATIONAL JOURNAL OF INNOVATIVE RESEARCH

IN SCIENCE | ENGINEERING | TECHNOLOGY

 9940 572 462  6381 907 438  ijirset@gmail.com



www.ijirset.com

Scan to save the contact details