



e-ISSN: 2319-8753 | p-ISSN: 2347-6710

# IJRSET

International Journal of Innovative Research in  
**SCIENCE | ENGINEERING | TECHNOLOGY**



# INTERNATIONAL JOURNAL OF INNOVATIVE RESEARCH

IN SCIENCE | ENGINEERING | TECHNOLOGY

Volume 13, Issue 4, April 2024

**ISSN** INTERNATIONAL  
STANDARD  
SERIAL  
NUMBER  
INDIA

Impact Factor: 8.423

9940 572 462

6381 907 438

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# Design and Analysis of Low-Power High Performance 4-Bit Parallel Shift Register Using Enhanced Triggered Low Power D-Flip Flop (EPTLFF)

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**ABSTRACT:** With increase in internet enabled smart systems, circuit miniaturization and low- operating power levels are given much priority in designing next-generation integrated circuits. Shift registers are commonly used electronic devices for data storage and transmission. The performance of a shift register depends on its internal circuitry that include type of technological node, design architecture and operating power levels. The present study focuses on the design and development of 4-bit parallel in parallel out (PIPO) shift register using enhanced pulse triggered low power (EPTL) D flip-flop. The manuscript initially demonstrates the performance of enhanced pulse triggered low power D flip-flop, that makes up the proposed 4-bit PIPO shift register using 18nm technological node yielding a minimum power consumption level  $0.75\mu\text{W}$  at an operational voltage of 0.7V. The power consumption of the individual EPTL D flip-flop is analyzed by varying operating voltages from 0.7V to 1.2V and its results are presented. Lastly, the 4-bit PIPO shift register is designed using EPTL flip-flop and its operation and performance is discussed. The designed 4-bit PIPO shift register can be operated below 1V operating voltage to yield minimal power consumption of around  $2\mu\text{W}$ . The proposed 4-bit PIPO shift register can be possibly implemented in low power energy- efficient data handling electronic devices, which has the true potential to match current industry needs. Average power, delay and power delay product of shift register (PIPO) are analysed.

**KEYWORDS:** Parallel In Parallel Out Shift Register, D Flip Flop, CMOS Design, Propagation Delay, Transistor Downscaling Low Power

## I. INTRODUCTION

The continuous downscaling of transistor physical dimensions has facilitated to increase the integrated circuit density, offering improved performance of electronic devices consistent with Moore's law [1]. However, downscaling comes at the expense of increased power dissipation. The recent surge of internet of things (IoT) enabled devices mandates the design and development of hand-held and low- power electronic devices to meet the current industry needs. IoT enabled devices require myriad sensors that rely on dynamic data storage and transmission for optimum performance. The data handling devices are principally designed to operate at minimum power levels for safe handling. Low power circuit design has been a prime force for recent IoT compatible analog and digital circuitry in the recent past [2-5]. The fundamental electronic component in data mining and data handling devices are flip flops, which are digital storage devices. It is expected that flip-flop circuitry account for 20 - 45 % of total power consumption in typical digital circuit design [6]. Thus, optimizing the flip flop circuit design is essential to achieve nominal power dissipation levels for data dependent IoT enabled electronic devices. A plethora of research has been done in this direction to minimize the flip flop circuit power consumption using varied circuit architectures [7-8]. Transmission gate flip flop (TGFF) architecture is most widely accepted design due to the absence of pre-charge; and presence of small number of internal nodes that are to be charged and discharged makes it viable for low operating power levels [9]. However, it suffers from large clock network that results in considerable dynamic power consumption even in the absence of any data activity that hinders its usage in IoT enabled devices [8]. Adaptive coupling flip flop (ACFF) design uses a single-phase clocking structure with smaller clock network and no pre-charge enables further reduction of power consumption compared to TGFF at zero data activity for higher operating voltages ( $V \geq 0.8\text{V}$ ) [10]. ACFF flip flop design relies on single- channel transmission gates and its reliability is heavily dependent on process parameters that invariably change when going to a smaller technological node for practical implementation. Enhanced pulse triggered low power (T) flip flop design are introduced to decrease

the clock signal network overloading by intelligent circuit modifications [8]. EPTL flip flops are contention free and are expected to operate at wide range of operating voltages. You et.al, recently proposed a contention free low power EPTL flip flop that is completely void of any redundant pre-charge and discharge operations which can save 80 % power consumption when compared to conventional TGFF under 10 % data activity [11]. The present manuscript analyzes the power consumption features of the EPTL D flip flop using 18nm technological node. The analysis at 18nm technological node attests to the small circuit layout of the flip flop that is compatible with present lithographical tools yielding reliable devices for nominal operation.

## II. LITERATURE SURVEY

Integrated nano electronics for the future.” While most of the electronics industry is dependent on the ever-decreasing size of lithographic transistors, this scaling cannot continue indefinitely. Nano electronics (circuits built with components on the scale of 18 nm) seem to be the most promising successor to lithographic based ICs. Molecular-scale devices including diodes, bistable switches, carbon nano tubes, and nano wires have been fabricated and characterized in chemistry labs. Techniques for self-assembling these devices into different architectures have also been demonstrated and used to build small-scale prototypes. While these devices and assembly techniques will lead to nano scale electronics, they also have the drawback of being prone to defects and transient faults. Fault-tolerance techniques will be crucial to the use of nano electronics. Lastly, changes to the software tools that support the fabrication and use of ICs will be needed to extend them to support nano electronics. This paper introduces nano electronics and reviews the current progress made in research in the areas of technologies, architectures, fault tolerance, and software tools watermarking. Here new method of using embedded technology to provide such application, Arduino is used as an embedded controller to interface Ethernet shield with a PC/Laptop to provide IoT over Ethernet. A user can use this parking service in the airport scenario provided by airport authority with user ID and password. Whenever a user need to check the vehicle in the parking lot, uses the ID and password to logon into the airport web link and view the status of the car in the parking lot using IoT. IoT Based Airport Parking System is discussed here to implement Arduino environment as IoT application.

## III. PROPOSED SYSTEM

Enhanced Pulse Triggered Low-power Flip Flop. Design Enhanced Pulse Triggered Low-power Flip Flop (EPTLFF), for high-speed operation of data storage and a popular alternative to Master slave flip-flop.

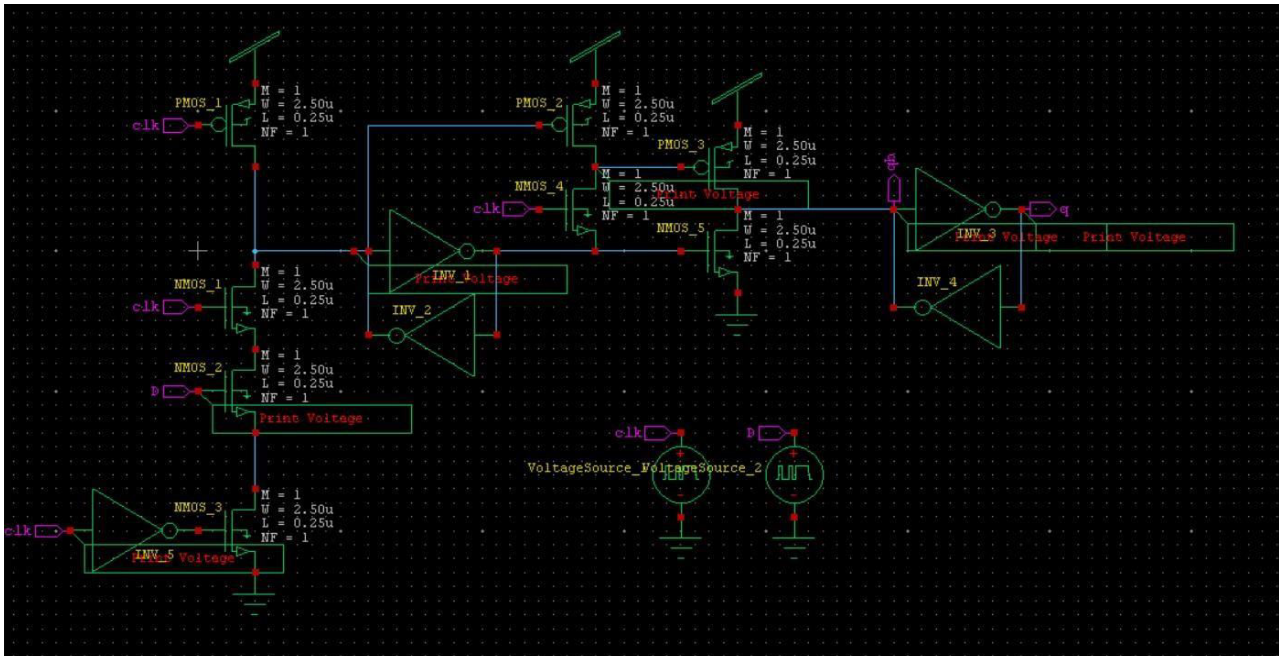
The proposed method in our project involves the use of an Enhanced Pulse Triggered Low-power Flip Flop (EPTLFF).

This design is aimed at high-speed data storage operations and serves as a popular alternative to the Master Slave Flipflop.

The enhanced pulse triggered low-power flip flop (EPTLFF) with pulse control scheme consists of pulse generator for generating Strobe signals and a latch for data storage. It reduces the number of transistors stacked in the discharging path and also reduces the overall switching delay.

The upper part latch design and lower part enhanced pulse generation. This particular clock pulse is used to a two-input pass transistor logic, N2, N3 a two-input pass transistor logic based AND gate to control the discharge of transistor N1. Since the two inputs to the AND logic are mostly complementary, the output node Z is kept at zero most of the time.





#### IV. ADVANTAGES OF PROPOSED SYSTEM

- └ Lower Power Consumption: The proposed method is expected to consume less power due to the use of fewer transistors, which is beneficial for energy efficiency and battery life.
- └ Reduced Delay: With fewer transistors, the proposed method might have a lower delay, leading to faster data transmission and improved performance.
- └ Simplicity: The use of fewer transistors could lead to a simpler circuit design, making it easier to implement and maintain.
- └ Cost-Effective: Fewer transistors mean lower costs, not only in terms of the components themselves but also in terms of the energy required to operate them.
- └ Compact Size: The proposed method might require less space on the chip due to the use of fewer transistors, which could be an advantage in applications where space is a constraint.
- └ Scalability: As technology continues to scale down, the proposed method might offer better scalability due to the smaller number of transistors.

#### V. DEVELOPMENT PROCESS

- └ Backend Development Tools: While the project is focused on backend development, it does not require programming. Instead, the emphasis is on circuit design.
- └ Tanner EDA: This is a comprehensive electronic design automation software suite used for the design purposes in this project. Tanner EDA enables the precise crafting of circuits and offers a range of tools for schematic capture, simulation, and layout.



VI. RESULT AND DISCUSSION

Flip Flop	TransistorCount	TechnologicalNode	Delay(ps)
TGFF	24	--	104.73
ACFF	22	40nm	96.47
TPSC	26	55nm	88.31
TPSC	26	45nm	79.62
EPTL (our work)	--	18nm	60.7

TABLE 1. COMPARISON OF DELAY TIMES OF THE VARIOUS HIGH SPEED FLIP FLOPS

Type of PIPO	TechnologyNode	Operational Voltage	Power consumption
PIPO using OBSC and RTPG FF[14]	90nm	1 V	52.997 μW
PIPO using EPTL FF[15]	50nm	1V	5.51 μW
PIPO using D FF[16]	16nm	0.7 V	7.48 μW
PIPO using TPSC D FF	45nm	0.7 V	5.52 μW
PIPO using EPTL D FF (our work)	18nm	0.7V	1.56 μW

TABLE 2.COMPARISON OF THE POWER CONSUMPTION FOR VARIOUS PARALLEL IN PARALLEL OUT SHIFT REGISTERS

The delay time of the designed 4-bit PIPO shift register inherently depends on the performance of the EPTL flip-flop as there are no interconnects between the flip flops in a PIPO shift register. The nominal delay calculated for the designed 4-bit PIPO shift register is 60.7ps at 0.7V and increases to 80.7ps at 1.2V, consistent with (2). It is to be noted that at smaller technological nodes, the leakage current becomes dominant over switching power due to process and quantum related effects. The observed low power consumption of ~3 μW and a delay time of 60ps at 18nm technological node suggests that the designed 4-bit PIPO shift register seems to be a practically feasible operation of making low power high performance integrated circuits.

VII. CONCLUSION

Utilizing an Enhanced Pulse Triggered Low Power Flip-Flop (EPTLPFF) instead of a True Single Phase Clock Flip-Flop (TSPCFF) leads to a reduction in the number of transistors within the circuit.

Consequently, this minimizes both the power consumption and the overall delay. The EPTLPFF achieves greater efficiency by employing a dynamic structure that allows for the latching of data only when necessary, thereby conserving energy.

Moreover, the simplified transistor network not only reduces the complexity of the design but also enhances the



reliability of the circuit. This approach is particularly beneficial in applications where power efficiency is paramount, such as in battery-operated devices and large-scale integrated circuits.

To summarize, a 4-bit parallel in parallel out shift register is designed using enhanced pulse triggered low power D flip flop. The significance of the key parameters including the power consumption and delay of the designed circuits are carefully analysed.

The designed 4-bit PIPO shift register consumes less than  $3\mu\text{W}$  of power and a nominal delay of  $60\text{ps}$  at operational voltages less than 1V, making it as an ideal candidate to be used for lowpower high performance portable internet enabled electronic circuits and systems.

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