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# Design an Efficient Braun Multiplier Using KSA Based Pass Transistor Logic Using 22nm

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**ABSTRACT:** The Braun multiplier is a well-established and widely recognized array multiplier architecture that has gained popularity due to its inherent simplicity, structural regularity, and efficient mechanism for partial product generation. These characteristics make it a highly favourable choice in the design of digital circuits, particularly in applications where predictable and uniform hardware structures are essential. Traditionally, Braun multipliers have been effectively utilized in various arithmetic operations within digital systems; however, with the continuous evolution of modern computing systems, there has been an increasing demand for designs that offer not only high computational speed but also reduced power consumption and enhanced overall performance.

In response to these emerging requirements, the integration of a Kogge-Stone Adder (KSA) into the Braun multiplier architecture, along with the implementation of advanced Pass Transistor logic technology at the 22nm scale, represents a significant and innovative advancement over conventional multiplier designs. The inclusion of the KSA improves the speed of the final addition stage, which is critical in large-bit-width multipliers, due to the parallel prefix structure of the KSA that minimizes the carry propagation delay. Furthermore, leveraging 22nm CMOS technology allows for more compact, power-efficient, and faster circuits, which are highly desirable in the design of high-performance digital systems.

**KEYWORDS:** Pass Transistor Logic, Braun multiplier, Kogge Stone Adder, Area consumption, , Parallel Prefix Adder, 22nm Technology, Tanner EDA.

## I. INTRODUCTION

The Braun multiplier is a well-established and widely recognized array multiplier architecture that has gained popularity due to its inherent simplicity, structural regularity, and efficient mechanism for partial product generation. These characteristics make it a highly favourable choice in the design of digital circuits, particularly in applications where predictable and uniform hardware structures are essential. Traditionally, Braun multipliers have been effectively utilized in various arithmetic operations within digital systems; however, with the continuous evolution of modern computing systems, there has been an increasing demand for designs that offer not only high computational speed but also reduced power consumption and enhanced overall performance. In response to these emerging requirements, the integration of a Kogge-Stone Adder (KSA) into the Braun multiplier architecture, along with the implementation of advanced Pass Transistor logic technology at the 22nm scale, represents a significant and innovative advancement over conventional multiplier designs. The inclusion of the KSA improves the speed of the final addition stage, which is critical in large-bit-width multipliers, due to the parallel prefix structure of the KSA that minimizes the carry propagation delay. Furthermore, leveraging 22nm CMOS technology allows for more compact, power-efficient, and faster circuits, which are highly desirable in the design of high-performance digital systems. Keywords – Pass Transistor Logic, Braun multiplier, Kogge Stone Adder, Area consumption, , Parallel Prefix Adder ,22nmTechnology,Tanner EDA..

## II. PROPOSED SYSTEM

The new Braun Multiplier using Kogge Stone Adder design now uses 22nm technology transistors.

In 22nm technology, the transistors have a much smaller channel length, significantly reducing area consumption and improving efficiency.

The system now uses fewer transistors—down from the original 276—resulting in less circuit complexity, lower power consumption, and faster operation.

Building a Better Braun Multiplier:

After testing the adders, researchers used them in a 4-bit Braun Array Multiplier (BAM).

The version of PTL, was used to build a BAM, and the performance was compared.

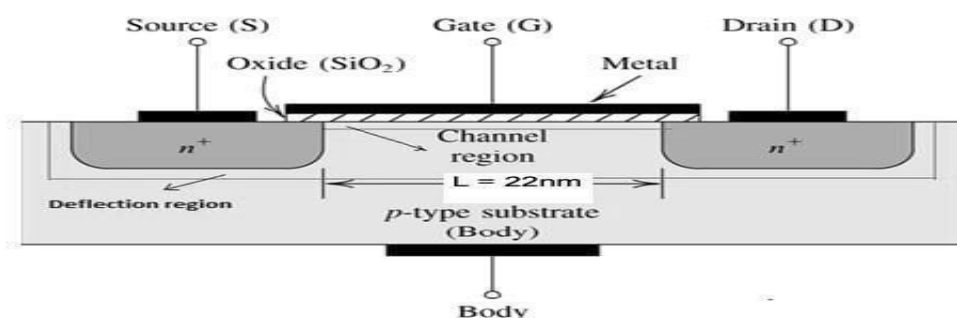
The results? All designs worked well, but one stood out.

Results for the PTL KSA (in 22nm):

Power usage: lower than in the 120nm version due to better transistor performance

Area: more compact layout compared to 120nm design

Delay: overall delay will be reduced to



With growing demand for faster and smaller electronics, efficient circuit design is more important than ever.

This study proves that by rethinking how we build multipliers, we can save space, reduce power, and increase speed all without sacrificing performance.

Now, using 22nm technology, we take a big step forward in chip design. Smaller, faster, and more energy-efficient circuits are no longer the future they're the present

## III. EXPERIMENTAL RESULTS

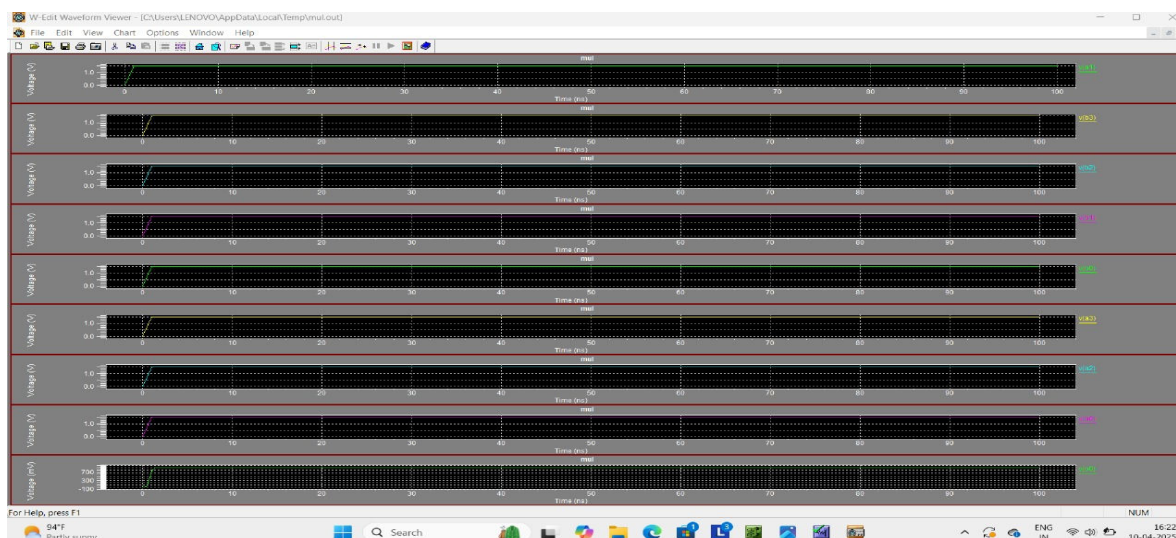


Fig 1: Input Waveforms





Fig 2: Output Waveforms



Fig 3: Delay Outputs

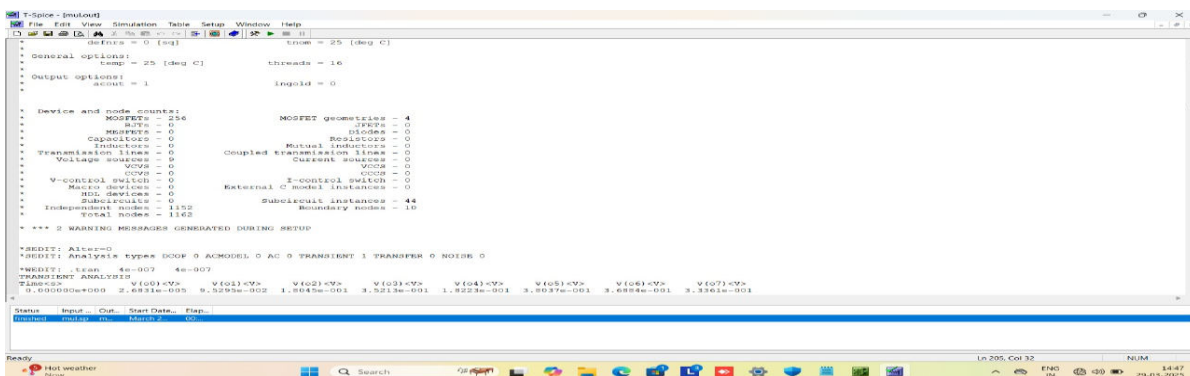


Fig 4: Transistor count output

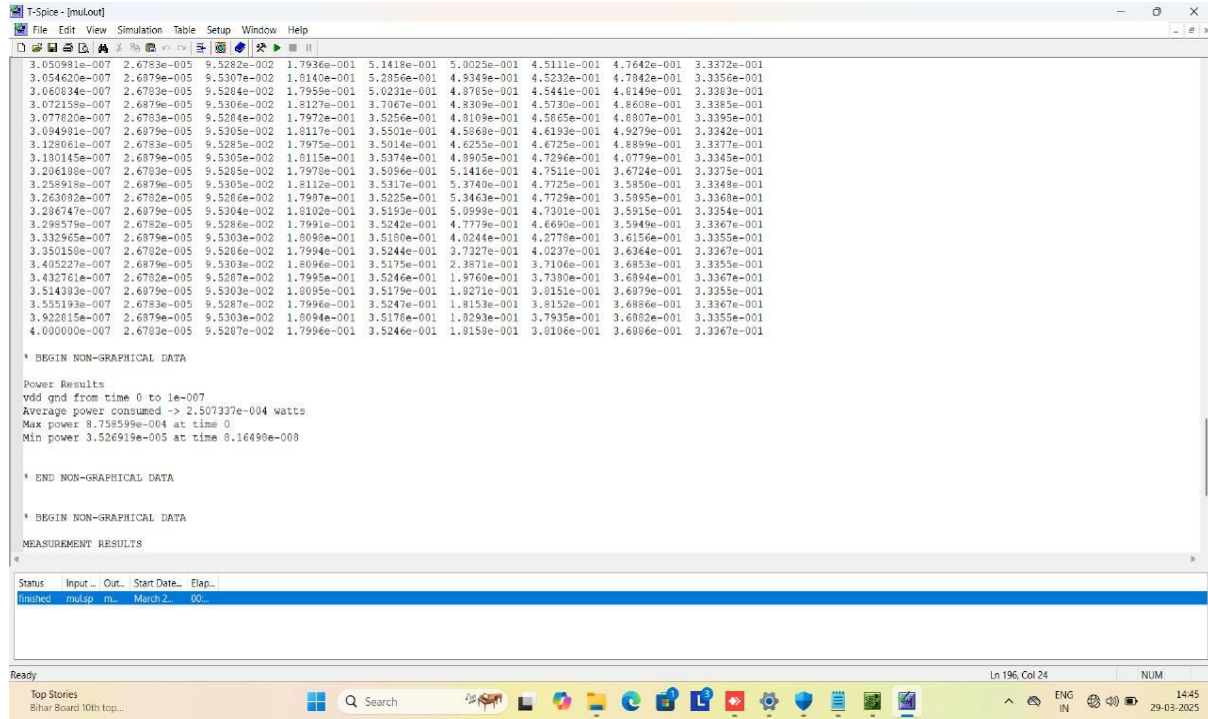


Fig 5 Power consumption output

#### IV.CONCULSION

This project involved designing a Braun Multiplier using a Kogge-Stone Adder (KSA) combined with pass transistor logic (PTL), targeting 22nm Pass Transistor technology in Tanner EDA. The design aimed to achieve high speed and low power by using the regular and modular structure of the Braun Multiplier, the fast performance of the KSA, and the area-saving benefits of PTL. Simulation results confirmed that the multiplier worked correctly and showed improvements in speed, area, and power usage compared to traditional CMOS designs. Using PTL reduced the number of transistors, which helped decrease unwanted capacitance and increase switching speed. The KSA, with its efficient carry propagation, further boosted the overall speed. The use of 22nm technology also improved the design by allowing for a smaller, more power-efficient layout. The final design passed all DRC (Design Rule Check) and LVS (LayoutVersus Schematic) checks in Tanner EDA, with very low leakage, proving that the approach is suitable for VLSI applications. In summary, combining the KSA and PTL in the Braun Multiplier provides a fast, compact, and low-power solution for modern digital systems.

#### REFERENCES

1. "Design an Efficient Braun Multiplier Using KSA Based CMOS Logics"  
Authors: Daphni S, Vijula Grace K. S, Judith Johnsi J, Bamini S
2. "Design of Low Power 4-Bit CMOS Braun Multiplier Based on Threshold Voltage Techniques"  
Author: Dayadi Lakshmaiah
3. "Design of Braun Multiplier with Kogge Stone Adder & Its Implementation on FPGA"  
Authors: Ms. Madhu Thakur, Prof. Javed Ashraf
4. "Design of High-Speed Low Power Computational Blocks for DSP Processors"  
Author: Sai Prasad Goud
5. "Efficient Serial Multiplier Design using Ripple Counters, Kogge-Stone Adder and Full Adder"  
Authors: S. Sangeetha, S. S. R. Kumar
6. "Design and Performance Analysis of Multipliers Using Kogge Stone Adder"  
Authors: Neeraja Bandi, R. Sai Prasad Goud

7. " An Optimized 4×4 Braun Multiplier for Parallel Processing Architectures with a 3-bit KSA Adder"  
*Authors:* M. Sakthimohan, Elizabeth Rani G, Monisha P, Nandhini S
8. " Design and Implementation of Braun Multiplier using Verilog: Review"  
*Authors:* Anukrati Sharma, Aparna Mittal, Anshika Singh, Raman Kapoor
9. " Design Analysis of Wallace Tree Based Multiplier Using Approximate Full Adder and Kogge Stone Adder"  
*Authors:* Navin Kumar M, Adithyaa R S, Bhavan Kumar D, Pavithra T
10. S. S. Sapatnekar, "**Timing Analysis and Optimization of Sequential Circuits**," Springer Science & Business Media, 2012.
11. P. Gupta, A. B. Kahng, P. Sharma, and D. Sylvester, "**Selective Gate-Length Biasing for Cost-Effective Runtime Leakage Control**," IEEE Transactions on Computer



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