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64-Bit FPGA based ALU Employing Reversible Logic

Dr. G. Harinatha Reddy¹, Srisailam Bhavya Sree², Cheelasani Ruchitha³,

Yatham Adi ShankarReddy⁴, Sirigiri Venkata Praveen Kumar⁵

Professor & Head, Dept. of ECE, NBKR Institute of Science & Technology, Vidyanagar, India¹

U. G. Student, IV B.Tech (ECE) , Dept. of ECE, NBKR Institute of Science & Technology, Vidyanagar, India²⁻⁵

ABSTRACT: The Arithmetic Logic Unit (ALU) is a critical component in digital system design, responsible for executing fundamental arithmetic and logical operations. This project presents the design and implementation of a 64-bit ALU utilizing reversible logic gates, developed using Verilog Hardware Description Language (HDL) and synthesized on the Xilinx ISE 14.7 platform using an FPGA development board. Reversible logic gates, characterized by their ability to uniquely map input vectors to output vectors and vice versa, mitigate issues such as data loss and excessive power dissipation commonly encountered in conventional (irreversible) logic circuits. By leveraging reversible logic, the proposed ALU design achieves notable improvements in speed and power efficiency over traditional gate-based architectures. A comprehensive library of reversible gates including AND, OR, NAND, NOR, and XOR was designed in Verilog HDL to construct the core components of the ALU. These include a full adder, full subtractor, 2:4 decoder, 3:8 decoder, multiplier, and comparator. The functionality and performance of the proposed ALU were validated through synthesis and simulation using the Xilinx Vivado design suite. The results confirm the ALU's suitability for low-power Very Large Scale Integration (VLSI) applications, demonstrating clear advantages over conventional ALU designs in terms of energy efficiency and operational speed.

KEYWORDS: Reversible gates, Verilog HDL, Feynman gate, Peres gate, Toffoli gate, Fredkin gate, Arithmetic Logic Unit.

I. INTRODUCTION

The widespread deployment of microprocessors and digital signal processors has led to a continuous demand for high-performance arithmetic hardware, positioning it as a critical and ongoing challenge in computer architecture. At the centre of this innovation lies the Arithmetic Logic Unit (ALU) a core element that serves as the processing engine of any computing system. The ALU is responsible for executing both arithmetic and logical operations essential for system functionality. It performs key operations such as addition, subtraction, multiplication, division, and logic operations like AND, OR, XOR, and NOT. The performance of the ALU directly impacts the speed, power efficiency, and parallelism of the processor. To meet the growing requirements of modern computing applications including scientific simulations, AI systems, and embedded applications ALUs are designed with a focus on speed optimization and low power consumption, often incorporating advanced techniques like pipelining, parallelism, and custom instruction sets. In today's processors, cache memory plays a pivotal role in accelerating computation. Acting as a high-speed buffer, it stores frequently used data and instructions, significantly reducing the time to access slower main memory. This results in a more responsive processor with improved throughput and computational efficiency. Cache and ALU together contribute to improved data handling, execution speed, and energy efficiency, laying the foundation for optimized performance across all modern computing domains. This work focuses on the design and implementation of functional blocks of a 64-bit ALU using Verilog HDL, targeting VLSI and ASIC-based systems. The ALU is designed as a combinational logic unit capable of performing key arithmetic and logic operations and is a fundamental building block in digital system design. With the trend towards miniaturization and complexity, modern ALUs are becoming more compact while offering enhanced performance. These are frequently used in both general-purpose processors and application-specific systems.

A. Overview of the ALU

An ALU is a digital circuit that processes binary integers through arithmetic and bitwise logical functions. In this design:

- The ALU performs addition, subtraction, logic functions, and comparisons.
- A multiplexer selects the required operation based on control lines.
- For arithmetic operations, three inputs A, B, and Cin are used.
- Logic functions generally require only A and B.

B. Arithmetic Operations

Arithmetic forms the backbone of all numerical computation. The ALU supports:

- Addition and Subtraction: Implemented using full adders/subtractors.
- Comparison: Includes greater than, less than, and equal to operations.
- These functions are fundamental in CPUs and digital controllers.

The arithmetic unit is designed for accuracy, low latency, and scalability for 64-bit processing, supporting applications requiring higher numerical precision.

C. Logical Operations

The logical unit executes bitwise operations, which are key in:

- Data masking
- Bit manipulation
- Conditional logic evaluation

Supported operations: AND, OR, NOT, XOR Each gate was coded in Verilog HDL, verified independently, and integrated into the ALU core. Logic gates form combinational circuits, which are the building blocks of complex logical functionality. These gates enable execution of Boolean functions that define the logic behaviour of the ALU.

II. LITERATURE SURVEY

Recent advancements in Arithmetic Logic Unit (ALU) design have emphasized optimizing performance metrics such as speed, power consumption, and chip area. Ravindran and Regeena (2015)[1] proposed a 16-bit ALU utilizing a combination of CMOS, pseudo-NMOS, and Pass Transistor Logic to enhance performance, employing a Carry Skip Adder configuration validated through DSCH and Microwind tools. Kumar and Singh (2021)[2] introduced a 4-bit ALU based on Complementary Energy Path Adiabatic Logic (CEPAL), achieving a 55% improvement in power efficiency over conventional CMOS designs at 100 MHz and 2.5 V, with analysis conducted using Tanner EDA tools and 250 nm technology libraries. In embedded systems, Rengasamy et al. (2013)[3] focused on reducing power consumption in a 16-bit ALU by activating only one functional unit at a time, optimizing key modules like the adder and multiplier using a Carry Look Ahead Adder and column bypassing techniques, respectively, with the entire design implemented in Verilog HDL. Buddhini and Wijesinghe (2016)[4] detailed the design and hardware implementation of a simple 16-bit RISC processor on a Xilinx Spartan-3E FPGA, capable of performing basic ALU operations, modelled using Verilog and featuring a stack-based I/O transfer system with a simplified instruction set for efficient execution and re-programmability. Collectively, these studies underscore the importance of strategic design choices in ALU development, leveraging various logic families, adiabatic logic, and architectural optimizations to enhance performance while minimizing power consumption and chip area.

III. PROPOSED METHOD

The proposed 64-bit Arithmetic Logic Unit (ALU) leverages reversible logic gates to address power dissipation and heat generation challenges inherent in traditional ALUs, particularly within Very Large-Scale Integration (VLSI) designs. By employing gates such as Feynman, Toffoli, Fredkin, Peres, and Haghparast-Navi (HNG), the design ensures lossless computation, thereby minimizing energy loss and enhancing efficiency. The ALU supports 16 arithmetic and logic operations, controlled via a 4-bit signal, and features a modular architecture composed of cascaded 1-bit reversible units to handle 64-bit operands. This structure facilitates scalability while maintaining performance and energy efficiency. Key functional units include the Arithmetic Unit for operations like addition and multiplication, the Logical Unit for operations such as AND and OR, the Shift and Rotate Unit, and the Comparison and Selection Unit. Collectively, these units contribute to reduced computational delay, high fault tolerance, and minimal signal

degradation. The reversible ALU's design aligns with green computing objectives and is well-suited for applications in digital signal processors, low-power devices, general computing, and emerging technologies like quantum computing. Furthermore, the design emphasizes optimization parameters such as minimizing constant inputs, garbage outputs, and quantum cost, which are critical for efficient reversible computing. Experimental implementations using platforms like Xilinx 80nm technology have demonstrated significant reductions in area and delay compared to conventional designs. These enhancements not only improve computational efficiency but also make the ALU highly suitable for integration into advanced computing systems, including those requiring Multiply and Accumulate (MAC) operations common in artificial intelligence and real-time processing applications

Control signal	Operation
0000	sum
0001	$a - b$
0010	$a * b$
0011	$a \mid b$
0100	$\sim a$
0101	R0
0110	$\sim(a \wedge b)$
0111	$\sim(a \& b)$
1000	32'd0
1001	$\sim(a \mid b)$
1010	$a \& b$
1011	IO STS
1100	INC
1101	$b * 1$
1110	$a \wedge b$
1111	$a * 1$

Table. 1. 16 operations using 4-bit control signal

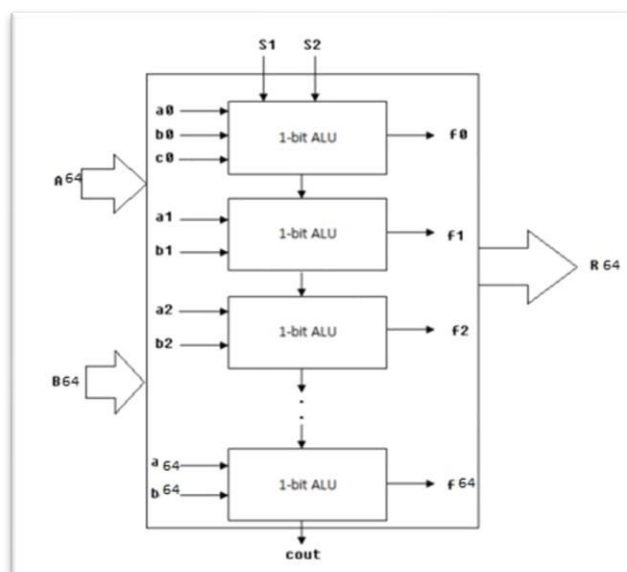


Fig. 1. Block Diagram of 64-bit ALU

IV. EXPERIMENTAL RESULTS

The implementation of a 64-bit FPGA-based Arithmetic Logic Unit (ALU) utilizing 4-bit control signals and reversible logic gates including Peres, Fredkin, Feynman, and Toffoli gates has demonstrated significant improvements in key performance metrics. The design efficiently performs 16 arithmetic and logical operations with minimal computational delay, making it well-suited for high-performance computing. In terms of resource utilization, the design uses only 468 Slice LUTs and 192 Slice Registers, confirming its area-efficient nature. Timing analysis indicates a maximum delay of 16.585 ns with no constraint violations, suggesting a well-balanced and stable architecture. All critical paths are optimized with manageable logic and net delays, ensuring effective data propagation across the system. The power analysis reveals a total consumption of 39.787W, with a junction temperature of 99.4°C. While this value may appear high, it is an anticipated result given the system's purpose of handling 64-bit wide arithmetic and logic operations. The design also exhibits low static power consumption (0.795W) and efficient usage of logic resources, reinforcing its potential for low-area VLSI systems. This study demonstrates that the integration of reversible logic with 4-bit control signals not only enhances operational flexibility but also contributes to optimized power and area performance. With appropriate power constraint tuning and further optimization, this reversible ALU architecture is scalable and accurate, showing excellent promise for next-generation, low-power, high-speed digital systems.

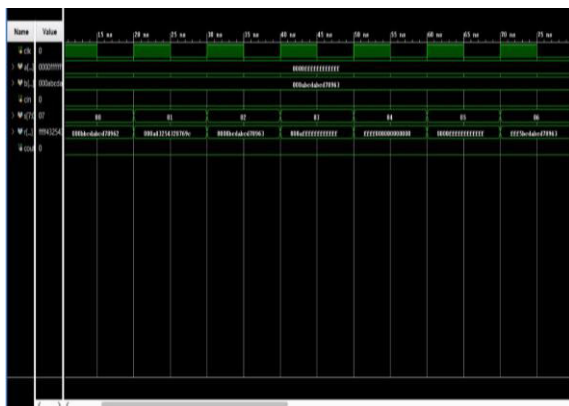


Fig. 2. Simulation Waveforms of 64-bit ALU

Name	Slice LUTs (134600)	Slice Registers (269200)	Bonded IOB (400)	BUFGCTRL (32)
ALU_REVERSIBLE_64	468	192	199	1
a1 (ALU_reversiblegates)	6	3	0	0
a2 (ALU_reversiblegates_10)	8	3	0	0
a3 (ALU_reversiblegates_21)	6	3	0	0
a4 (ALU_reversiblegates_32)	7	3	0	0
a5 (ALU_reversiblegates_43)	5	3	0	0

Fig. 3. Area Values of 64-bit ALU

Design Runs		Timing	Power	Utilization							
Unconstrained Paths - NONE - NONE - Setup											
Name	Slack	Levels	Routes	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Requirement	Source Clock
Path 1	29	30	7	a[1]	cout		16.585	6.077	10.508	input port clock	
Path 2	28	29	7	a[1]	a62/result_reg/D		13.580	3.717	9.863	input port clock	
Path 3	28	29	7	a[1]	a63/result_reg/D		13.580	3.717	9.863	input port clock	
Path 4	28	29	7	a[1]	a65/result_reg/D		13.580	3.717	9.863	input port clock	
Path 5	28	29	7	a[1]	a64/result_reg/D		13.551	3.717	9.834	input port clock	
Path 6	27	28	7	a[1]	a59/result_reg/D		13.128	3.612	9.516	input port clock	
Path 7	27	28	7	a[1]	a58/result_reg/D		13.117	3.612	9.505	input port clock	

Fig. 4. Delay Values of 64-bit ALU

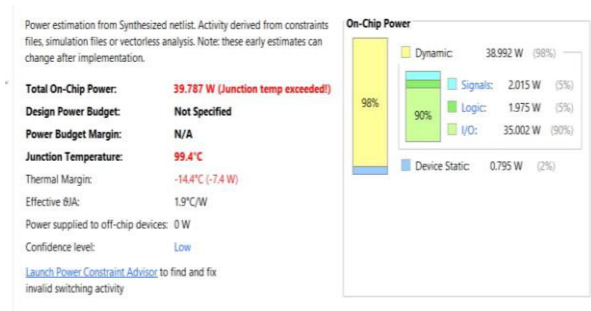


Fig. 5. Power Values of 64-bit ALU

V. CONCLUSION

The proposed 64-bit FPGA-based ALU employing reversible logic showcases substantial improvements in computational efficiency, reduced power dissipation, minimized chip area, and optimized delay. By integrating reversible logic gates such as Peres, Fredkin, Feynman, and Toffoli, the ALU efficiently performs 16 arithmetic and logical operations while significantly lowering energy consumption. The implementation of both 64-bit and 32-bit

Reversible ALUs highlights the superior performance of reversible logic when compared to conventional irreversible logic designs. The comparative analysis reveals notable reductions in power dissipation, area(no. of LUTs), and logic delay achieved by utilizing 4-bit control signals with reversible logic gates. This demonstrates the effectiveness of the proposed approach for low-power VLSI applications. Moreover, the shift from traditional 1-bit control signals to 4-bit reversible logic control enhances operational flexibility and efficiency. Beyond ALU design, this work underscores the versatility of reversible logic in broader digital design applications, such as encoders and other complex circuits. The incorporation of additional reversible gates like CNOT, DNG, and HNG further emphasizes the potential to optimize power, delay, and area in future designs. In summary, this research establishes the superiority of reversible logic in modern computing architectures, offering a promising direction for the development of energy-efficient, scalable, and sustainable digital systems. The innovations presented in this project pave the way for next-generation low-power FPGA-based solutions in advanced computing environments.

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