



International Journal of Innovative Research in Science Engineering and Technology (IJIRSET)

(A Monthly, Peer Reviewed, Refereed, Scholarly Indexed, Open Access Journal)



Impact Factor: 8.699

Volume 14, Issue 6, June 2025

Design of Noise Free Chips using Schmitt Trigger Optimization

Mamidi Nithin Kumar¹, Ponugoti Srinithya², Ramagundam Santhosh³, Repaka Askhitha⁴,

Dr K Bindu Madhavi

Dept. of Electronics & Communication Engineering, Hyderabad Institute of Technology and Management (HITAM),
Hyderabad, India

Associate Professor, Dept. of Electronics & Communication Engineering, Hyderabad Institute of Technology and
Management (HITAM), Hyderabad, India

ABSTRACT: This report presents an in-depth examination of three Schmitt Trigger circuit structures: 4-Transistor (4T), 6-Transistor Conventional and a Body Biasing-modified 6-Transistor Schmitt Triggers. To study their behavior and performance, a set of software tools was combined. MATLAB enabled behavioral modeling for the description of early-stage logic functionality. Xilinx Vivado was used for Register Transfer Level (RTL) design and digital simulations, conforming the circuits to FPGA implementation guidelines. LTSpice provided precise transistor-level analog simulations to investigate real-world circuit behavior. The analysis was targeted towards primary parameters like noise immunity, switching performance (propagation delay and hysteresis), power dissipation, and overall applicability for FPGA and ASIC usage. Particular emphasis was placed on the effect of body biasing in the improved 6T structure, analyzing its advantages in power efficiency and signal integrity enhancement. Through the application of a multi-tool simulation technique and comparison between various architectures, the report indicates the trade-offs and benefits of each structure. The results offer useful information to designers who want to optimize Schmitt Triggers for low-power, high-speed digital circuits.

KEYWORDS: Schmitt Trigger, 4T Schmitt Trigger, 6T Conventional Schmitt Trigger, 6T Body Biased Schmitt Trigger, MATLAB Simulation, Vivado Design Suite, Verilog HDL, LTSpice Simulation, Hysteresis Loop, FPGA Implementation, Noise Immunity, Threshold Voltage, Transistor-Level Design, Behavioral Modeling.

I. INTRODUCTION

Schmitt Triggers are critical additives in digital structures, especially for processing noisy or slowly varying input alerts. This mission focuses on the layout, simulation, and performance evaluation of 3 varieties of Schmitt Trigger circuits: 4T, 6T Conventional, and 6T with Body Bias. To offer a comprehensive knowledge, a tri-level simulation technique changed into adopted the use of MATLAB, Vivado, and LTSpice. MATLAB became employed for behavioral modeling and hysteresis evaluation, Vivado was used for virtual design and FPGA simulation, whilst LTSpice enabled accurate transistor-degree circuit verification. Each device contributes uniquely—ranging from conceptual modeling to hardware validation and analog precision. The task targets to examine the designs based totally on parameters which include hysteresis width, switching velocity, energy efficiency, and implementation feasibility on FPGA or ASIC structures. This multi-device method gives a holistic view of Schmitt Trigger performance across abstraction stages.

II. RELATED WORKS

Now in this related work part, we will discuss some work done in this field.

A. Design, and Analysis of CMOS Schmitt Trigger:

The authors of the paper [1]. In "Design and Analysis of CMOS Schmitt Trigger," Kumar KVLP introduced a CMOS-based Schmitt Trigger implemented with a 130nm process and experimentally verified for important performance

parameters such as power consumption, slew rate, and hysteresis. The research compares this design with traditional Schmitt triggers, noting that the CMOS version dissipates less power and operates more quickly. The authors also tested the effect of environmental conditions like temperature and supply voltage fluctuations. Experimental data proved that the CMOS Schmitt Trigger performed reliably under varying conditions, being more stable and reliable than traditional designs. Their results indicate that CMOS Schmitt Triggers are ideal for contemporary digital circuits with noise immunity and effective signal conditioning.

B. Design, Implementation and Analysis of Different Models of CMOS Schmitt Trigger:

The authors in their paper [2].Intended to evaluate the performance and suitability of these models for modern electronic applications.The study examines several CMOS Schmitt trigger types, with particular focus given to voltage transfer characteristics, hysteresis, and noise immunity. Using simulations and theoretical analysis, the paper assesses the significant performance advantages and limitations of each model, providing valuable insight into their performance under different operating conditions. The authors identify, based on the analysis of these parameters, the importance of detailed design considerations in optimizing the performance of Schmitt triggers for the implementation of varying applications, including signal conditioning and noise filtering in digital circuits. This work provides important knowledge to the CMOS Schmitt trigger design community, assisting engineers with deciding on the best configuration based on the application requirements.

C. Design of a High-Speed, Low-Noise and Low-Leakage Schmitt Triggers:

The authors in their paper [3]. Introduced a CMOS-based Schmitt Trigger implemented using a 130nm process and verified for important performance parameters such as power consumption, slew rate, and hysteresis. The research compares this design with traditional Schmitt triggers, pointing out the CMOS version's reduced power dissipation and increased speed. The authors also explored the effects of environmental parameters like temperature and variations in supply voltage. Experimental outcomes confirmed that the CMOS Schmitt Trigger provided dependable performance in varied conditions and compared favorably to traditional designs with regard to stability and reliability. The findings conclude that CMOS Schmitt Triggers are optimally suitable for contemporary digital circuits demanding noise immunity and effective signal conditioning.

D. Analysis and Design of the Classical CMOS Schmitt Trigger in Subthreshold Operation:

The authors at their paper [4].design the traditional CMOS Schmitt trigger to operate in subthreshold, aiming at ultra-low-power applications such as wearables and biomedical devices. They present an analytical analysis of its exponential current-voltage characteristic, with emphasis on hysteresis control by transistor sizing and biasing. Closed-form expressions for switching thresholds are obtained to accurately predict circuit behavior. SPICE simulations confirm their analysis. The authors describe trade-offs among power, hysteresis width, and delay, providing design guidelines for low-power controlled-hysteresis designs. Comparing different topologies, they find the classical Schmitt trigger is the most straightforward and efficient to use subthreshold. Their work provides a helpful reference for subthreshold circuit design.

E. Comparative Analysis of CMOS Schmitt Triggers:

The authors in their paper [5].compare several classical and modified designs using some important performance parameters including hysteresis width, power consumption, and propagation delay. The simulations were done using CADENCE Virtuoso with the Spectre simulator in a 500nm CMOS technology node. The results suggest that each architecture has its strengths and weaknesses - some exhibit superior noise immunity due to wider hysteresis; however, some are designed for a lower power consumption or a faster switching speed without sacrificing robustness. The paper points out that there is no one best architecture; different designs must be selected as they will relate to the project needs. The example given was the GPIO buffers. In a GPIO buffer, robustness to noise may be more important than speed or power. The authors highlight clear trade-offs in regard to various aspects of design and recommend that for each case, the balance will depend on the task in mind. Some applications – such as low-power IoT systems or biomedical devices – may benefit from a more power-conserving design. Overall, the design paper serves as a useful

insight for circuit designers that elucidates some of the most suitable Schmitt triggers for use in contemporary CMOS circuits.

III. METHODOLOGY

Simulation and Performance Analysis of Schmitt Trigger Circuits using MATLAB

This project, which uses MATLAB for behavioral modeling, Vivado for RTL design, and LTspice for analog-level circuit simulation, will simulate and perform analysis for a total of three designs of Schmitt Trigger. The designs will be: 4T, 6T Conventional, & 6T with Body Bias.

MATLAB Simulation for Behavioral Modeling MATLAB was utilized to analyze the voltage transfer characteristics (VTC) and to produce hysteresis curves for the various Schmitt Trigger circuits. The procedural steps are presented below:

- Step-1. Model the input-output behavior using threshold logic for each circuit (4T, 6T, 6T-BB).
- Step-2. Simulate and draw hysteresis loops using input voltage sweeps.
- Step-3. Tune the threshold parameters to see variations in performance.
- Step-4. Use plots to identify switching points and hysteresis widths.

Digital RTL Design of Schmitt Trigger Using Vivado

Vivado Design Suite is employed for the design and simulation of digital circuits. The Schmitt Trigger circuits were coded using Verilog HDL, and the logic code was developed to model switching behavior using feedback and state control. Testbenches were created to simulate ramping input, similar to an analog nature, and simulations outputs were evaluated to identify the presence of hysteresis. The Verilog code was then synthesized and demonstrated on a Spartan-7 FPGA to evaluate performance in hardware. The results showed significant improvements in noise tolerance and signal integrity, validating the effectiveness of the Schmitt Trigger design.

Transistor-Level Simulation Using LTspice

LTspice is a circuit simulation tool used for transistor-level analysis. In this project, we built the 4T, 6T, and 6T Bodied Bias Schmitt Trigger circuits in CMOS technology. We performed Transient Simulation and DC sweep simulation for the DC response of circuits to obtain hysteresis voltages and to observe switching behavior. The 6T Bodied Bias version was able to body bias devices to give us adjustable threshold voltages that provided wider hysteresis. This was especially useful when analysing non-ideal real-world effects when looking at switching behavior and noise immunity.

Cross-Tool Comparison

After simulation study in all three tools, the same ramp input was applied across MATLAB, Vivado, and LTspice to compare the results of the simulations. The outputs were analysed for comparison looking at hysteresis width, switching delay, and general circuit performance. This cross-platform validated the design at different levels of abstraction required for the various tools.

IV. IMPLEMENTATION

Schmitt Trigger circuits are implemented and simulated using three different tools: MATLAB, Xilinx Vivado, and LTSpice. The three designs—4T, 6T, and 6T with Body Bias—are used to examine frequency performance, power efficiency, and hysteresis behaviour.

i. LTSpice Implementation

Analogue Devices created the SPICE-based analogue circuit simulator LTSpice. It is perfect for simulating transistors at the MOSFET level. The first step in the implementation was making a new schematic in LTSpice and adding the required ground, NMOS, PMOS, and voltage sources (Vin and VDD). Two PMOS and two NMOS transistors were

linked in a simple inverter configuration for the 4T Schmitt Trigger, with feedback from the output to the gate of one PMOS and one NMOS transistor. In order to intensify the hysteresis effect, more feedback transistors were added to the 6T design.

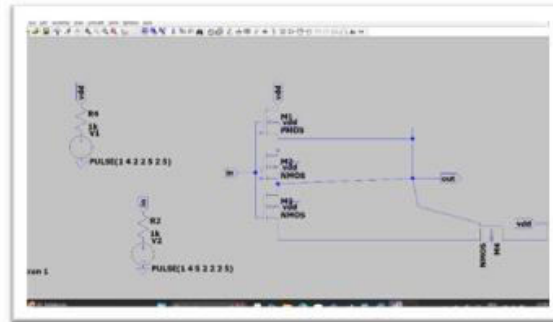


Fig.no.1.1 Design of 4T Schematic Trigger

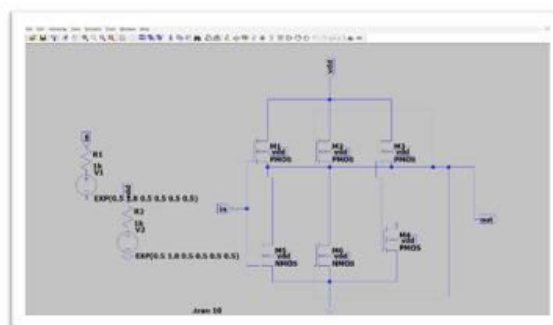


Fig.no.1.2 Design of 6T Body Bias Schematic Trigger

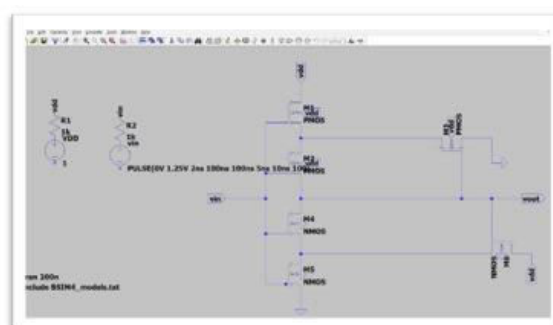


Fig.no.1.3 Design of 6T Schematic Trigger

A bias voltage was applied to the NMOS's substrate terminal in order to dynamically modify the threshold voltage for the 6T Body Bias design. The transient simulation was started with the tran 0.1n 100n command, and the input voltage source was defined as a pulse using the command PULSE(0 1.8 0 1n 1n 10n 20n). Plotting Vin and Vout allowed for the observation of the simulation's outcomes. Only when the input exceeded the threshold levels did switching take place, demonstrating the output's obvious hysteretic behaviour. Because of dynamic threshold control, the body-biased design showed increased stability. Additional analyses, such as frequency response and power measurement, were performed.

ii. MATLAB implementation

The Schmitt Trigger designs were analysed and behaviourally simulated using MATLAB. The user was prompted to enter the supply voltage (VDD), upper threshold (Vth_high), and lower threshold (Vth_low) at the beginning of the implementation. The input voltage signal was created as a square wave at 10 MHz. Conditional statements in a loop were used to implement logic that determined the output voltage for each design (4T, 6T, and 6T Body Bias) based on the thresholds.

```

>> san_3
Enter the supply voltage Vdd (e.g., 1.8): 1.8
Enter upper threshold for 4T (e.g., 1.2): 1.2
Enter lower threshold for 4T (e.g., 0.6): 0.6
Enter upper threshold for 6T (e.g., 1.1): 1.1
Enter lower threshold for 6T (e.g., 0.7): 0.7
Enter upper threshold for 6T BB (e.g., 1.0): 1.0
Enter lower threshold for 6T BB (e.g., 0.8): 0.8
    
```

Fig.no.2.1 Inputs

```

Estimated Power Consumption:
4T Schmitt Trigger: 10.92 uW
6T Conventional: 12.53 uW
6T Body-Bias: 14.32 uW
    
```

Fig no.2.2 Power Consumption

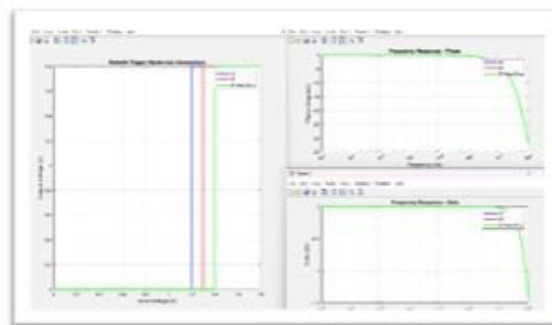


Fig.no.2.3 Output Waveforms

Every time point's output voltage was determined in detail and plotted next to the input voltage. Gain and phase response were calculated for frequency analysis using MATLAB's FFT function. Furthermore, Monte Carlo simulations were performed to assess the circuit's resilience to process fluctuations by varying the threshold voltages at random and tracking the output and power behaviour that resulted. Additionally, power usage and noise margins (NMH and NML) were computed and displayed. Plots demonstrated that all three designs operated as intended, with the 6T Body Bias performing best in variable and noisy environments.

iii. Xilinx Vivado implementation

Digital representations of the Schmitt Trigger circuits were created and simulated using Verilog and Vivado. Verilog source files for the 4T, 6T, and 6T Body Bias designs were added to a newly made RTL project. To simulate threshold-dependent switching, each module employed parameterised if-else logic.

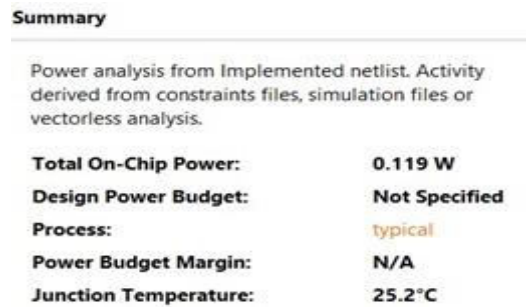


Fig.No.3.1 Power Summary

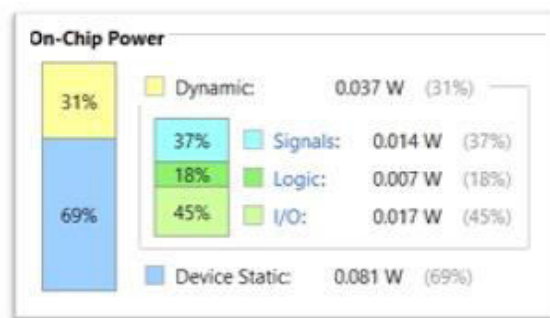


Fig.no.3.2 Power Consumption

A testbench was created to provide toggling input voltages, and thresholds were represented as logical conditions. To keep the simulation in sync, clock and reset signals were incorporated. With the help of Vivado's integrated waveform viewer, behavioural simulation was carried out, enabling the observation of Vout's digital changes in response to Vin. The simulation verified that the hysteresis behaviour was maintained, with the output only toggling when the input surpassed Vth_high or fell below Vth_low. The proper delay and switching behaviour were confirmed by timing diagrams. Vivado's switching activity reports were used to estimate power.

Comparison Table on LTSpice, MATLAB, Xilinx Vivado.

Criteria	LTSpice	MATLAB	Vivado
Simulation Type	Analog / Transistor-Level	Behavioral / Functional	Digital / Logic-Level
Design Focus	MONTE level accuracy	Mathematical modeling & analysis	HDL implementation (Verilog)
Inputs	PULSE, DC, AC, voltage sources	User-defined parameters (VDD, Vth, etc.)	Binary signals from testbench
Power Analysis	From VDD × I(VDD)	From output transitions	Based on switching activity estimation
Noise Analysis	Manual with models	Monte Carlo variation support	Not supported directly
Ease of Use	Moderate (graphical + SPICE syntax)	Easy (scripted, intuitive)	Moderate (HDL + GUI)
Speed of Simulation	Medium (SPICE level)	Fast (numerical models)	Fast (gate-level simulation)
Advantages	High fidelity, real circuit behavior	Flexible, customizable analysis	Real hardware relevance, timing evaluation

REFERENCES

- [1] Kumar KVLP, Prabhakar VSV, Bhavani MD, Geetha K. Venkatesh M, Hari Kishore K. Design and analysis of CMOS Schmitt trigger. Int J Innoy Technol Explore Eng. 2019 May; 8(75):106-9.
- [2] Khanna B. Gupta R. Design, implementation and analysis of different models of CMOS Schmitt trigger. Int Coni Intel Cire Byst ICICS. 2018,63-8. DOI: 10.1109/ICICS.2018.00025.
- [3] Kumawat K, Ajnar D8, Jain PK. Design and analysis of noise immune high-speed and leakage tolerant Schmitt trigger using 180nm CMOS technology, IEEE Madras Sect Conf MASCON 2021;15.DOI:10.1109/MASCONS1689.2021.956358.
- [4] Golca KR. Saini LM. Comparative analysis of CMOS Schmitt triggers. 2023 3rd Int Conf Mob Netw Wirel Commun ICMNWC. 2023,1-5. DOI: 10.1109/ICMNBC60182.2023.10435839.
- [5] Pasini Melek LA, da Silva AL., Schneider MC, Galup-Montoro C. Analysis and design of the classical CMOS Schmitt trigger in subthreshold operation. IEEE Trans Circ Syst 1. 2017;64:869 78. DOI: 10.1109/TCSI.2016.2631726.



INTERNATIONAL
STANDARD
SERIAL
NUMBER
INDIA



INTERNATIONAL JOURNAL OF INNOVATIVE RESEARCH

IN SCIENCE | ENGINEERING | TECHNOLOGY

 9940 572 462  6381 907 438  ijirset@gmail.com



www.ijirset.com

Scan to save the contact details