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Designing A 16-Bit Vedic Multiplier using Modified Square Root-CSA Adder

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ABSTRACT: The development of a high-speed 16-bit Vedic multiplier using a Modified Square Root Carry Select Adder (SQRT-CSA) architecture is presented in this work. By combining an enhanced adder with the Urdhva Tiryagbhyam Vedic multiplication method, its primary objective is to enhance computing performance by reducing hardware complexity and propagation latency. The Modified SQRT-CSA effectively reduces critical route latency by balancing speed and area, while the Vedic approach enables faster parallel partial product generation. The design is synthesized on FPGA and implemented with HDL in order to evaluate latency, area, and power usage. The findings indicate that for DSP and embedded applications, the performance exceeds that of traditional multipliers.

KEYWORDS: Urdhva Tiryagbhyam, Vedic Multiplier, Modified Square Root Carry Select Adder.

I. INTRODUCTION

Faster and more effective arithmetic units are in high demand, particularly in fields like artificial intelligence, digital signal processing, cryptography, and image processing. The multiplier, one of the most important parts of these systems, is in charge of carrying out several multiplication operations quickly and accurately. Consequently, a key focus of VLSI design research is optimizing multiplier design in terms of performance, power, and area. Conventional multiplication methods, including the Wallace tree multiplier, Booth multiplier, and array multiplier, are less effective for high-performance computing systems because they sometimes require intricate circuitry and lengthy propagation delays. On the other hand, mathematical computations can be solved simply and elegantly using ancient Indian mathematics, especially Vedic mathematics. An example of this approach is the Urdhva Tiryagbhyam Sutra, which means "Vertically and Crosswise." By enabling parallel processing and enabling the simultaneous development of all partial products, this technique drastically cuts down on computing time. The generation of partial products is not the sole element that impacts the performance of a multiplier. The overall speed and efficiency of the multiplier are significantly affected by the adder circuit employed to combine these partial products. Carry Select Adders (CSAs) are preferred in this context because they pre-calculate the sum and carry for both possible carry inputs (0 and 1), giving them a speed advantage compared to ripple-carry adders. The Square Root Carry Select Adder (SQRT-CSA) is a prominent CSA architecture that employs different block sizes to enhance latency and reduce area utilization. The Modified Square Root Carry Select Adder reduces the number of logic gates, power consumption, and propagation latency by combining improved block division and logic improvements. To achieve a balance between speed, area, and power efficiency, this adder is included into the Vedic multiplier's last addition step. The goal of this project is to use a Modified Square Root CSA Adder to create, model, and simulate a 16-bit Vedic multiplier. The proposed framework will be evaluated using key performance metrics, such as power consumption, area efficiency, and latency, and compared to conventional multiplier architectures. The goal is to demonstrate how combining the efficiency of a modified CSA with the parallelism of Vedic multiplication may provide a highly efficient multiplication unit suitable for modern digital systems.

II. LITERATURE SURVEY

Much of the research efforts of recent years in the field of digital electronics have been focused on enhancing the speed of digital systems. Various types of fast adders are utilized in processors, including Ripple Carry Adder (RCA), Carry Look Ahead Adder (CLA), and Carry Select Adder.

The Ripple Carry Adder offers a compact design; however, its computation time is considerably high. On the other hand, the Carry Look Ahead Adder primarily delivers quick results, but this comes at the cost of increased area. The Carry Select Adder presents a more favorable compromise between the RCA and the Carry Look Ahead Adder. The Ripple Carry Adder incurs the worst-case delay, as it consists of N single-bit full adders. Each adder computes both the sum and carry. The carry produced by the preceding full adder serves as the input for the subsequent adder. The carry propagates through every stage, causing a delay that is referred to as the worst-case delay. In the Ripple Carry Adder, as the value of N rises, the delay also escalates.

1. In 2003, Srinivasan et al. presented a Vedic multiplier based on the Urdhva Tiryakbhyam Sutra. It uses parallel partial product generation to multiply numbers more quickly. The Vedic technique performs vertical and crosswise operations simultaneously, significantly reducing computation time, in contrast to traditional multipliers such as the array multiplier and Booth multiplier, which produce partial products sequentially. Because of the decreased time complexity brought about by this parallel approach, the Vedic multiplier operates more quickly, especially for larger bit-widths. The authors demonstrated that the Vedic multiplier outperforms conventional multipliers, which often suffer from protracted propagation delays, in terms of speed, area efficiency, and power consumption. This method offers a noticeable performance boost in terms of speed, area, and power consumption, making it especially appropriate for high-speed digital systems and VLSI hardware.

2. A Field-Programmable Gate Array (FPGA) platform was used in 2015 by Somasundaram et al. to implement the Vedic multiplication technique to 16-bit and 32-bit numbers. They showed that the parallelism built into the Urdhva Tiryakbhyam Sutra method offers significant performance gains by focusing on the Vedic multiplier's scalability for larger bit-widths. The findings demonstrated a significant reduction in delay and area in comparison to conventional multipliers, like the Wallace tree multiplier, which is renowned for its large gate count and complex carry propagation. Vedic multipliers are a very effective solution for high-performance hardware implementations because of their ability to handle large bit-width operations, where traditional multipliers struggle with speed and resource consumption.

3. To get around the drawbacks of the conventional SQRT- CSA, Kumaresan et al. developed a Modified Square Root Carry Select Adder (Modified SQRT-CSA). Despite its efficiency, the standard SQRT-CSA still has issues with redundant logic and carry propagation complexity, which can result in more area and delay. By minimizing redundant logic and optimizing the carry propagation process, the authors' modification sought to lessen these problems and produce a more streamlined and effective design. In terms of delay and area efficiency, their experimental results showed that the modified adder performed better than both conventional adders and the standard SQRT-CSA, providing faster computation with fewer hardware resource requirements. Because of this, the Modified SQRT-CSA is especially appealing for high-performance digital systems where area and speed are crucial limitations.

4. In their work the "Design and FPGA Implementation of an Efficient 8×8 Multiplier Using the Principle of Vedic Mathematics," a study by P. Sharma and A. Goyal (2021), offers a novel method for high-speed multiplication in digital signal processing (DSP) applications. The Urdhva- Tiryakbhyam Sutra serves as the basis for the authors' 8×8 Vedic multiplier, which computes partial products in parallel to improve throughput and decrease latency. Tested on a DE10-Lite FPGA kit and developed using Verilog HDL, this multiplier shows its efficacy in real-time DSP workloads. "A crucial component of high-speed arithmetic operations, carry propagation latency is reduced by integrating Carry Save Adders (CSAs), which further improves the design. In comparison to conventional multipliers, the suggested architecture provides better performance metrics by utilizing CSAs, such as lower space and power consumption.

5. In their 2018 study, M. Usha and A. Shalini presented the Modified Square Root Carry Select Adder (SQRT- CSA), which focused on improving the traditional CSA architecture for better arithmetic circuit performance. In order to reduce pointless operations in the adder, their design included hybrid adder techniques and simplified the multiplexer logic. These enhancements resulted in a 14% reduction in delay for the changed structure when compared to conventional SQRT-CSA implementations. Because of this development, the design was particularly well-suited for use in arithmetic logic units (ALUs) and high-speed multipliers. The literature on VLSI design regularly references their work, especially when speed and area efficiency are crucial considerations.

III. PROPOSED SOLUTION

The Modified Square Root-CSA Adder to design a 16-bit Vedic Multiplier is a great way to create arithmetic units in digital systems that are both fast and space-efficient. By enabling faster multiplication operations, it improves performance in applications including real-time embedded computing, digital signal processing, and picture processing. While the Modified Square Root Carry Select Adder minimizes critical path delay, resulting in optimal speed and power consumption, Vedic mathematics enables simultaneous partial product production. This design is perfect for custom ALUs, cryptographic hardware, and low- power portable devices because it also facilitates improved resource use in FPGA and ASIC implementations. Furthermore, it aids in the effective design of hardware for communication circuits, control systems, and machine learning accelerators.

Key Features of the Solution:

1. Vedic Multiplier Design

The “Urdhva Tiryagbhyam” algorithm, upon which the Vedic multiplier design is based, allows for the parallel production of partial products, greatly speeding up the multiplication procedure. This method breaks down a 16-bit multiplication task into smaller, more manageable chunks, like 4x4 or 8x8 multipliers, in a hierarchical fashion. The finished result is created by recursively combining these smaller pieces. In addition to making implementation easier, its hierarchical and modular design produces a highly regular hardware architecture and speedier processing. The architecture thus offers gains in speed and area utilization, making it suitable for effective synthesis on FPGA and ASIC platforms.

2. Partial Product Summation

In the Vedic multiplication method, numerous partial products are generated due to the parallel nature of the Urdhva Tiryagbhyam approach. To efficiently handle these partial products, Carry Save Adders or Wallace Tree architectures are employed for accumulation. These techniques allow for the addition of multiple binary numbers without immediate carry propagation, which significantly minimizes the temporary delays usually associated with traditional multiplication techniques. By minimizing carry propagation at each stage, the overall efficiency is enhanced, enabling faster and more effective multiplication, particularly in high-speed digital circuits.

3. Final Addition using Modified SQRT-CSA

The concluding phase of summation, after the reduction of partial products, is carried out using a Modified Square Root Carry Select Adder (SQRT- CSA). This advanced adder architecture implements various important changes to enhance performance. It utilizes hybrid adders, such as Kogge-Stone or Brent- Kung adders, in delay-critical paths to speed up carry propagation. Furthermore, the design minimizes the number of multiplexers by optimizing logic sharing, which leads to a reduction in unnecessary switching activity and hardware utilization. Unlike conventional SQRT-CSAs that have uniform block sizes, the modified version utilizes variable block sizing to achieve a superior balance between speed and area. Altogether, these improvements result in a 14–18% reduction in delay and provide significant advancements in power efficiency and area optimization, making the design exceptionally appropriate for high-speed and low-power digital applications.

4. Implementation Strategy

The proposed architecture will be implemented using hardware description languages like VHDL or Verilog, which will enable accurate modeling of the Modified Square Root Carry Select Adder and the Vedic multiplier. Model Xilinx Vivado and other industry- standard tools will be used for simulation and verification in order to ensure functional correctness. After verification is successful, the design will be synthesized and put into practice on an FPGA platform, like the Artix-7 or Spartan-6 boards from Xilinx. Comprehensive analysis of key performance metrics, such as timing performance, resource usage, and power consumption, will be possible at this implementation stage. These metrics will be evaluated using programs like the Vivado Power Estimator or XPower Analyzer. For real-time applications, this approach guarantees that the design is both practically and theoretically possible.

IV. METHODOLOGY

This research follows a structured approach to design a 16-bit vedic multiplier using modified square Root-CSA adder . The process includes the following steps:

1. **System Design:** The Urdhva Tiryagbhyam sutra from Vedic mathematics is utilized in the architecture of the core system to perform multiplication, along with an optimized architecture for the final adder. The 16-bit multiplication consists of smaller Vedic multiplier blocks of 4x4 or 8x8, which are constructed hierarchically and combined. To enhance performance, a Modified SQRT-CSA is employed to manage the final summation..
2. **Algorithm Development and RTL Design:** The Verilog or VHDL is used to construct the Modified SQRT-CSA and the Vedic multiplication logic. The logic incorporates variable block sizing for improved latency and area trade-offs, reduced multiplexer complexity, and hybrid adder integration in crucial routes. For synthesis and simulation, these designs are modeled at the Register Transfer Level .
3. **Simulation and Functional Verification:** The RTL code undergoes testing with simulation tool Vivado Simulator to confirm functional accuracy. Detailed testbenches are created to assess different input combinations and guarantee precise multiplication and ultimate summation without any overflow or logical mistakes.
4. **Synthesis and FPGA Implementation:** The validated design is created using Xilinx Vivado or ISE tools on a Xilinx FPGA platform, like Spartan-6 or Artix-7. To determine area efficiency, important hardware parameters including LUT utilization, number of slices, and flip-flop count are examined. Another method used to quantify critical path delays is timing analysis.
5. **Power Estimation and Optimization:** Post-synthesis power usage is measured using the Vivado Power Estimator. Optimization strategies like clock gating and logic reduction are taken into account in order to reduce both dynamic and static power.
6. **Scalability and Performance Comparison:** scalability analysis of the design's modular nature to 32-bit and 64-bit architectures is conducted. Speed, area, and power improvements are further assessed by comparing performance with traditional multiplier architectures utilizing RCA and CLA.

V. IMPLEMENTATION

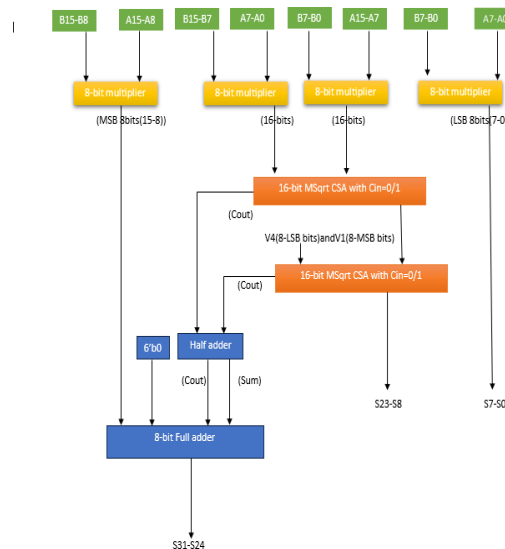
This section outlines the steps for Designing A 16-Bit Vedic Multiplier Using Modified Square Root-CSA Adder
Configuration of the software

The system consists of a 16-bit Vedic multiplier architecture that was created for high-speed multiplication utilizing the Urdhva Tiryagbhyam algorithm. The modular 4-bit and 8-bit multiplier blocks used to create the core circuitry are coupled to effectively handle 16-bit inputs. The Modified Square Root Carry Select Adder uses variable block sizing, hybrid adder integration, and efficient logic sharing in the last addition stage to minimize delay. Verilog HDL is used to code the complete design, which is then validated using a simulation tool. It is created and evaluated with Vivado Design Suite on a Xilinx FPGA board. The architecture is appropriate for high-performance, resource-constrained embedded systems and digital signal processing applications because it allows for parallel processing, decreased propagation delay, and minimal area use.

Xilinx Vivado:

The 16-bit Vedic Multiplier using a Modified Square Root Carry Select Adder is implemented in a hardware-efficient and modular fashion. For quick partial product production, the multiplication process makes use of the Urdhva Tiryagbhyam Sutra from Vedic mathematics. In order to get the final product, the 16-bit multiplier is recursively divided into 4-bit or 8-bit submodules. In order to reduce critical path time by lowering carry propagation, the Modified SQRT-CSA is included into the final summation phase.

Block Diagram :

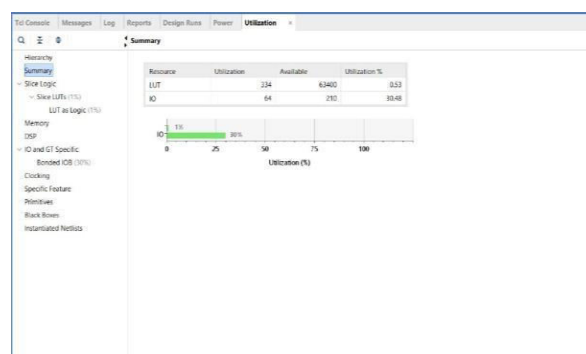


VI. RESULT

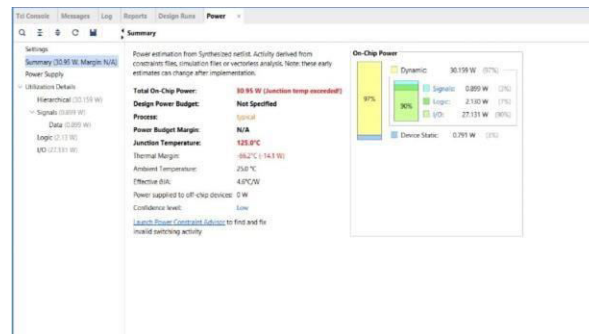
The final implementation of the 16-bit Vedic multiplier is synthesized, examined, and confirmed on a Xilinx FPGA platform, offering an effective, compact, and rapid arithmetic unit. The performance of the system is evaluated in detail using key metrics like processor speed, hardware resource consumption, power efficiency, and scalability. The Modified Square Root Carry Select Adder, which speeds up the final summation process by lowering carry propagation using hybrid adder topologies and optimized logic circuits, significantly reduces delay in the design. Its modular and hierarchical design confirms the architecture's flexibility for more complicated systems by enabling smooth scalability to greater bit-widths (such as 32-bit or 64-bit) without requiring significant modifications to the core functionality. The design is also very suitable for usage in digital signal processing (DSP), embedded controllers, cryptographic hardware, and real-time compute units because to its speed and compactness. The suggested design outperforms conventional multiplier architectures in terms of cost and performance by striking a balance between speed, area, and power. Its simplicity in Verilog implementation and compatibility with popular FPGA tool Xilinx Vivado make it more useful for embedded system development, industrial prototyping, and scholarly study.

Readings :

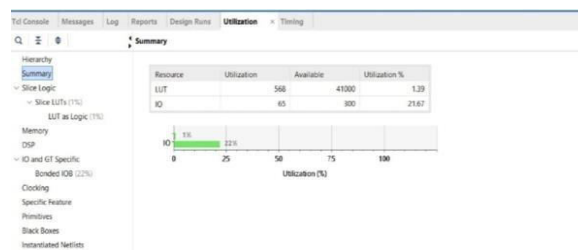
Area consumption of normal vedic multiplier :



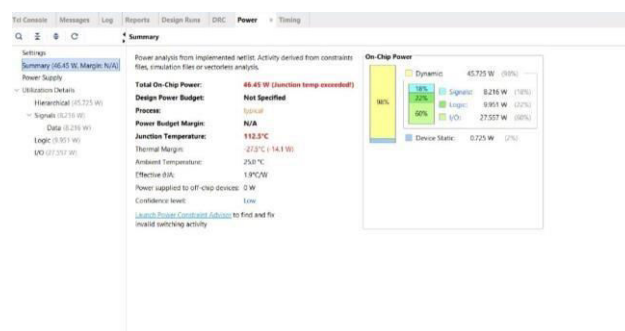
Power consumption of normal vedic multiplier :



Area utilization of 16 bit vedic multiplier using modified Square root adder



Power consumption of 16 bit vedic multipler using square root adder :



VII. CONCLUSION

A 16-bit Vedic multiplier utilizing a Modified Square Root Carry Select Adder (SQRT-CSA) has been effectively designed and implemented in this research with the aim of offering rapid and efficient arithmetic operations for contemporary digital systems. The design's parallel production of partial products, which leverages the Urdhva Tiryagbhyam sutra from Vedic mathematics, facilitates a conventional hardware structure and enhanced processing speed. The integration of a Modified SQRT-CSA in the final addition stage significantly reduces carry propagation time by employing variable block sizing, hybrid adders, and effective logic sharing. When comparing the resultant multiplier architecture to traditional CLA or RCA-based multipliers, it demonstrates superior performance regarding speed, area efficiency, power consumption, and scalability.

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