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# FPGA-Based Implementation of Equalization for 5G Wireless Communication

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**ABSTRACT**: This paper describes the implementation of a Least Squares Estimation (LSE) based equalization algorithm on a Field-Programmable Gate Array (FPGA) for 5G wireless communication systems. Leveraging Xilinx tools, the design optimizes digital signal processing for high-speed data transmission, enhancing system performance and reliability. The project focuses on the implementation of equalization algorithm for compensating channel distortions. The implementation considers key aspects such as resource utilization, power efficiency, and real-time processing capabilities. The project showcases the potential of FPGA-based acceleration for computationally intensive algorithms.

#### I. INTRODUCTION

The advancement of wireless communication has led to the development of 5G networks, which aim to provide higher data rates, ultra-low latency, and improved reliability. However, 5G wireless channels are highly susceptible to impairments such as multipath fading, interference, and noise, which can degrade signal quality and overall system performance. Equalization techniques are crucial in combating these issues, allowing for the recovery of the transmitted signal with minimal distortion. Field-Programmable Gate Arrays (FPGAs) offer an excellent platform for implementing real-time signal processing algorithms due to their parallelism, flexibility, and high computational capability. By using FPGAs, complex equalization methods can be efficiently realized to meet the stringent performance requirements of 5G. This project focuses on the FPGA-based design and implementation of equalization algorithms tailored for 5G wireless communication. Techniques such as Least Square Estimation (LSE) equalization are considered to improve signal quality. The project also emphasizes hardware optimization to achieve low latency and high throughput. Implementing equalization on FPGA enables real-time processing, adaptability to varying channel conditions, and scalability for future enhancements. Overall, this work aims to contribute toward more robust and efficient 5G receiver designs through hardware accelerated equalization.

#### **II. LITERATURE SURVEY**

The first study [1] Parik Harsh and Vasani Ekta, published in the International Journal of Advance Research and Innovative Ideas in Education, explores an Artificial Neural Network (ANN)-based equalization technique to mitigate Inter-Symbol Interference (ISI) in 5G wireless networks. ISI, caused by multipath propagation, leads to symbol overlap and Bit Error Rate (BER) degradation, impacting LTE and 5G systems. Traditional equalization techniques like Linear Equalizers and Decision Feedback Equalizers (DFEs) struggle in dynamic wireless environments. The authors propose an ANN-based equalizer, leveraging machine learning to dynamically adjust to

real-time channel variations. By learning and adapting to signal distortions, ANNs enhance system reliability, scalability, and low-latency communication, making them ideal for next-generation networks.

The second study [2] Yongbo Bai and colleagues, in their IEEE paper, presented an "FPGA implementation of a channel equalizer based on the Least Mean Squares (LMS) algorithm". LMS is a simple yet effective adaptive filtering technique that updates filter coefficients in real-time to minimize the mean square error between the received and expected signals. The use of FPGA hardware enables parallel processing and low latency, which are crucial for high-speed communication systems. Their work demonstrated that LMS-based equalizers are not only efficient in mitigating ISI but also feasible for real-time deployment in 4G and 5G networks.



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The third study [3] Nitin Tandon extended this approach by "implementing a Recursive Least Squares (RLS) equalizer on FPGA". His research focused on optimizing performance in fading channels, which are common in mobile communication scenarios. The RLS algorithm, known for its faster convergence compared to LMS, was modeled using tools like MATLAB, Simulink, and Xilinx System Generator. Simulation results confirmed that the RLS-based equalizer offered better signal clarity and reliability, making it a suitable choice for resource-constrained, real-time communication systems.

The fourth study [4] Further analysis was provided by Praveen Kumar Reddy and his team, who explored the design and performance of efficient adaptive equalizers for wireless communication. Their study evaluated both LMS and RLS algorithms in terms of convergence speed, computational complexity, and Bit Error Rate (BER). The simulation outcomes highlighted the importance of adaptive filtering techniques in combating ISI and multipath fading, particularly in 5G and broadband wireless access scenarios. Their work underscored that selecting the appropriate equalization method depends on the trade-off between performance and computational efficiency.

#### **III. METHODOLOGY**

The project entails applying a Least Squares Estimation (LSE)-based equalization algorithm to an FPGA with the aim of real-time signal recovery in 5G and beyond wireless communication systems. The implementation starts with coding the algorithm in  $C/C^{++}$  through High-Level Synthesis (HLS), which provides a software-like method of specifying hardware logic. Major operations like matrix transposition, multiplication, and inversion are done in fixed-point to ensure optimal performance and resource usage on the FPGA.

A complete testbench environment is established to run a range of input scenarios and check the numerical precision and logical validity of the algorithm. The design is synthesized into Register-Transfer Level (RTL) code using HLS after being validated. A co-simulation step confirms that the generated RTL is functionally consistent with the original C/C++ model, which is important for ensuring functional consistency. The RTL design that is validated is subsequently exported as an IP (Intellectual Property) block and integrated into a complete system via Vivado's IP Integrator. System-level design incorporates fundamental hardware blocks like AXI interconnects, DMA engines, memory controllers, and an ARM Cortex-A53 processor subsystem that are found on the Zynq UltraScale+ RFSoC (ZCU111) platform. To provide support for in-system debugging, a System Integrated Logic Analyzer (ILA) is included to allow real-time visibility of internal signals while in use. Upon successful integration and verification, a bitstream is created and deployed through the Vitis software platform, controlling hardware-software interaction, driver integration, and FPGA programming. The FPGA performs the LSE-based equalization algorithm with low latency and high throughput upon deployment, satisfying the strict requirements of high-speed 5G baseband processing.

This project illustrates the benefits of FPGA acceleration, such as parallel processing, reconfigurability, and efficient handling of complex mathematical operations. With the toolchain provided by Xilinx—HLS for algorithm development, Vivado for hardware design, and Vitis for deployment—the workflow is simplified and efficient. The end implementation exemplifies the ability of FPGAs to function as high-performance, adaptive computing platforms for next-generation wireless communication systems.



#### Fig. 1. Block Diagram



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Fig. 2. Circuit Diagram

The circuit diagram includes a Zynq UltraScale+ Processing System ( $zynq\_ultra\_ps\_e\_0$ ) as the main control unit, handling software operations and communicating with programmable logic through AXI. A Processor System Reset block provides proper initialization and synchronization. Custom AXI Stream IPs, input\_h\_0 and input\_y\_0, supply the matrix H and vector y to the Least Squares Estimator (least\_estimator\_0), the main HLS-generated block that does signal estimation. The output is observed with a System ILA for real-time debugging, and a VIO core facilitates dynamic interaction with internal signals to assist in system observation and control during execution.

#### **IV. SYSTEM COMPONENTS**

#### A. ZYNQ ULTRASCALE + RFSOC ZCU111 BOARD:

The Zynq UltraScale+ RFSoC ZCU111 Evaluation Kit from AMD is a high-performance development platform designed for advanced RF applications. It features the XCZU28DR RFSoC, integrating 8 high-speed 12-bit ADCs (up to 4.096 GSPS), 8 14-bit DACs (up to 6.554 GSPS), and 8 soft-decision FEC cores optimized for standards like 5G and LTE. The board includes a powerful processing system with quad-core ARM Cortex-A53 and dual-core Cortex-R5, along with 8GB of DDR4 memory split between the processing system and programmable logic. It offers a range of high-speed interfaces including USB 3.0, SATA, DisplayPort, PCIe Gen3 x8, Gigabit Ethernet, and an FMC+ connector for I/O expansion, making it ideal for direct RF sampling and real-time signal processing tasks.



Fig.3. ZynqUltraScale+RFSoC ZCU111 Board

#### B. XILINX TOOLCHAIN:

#### VIVADO HLS:

The Xilinx Vivado HLS tool synthesizes a C function into an IP block that you can integrate into a hardware system. It is tightly integrated with the rest of the Xilinx design tools and provides comprehensive language support and features for creating the optimal implementation for your C algorithm.



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Following is the Vivado HLS design flow:

- 1. Compile, execute (simulate), and debug the C algorithm.
- 2. Synthesize the C algorithm into an RTL implementation, optionally using user optimization directives.
- 3. Generate comprehensive reports and analyze the design.
- 4. Verify the RTL implementation using a pushbutton flow.
- 5. Package the RTL implementation into a selection of IP formats.



Fig. 4. Vivado hls.

#### VIVADO HLx:

Vivado HLx Design Suite is a comprehensive development environment from AMD (Xilinx) used for designing, simulating, and implementing digital systems on FPGAs and SoCs. It enables hardware developers to build complex systems using a combination of pre-built and custom Intellectual Property (IP) blocks through a graphical IP Integrator interface. Designers can easily interconnect IP cores, define hierarchical designs, and manage clocking, resets, and data paths within the system. The suite also includes powerful simulation tools to verify the functionality and timing of designs before synthesis. High-Level Synthesis (HLS) support allows for converting C/C++ code into HDL, accelerating algorithm development. Once the design is verified, Vivado synthesizes the logic, maps it to FPGA resources, and generates a bitstream for configuration. The suite also includes tools for timing analysis, power estimation, and hardware debugging via Integrated Logic Analyzers (ILA). Vivado HLx simplifies the development flow and shortens time-to-market for FPGA-based applications across industries.



Fig. 5. Vivado hlx.

#### Vitis:

Vitis is AMD Xilinx's unified software platform that simplifies and accelerates application development on FPGAs, adaptive SoCs, and embedded systems. It allows developers to use high-level languages like C, C++, and Python to build, debug, and deploy hardware-accelerated applications without requiring deep HDL expertise. Vitis supports hardware-software co-design by enabling compute- intensive functions to be offloaded to FPGA fabric, boosting performance and efficiency. Integrated with Vivado for hardware design, it includes Vitis HLS for converting C/C++ to RTL, domain-specific libraries for machine learning, DSP, and data analytics, and Vitis AI for deep learning inference. With platform abstraction and board support packages, Vitis ensures code portability across various Xilinx platforms, including Zynq UltraScale+ MPSoCs, RFSoCs, and Alveo accelerator cards, providing a powerful and scalable development environment.



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Fig. 7. HLS Output.

#### V. RESULTS

Fig. 7 shows the waveform output of an HLS-generated Least Squares Estimator module viewed in Vivado's HLS. It displays the AXI-Stream interface signals (outData), where tdata holds the 32-bit hexadecimal output values produced by the estimator. Signals like tvalid, tready, and tlast indicate proper handshaking and data transfer. Each green hex value represents a fixed-point result from the equalization algorithm. The presence of tlast marks the end of the output data stream.







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Fig. 8 shows a waveform captured from Vivado's HLx, showing the real-time behavior of the output data stream (outData\_0) from an FPGA module. The outData\_0\_tdata signal contains 32-bit fixed-point hexadecimal output values from the design, with valid results such as fff64675, fff424c7, etc. The tvalid signal is asserted high, indicating that the output data is valid, and tlast goes high on the final data word to signal the end of the AXI stream packet. The peripheral reset and clock (pl\_clk\_0) signals show proper operation and synchronization. This confirms successful data transfer and functioning of the output logic from the least squares estimator or related IP block.



#### Fig. 9. Vitis Output.

Fig. 9 shows a waveform captured using Vivado's Integrated Logic Analyzer (ILA). It monitors the AXI Stream interface outData of the least\_estimator block. The TVALID and TREADY signals are both high, confirming valid data transfer. The TDATA signal displays a sequence of 32-bit fixed-point hexadecimal values such as fff6c0, 000170, and 0019f0, representing output data words. TLAST is low, indicating that the end of the stream packet has not yet been reached at this point. The signals are synchronized with the clock, and the stream is marked as "Active" with a "Stream Beat" during this capture window.

#### VI. CONCLUSION

In this work, we designed and implemented an FPGA-based equalization system for 5G wireless communication using the Least Squares (LS) channel estimation algorithm. Leveraging the parallelism and low-latency capabilities of the Zynq UltraScale+ RFSoC, the system effectively compensates for channel impairments such as multipath fading and interference. Developed through hardware-software co-design using Xilinx HLS, Vivado, and Vitis, the solution achieves real-time performance and accurate channel estimation. The project demonstrates the viability and advantages of deploying advanced signal processing on reconfigurable hardware, laying the groundwork for further optimization and real-world 5G applications.

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