



(A Monthly, Peer Reviewed, Refereed, Scholarly Indexed, Open Access Journal)



#### Impact Factor: 8.699

#### Volume 14, Issue 6, June 2025

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[www.ijirset.com |A Monthly, Peer Reviewed & Refereed Journal| e-ISSN: 2319-8753| p-ISSN: 2347-6710|

#### Volume 14, Issue 6, June 2025

#### |DOI: 10.15680/IJIRSET.2025.1406047|

### Design of Double-Edge Triggered Flip-Flop using C-MOS

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**ABSTRACT:** This paper presents a low-power Double-Edge Triggered Flip-Flop (DETFF) design implemented using CMOS-based logic modules. The core building block of the proposed design is a custom c-mos module that mimics a simplified logic comparator using behavioral modeling. This CMOS logic structure is used within the DETFF to suppress unnecessary toggling and control signal flow with greater efficiency. The DETFF captures input data on both rising and falling edges of the clock, using a dual-latch mechanism supported by two interconnected c-mos modules. The design is validated using a testbench that simulates clock generation, reset control, and various test scenarios to evaluate edge-triggered behavior. Functional verification and performance evaluation are conducted through Cadence NClaunch, confirming the DETFF's correct functionality, reduced switching activity, and improved power efficiency under glitch-prone inputs. The simulation results also demonstrate robustness in state retention and low-latency operation during both clock edges, making the design suitable for low-power synchronous systems.

KEYWORDS: low-power, Double-edge, flip-flop, CMOS, dual-latch, low latency, synchronous

#### I. INTRODUCTION

In modern digital systems, power efficiency and timing precision are critical design considerations, especially in portable and high-performance applications. Flip-flops, being fundamental storage elements in sequential circuits, significantly contribute to the total power consumption of a system. Among them, Double-Edge Triggered Flip-Flops (DETFFs) offer an efficient alternative to conventional single-edge flip-flops by sampling data on both the rising and falling edges of the clock. This characteristic enables clock frequency reduction while maintaining throughput, thereby contributing to dynamic power savings.

However, DETFFs are prone to glitches and redundant switching activities, particularly in designs where logic transitions are not effectively controlled. To address this challenge, this work introduces a novel DETFF design utilizing CMOS-based logic to enhance power efficiency and minimize unnecessary transitions. The design incorporates a custom c-mos module that operates as a logic comparator, effectively suppressing glitches by ensuring controlled data flow between latches. The integration of this CMOS structure helps in reducing power consumption without compromising timing accuracy.

In this paper the DETFF is implemented in Verilog HDL and validated using Cadence NClaunch simulation tools. A dedicated testbench applies various clock, reset, and input data conditions to evaluate the flip-flop's behaviour under different operating scenarios. The simulation results confirm that the proposed CMOS-based DETFF design achieves reliable double-edge data capture, reduced latency, and improved energy efficiency, making it suitable for low-power and high-speed VLSI applications.

#### II. METHODOLOGY

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Various methodologies for double edge triggered flip flop have been rigorously analyzed to identify potential improvements and gaps, paving the way for developing CMOS technology. A summary of these approaches is provided below.

#### A. Anti-interference low-power double-edge triggered flip-flop based on C-elements

In this paper, when the input signal has been interfered and glitches occur, the power consumption of Double-Edge Triggered Flip-Flops (DETFFs) will significantly increase. To effectively reduce the power consumption, this paper presents an anti-interference low-power DETFF based on C-elements. The improved C-element is used in this DETFF, which effectively blocks the glitches in the input signal, prevents redundant transitions inside the DETFF, and reduces the charge and discharge frequencies of the transistor. The C-element has also added pull-up and pull-down paths, reducing its latency. Compared with other existing DETFFs, the DETFF proposed in this paper only flips once on the clock edge, which greatly reduces the redundant transitions caused by glitches and effectively reduces power consumption. This paper uses HSPICE to simulate the proposed DETFF and other 10 DETFFs. The findings show that compared with the other 10 types of DETFFs, the proposed DETFF has achieved large performance indexes in the total power consumption, total power consumption with glitches, delays, and power delay product. A detailed analysis of variance indicates that the proposed DETFF features less sensitivity to process, voltage, temperature, and Negative Bias Temperature Instability (NBTI)-induced aging variations.

#### B. Low Power CMOS Based Dual Edge Triggered Flip Flop Using LECTOR C-Element

In the presence of signal interference and glitches, Double-Edge Triggered Flip-Flops (DETFFs) experience a substantial rise in power consumption. To address this issue and achieve power efficiency, this paper focuses on low-power DETFF utilizing LECTOR C-elements. The enhanced C-element integrated into DETFF effectively mitigates input signal glitches, inhibits unwanted transitions within the DETFF, and reduces the transistor's charge and discharge frequencies. LECTOR Circuit integrates two self-controlled leakage control transistors along the route from the power supply to the ground. This placement strategically introduces extra resistance, effectively diminishing the leakage current in the pathway. Further the optimized LECTOR C-Element reduces the delay by 15%. The utilization of these self-controlled transistors represents a promising advancement in mitigating leakage issues, showcasing potential improvements in the efficiency of CMOS circuits. In contrast to other currently available DETFFs, the DETFF introduced in this study undergoes a single flip exclusively at the clock edge and reduces the power consumption by 20%. The simulations were carried out by varying the Vdd voltage for the circuit form 0.6V to 1.2V on Cadence Virtuoso using GPDK-90 library and have the simulation results.

#### C. Low Power DET Flip-Flops Using C-Element

To achieve compact space, high speed and low power in VLSI design is currently the core goal of research personnel. Due to its excellent performance and low power usage, dual edge triggered (DET) approach is the most preferred choice among researchers in the field of VLSI designing. At 50% of clock frequency, DET approaches deliver the same throughput as single edge triggered (SET) systems. The DETFF that is suggested with combination of 2p-1n structure and the C-element circuit. The proposed circuit multiplexes two input latches to one output in a Latch-MUX DET flip-flop by operating in both positive and negative clock cycles. The other structure balances out any errors or glitches that occur in one of the structures. This layout generates output that is fully error-free and can raise system performance. The latches is level-triggered by opposing clock levels to guarantee that every change at the input is always followed by a latch.

#### D. Efficient Design and Analysis of Dual-Edge Triggered Flip-Flop for Advanced VLSI Systems

This paper has a comparative study conducted on various Flip Flop (FF) topologies flop Dual edge triggering (DET) of clock to reduce synchronous IC's dynamic power dissipation. A Static DET FF with inverters connected back-to-back (B2B) and a transmission gate (TG), as well as a real single-phase clock static DET FF, are two different forms of latch multiplexer based DET FFs that are examined. Additionally, a C element based DET FF is examined, offering power efficiency but being more complex and error prone. To address these challenges, a proposed DET FF scheme is introduced, which is transparent when CLK=1 and uses complementary static latches. It employs a Fully Static Complementary CMOS MUX for improved reliability and low voltage operations. The proposed design outperforms an earlier True Single Phase Clocked DET FF (TSPC) with 38 transistors by using 36 transistors.

#### III. SYSTEM DESIGN

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The simulation diagram of the proposed idea is shown in fig.3. Key components of this setup include Cadence Virtuoso software, VMware Workstation Player 17.5. Using the component sand coding in the environment of the cadence where we get the simulation diagram. A brief overview of each component is provided below.

#### 1. Cadence Virtuoso:

Cadence Virtuoso Studio, an application of the Cadence.AI Generative AI Platform, leverages 30 years of industry knowledge and leadership in custom/analog design to give you broader support for systems, including RF, mixed-signal, photonics, and advanced heterogeneous designs. Innovative artificial intelligence (AI) techniques, cloud enablement, infrastructure improvements, and integration across Cadence products complement these design flows, creating a hub for efficiently delivering real designs for the real world.

## cādence°

Fig.1 CADENCE

#### 2. VMware Workstation Player 17.5:

VMware Workstation Player is a virtualization software package for x64 computers running Microsoft Windows or Linux, supplied free of charge by VMware, Inc. It can run existing virtual appliances and create its own virtual machines, which require an operating system to be installed to be functional.



Fig.2 VMware Workstation Player 17.5



Fig.3 Simulation Diagram

#### IV. IMPLEMENTATION AND TEST PROTOTYPE





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The Double-Edge Triggered Flip-Flop (DETFF) was implemented using Verilog HDL, focusing on the use of CMOSbased logic with integrated C-elements to achieve data capture on both rising and falling clock edges. The C-element logic ensures output transitions only when both inputs agree, which was critical in managing the internal latching behavior for stable double-edge operation.

For schematic-level design and validation, Cadence Virtuoso ADE was utilized to construct the circuit schematics and simulate them under real-world constraints. Behavioral verification and logic simulations were carried out using NCLaunch, the simulation interface of Cadence's NC-Sim. NCLaunch enabled waveform tracing, event monitoring, and console output tracking, providing a comprehensive environment for functional verification of the design.

A custom testbench module was developed in Verilog to generate clock pulses, reset signals, and varying data (d) values. The waveform results were analyzed using NCLaunch's waveform viewer and verified against expected truth table values. The flip-flop demonstrated functional response to both clock edges and reset conditions, with transitions in q matching input d under specified timing scenarios.

Through this integrated design and simulation approach, a functional prototype was successfully tested in a simulated lab environment. The use of Virtuoso for design and NCLaunch for simulation allowed for precise analysis of timing behavior and logical correctness, making it a robust method for validating the DETFF architecture. This prototype paves the way for future improvements in layout generation, power optimization, and integration into larger sequential logic systems within ASIC or FPGA architectures.

#### V. CONCLUSION

The prototype of the Double-Edge Triggered Flip-Flop using CMOS and C-Elements was successfully designed and simulated in a virtual testbench environment. Experimental waveform results were analysed using the generated schematic and console outputs, allowing verification of basic functional behaviour. The design was structured to capture data on both rising and falling edges of the clock, aimed at enhancing speed and reducing power consumption in sequential digital circuits.

This project effectively met its objective of creating a low-power, edge-sensitive flip-flop suitable for high-speed VLSI systems. The incorporation of C-elements contributed to noise resilience and glitch suppression, providing improved performance in asynchronous and synchronous environments. The implementation also helped in understanding complex CMOS behaviour, double edge triggering mechanisms, and timing analysis within integrated circuits.

Furthermore, this project can be enhanced by introducing layout design and physical implementation using tools such as Cadence Virtuoso. Additionally, optimizing the transistor sizing and introducing clock gating can further improve power efficiency. The design approach also has the potential to be extended toward pipelined architecture and data path optimization in larger digital systems.

Overall, the project demonstrates a practical and scalable methodology in advanced flip-flop design, aligning well with modern VLSI design goals in terms of speed, power, and reliability.





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Fig. 4 Flow Chart

#### REFERENCES

[1] Huang, Z., Yang, X., Song, T., Qi, H., Ouyang, Y., Ni, T., & Xu, Q. (2021). Anti-interference low-power doubleedge triggered flip-flop based on C-elements. Tsinghua Science and Technology, 27(1), 1-12.

[2] Rawat, A., & Kumar, M. (2024, June). Low Power CMOS Based Dual Edge Triggered Flip Flop Using LECTOR C-Element. In 2024 International Conference on Computer, Electronics, Electrical Engineering & their Applications (IC2E3) (pp. 1-6). IEEE.

[3] Abhishek, A. M., Veena, M. B., & Archana, S. (2023, March). Low Power DET Flip-Flops Using C-Element. In 2023 2nd International Conference for Innovation in Technology (INOCON) (pp. 1-4). IEEE.

[4] Gopika, E. P., Anand, A. B., Shajin, S., Brinda, P., Sreenidhi, H., Rajeev, P., & SD, B. S. (2024, March). Efficient Design and Analysis of Dual-Edge Triggered Flip-Flop for Advanced VLSI Systems. In 2024 10th International Conference on Advanced Computing and Communication Systems (ICACCS) (Vol. 1, pp. 306-310). IEEE.

[5] Unger, S. H. (1981). Double-edge-triggered flip-flops. IEEE transactions on Computers, 100(6), 447-451.

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[6] Afghahi, M., & Yuan, J. (1991). Double-edge-triggered D-flip-flops for high-speed CMOS circuits. IEEE Journal of Solid-State Circuits, 26(8), 1168-1170.

[7] Qiu, S., Yao, M., Chen, R., & Wang, Z. (2024, September). True-Single-Phase-Clock Dual-Edge-Triggering Flip-Flop Based on Low Power Control Technique. In 2024 6th International Conference on Circuits and Systems (ICCS) (pp. 53-57). IEEE.





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[8] Saiteja, K., Vaithiyanathan, D., Verma, P., & Kaur, B. (2023, December). Review of Dual-Edge Triggered Low-Power D Flip-Flops. In 2023 3rd International Conference on Smart Generation Computing, Communication and Networking (SMART GENCON) (pp. 1-6). IEEE.

[9] Qiu, S., Yao, M., & Liu, Z. (2022, November). Low-Power Double-Edge Triggered D Flip-Flop Based on the Conditional Discharge Technique. In 2022 IEEE 22nd International Conference on Communication Technology (ICCT) (pp. 1501-1505). IEEE.

[10] Mathiazhagan, V., Ananthamoorthy, N. P., & Venkatesh, C. (2022). Design and Implementation of Enhanced Edge Triggered Flip-Flop for Low Power Dissipation. Journal of Nanoelectronics and Optoelectronics, 17(9), 1261-1273.









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