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ASIC Implementation of 32-BIT RISC-V RTL

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ABSTRACT: The ASIC implementation of the RISC-V 32-bit processor offers several key features, including a streamlined, high-performance architecture based on the open-source RISC-V instruction set. It supports efficient pipelining and parallel execution, ensuring optimal throughput. The design incorporates low power consumption, customizable data paths, and scalable memory structures. With a focus on high-speed execution and minimal latency, this ASIC implementation is ideal for embedded systems, offering flexibility and cost-effective integration for a wide range of applications.

KEYWORDS: RISC-V Architecture, ASIC Design,32-bit Processor, RTL Synthesis, Physical Design Flow, Timing Optimization.

I. INTRODUCTION

RISC-V (Reduced Instruction Set Computing-V) is an open-standard instruction set architecture (ISA) designed to provide a free and open alternative to proprietary ISAs. Developed in 2010 by the University of California, Berkeley, RISC-V has gained significant attention and adoption in recent years due to its flexibility, scalability, and customizability. RISC-V was born out of the need for an open and extensible ISA that could be used in various applications, from embedded systems to high-performance computing. The initial design was based on the RISC (Reduced Instruction Set Computing) principles developed in the 1980s. The RISC-V project started as a research project at UC Berkeley, led by Krste Asanovic' and David Patterson. RISC-V offers several key features that make it attractive: Open-source: RISC-V is released under the permissive BSD license, allowing anyone to use, modify, and distribute the ISA. Simple and extensible: RISC-V has a simple base ISA, with optional extensions for specific applications. Scalability: RISC-V supports 32-bit, 64-bit, and 128-bit address spaces. Customizability: Users can add custom instructions and extensions. Energy efficiency: RISC-V is designed for low power consumption. Highperformance: RISC-V supports out-of-order execution, pipelining, and superscalar execution. RISC-V's architecture consists of: Base ISA: Defines the fundamental instructions for arithmetic, logical, and control flow operations. Extensions: Optional modules that add functionality, such as: - Multiply and divide (M) - Atomic operations (A) -Floating-point (F) - Vector processing (V) Cryptography (C) Privilege levels: Supports multiple privilege levels for secure execution.

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II. LITERATURE SURVEY

[1] P. Mantovani, et al. Title: A 32-bit RISC-V Processor Designed with High-Level Synthesis Published on: 2017 Observations: We observed that high-level synthesis can significantly improve processor design productivity and quality. They also identified challenges and opportunities in applying HLS to processor design. Applicability: This research is applicable to the development of efficient and scalable processor designs for various applications, including embedded systems and IoT devices. [2] Tanvi Sawant, et al. Title: Design and Implementation of 32-Bit RISC Processor Using Verilog HDL. Published on: 2019 Observations: We observed that the proposed processor design achieved improved performance and area efficiency. Applicability: This research is applicable to the development of digital logic designs and computer architectures for various applications. [3] Chethana H K, Manish S, Harshitha C S, Dr C M Patil, Keerthana B Title: Physical Design of 32-bit RISC-V Processor Published on: 2021 Observations: We observed that the proposed design achieved improved timing closure and area efficiency Applicability: This research is applicable to the development of high- performance and low power processor designs for various applications. including embedded systems and devices. [4] Pritam Sarkar, Dr vasundhara patel K S Title: 32-Bit RISC-V Pipelined Dual Core Processor: Design and Optimization Published on: 2024. Observations: We observed that the proposed processor design achieved improved performance and power efficiency. Applicability: This research is applicable to the development of high- performance and low power processor designs for various applications, including embedded systems and devices. [5] Hyogeun An, Sudong Kang, Dennis A N Gookyi, Garud Kanda, Kwangki Ryoo. Title: Single Cycle 32-bit RISC-V ISA Implementation and Verification Published on: 2022. Observations: We observed that the proposed implementation achieved improved performance and area efficiency. Applicability: This research is applicable to the development of efficient and scalable processor designs for various applications.

III. METHODOLOGY

The ASIC implementation of RISC-V RTL involves three main phases. Phase 1: Synthesis begins with selecting a 45nm standard cell library, which provides pre-designed and verified logic gates optimized for performance, area, and power at that technology node. The RTL design is then synthesized using tools like Cadence Genus, converting the high-level code into a gate-level netlist. The design is subsequently optimized for timing closure and area efficiency through techniques such as logic restructuring and gate resizing. Phase 2: Timing Analysis and Optimization involves performing static timing analysis (STA) with tools like Tempus to identify timing violations (e.g., setup and hold time issues). These violations are then optimized by applying fixes like buffer insertion or gate resizing. This phase iterates between synthesis and timing analysis until all timing constraints are met. Finally, Phase 3: Physical Design starts with floor planning and placement, where the layout plan is defined, major blocks are placed, and standard cells are arranged to minimize routing congestion. The design is then routed using tools like Cadence Innovus to connect all placed cells with metal interconnects, a crucial step for parasitic extraction and accurate timing. The physical design integrity is verified through Design Rule Checking (DRC), Layout Versus Schematic (LVS), and checks for issues like antenna effects and electromigration

Fig 1 Block diagram of 32bit RISC-V Processor

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IV. EXPERIMENTAL RESULTS.

Synthesize a 32-bit RISC-V Processor Core: Synthesize 32-bit RISC-V processor core using RTL (Register-Transfer Level) code.

The QoS (Quality of Synthesis) summary in the screenshot provides an overview of the performance metrics and resource utilization for a RISC-V processor synthesized using Cadence tools. The summary is split into four stages: generic, map, syn_opt, and final, representing the optimization progress throughout the synthesis flow. In the final stage, the slack is 0 ps, meaning the design just meets the timing requirement. Initially, the design had negative slack (e.g., -561 ps in the generic stage), which was resolved progressively through synthesis optimization. TNS (Total Negative Slack), which measures total delay across all violating paths, was reduced from -572 ps to 0, and failing paths dropped from 2 to 0, confirming successful timing closure. The cell area decreased significantly from 663 units in the generic phase to 105 units in the final stage, indicating area optimization. Total instances remained consistent at 29 during the last three stages. CPU and real runtime remained around 30 minutes, and memory usage was about 1535 MB, which is reasonable for this scale of design. This QoS report reflects an efficient and successful synthesis process, with all critical timing and area metrics optimized to meet design specifications.

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Fig 3 Final timing path 1

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The timing report generated from the synthesis of the RISC-V processor provides critical information about the timing performance and path analysis of the design. Each setup check path in the report verifies whether data launched from a flip-flop arrives at its destination flip-flop within the allocated clock period, considering setup time and uncertainties. From the report, we observe paths such as IFU_module_PC_reg[x]/CK -> D, which show successful (MET) setup checks with positive slack values, confirming the design meets timing requirements. For instance, Path 4 has a data path delay of 183 ps and a required time of 188 ps, resulting in a positive slack of 5 ps. Similarly, Path 2 and Path 3 also show MET status with slacks of 5 ps, meaning they just meet the constraints. Path 1, an external delay check, meets the 150 ps requirement exactly, with zero slack.

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Fig 4 Final timing Path 2

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Fig 4 Final timing Path 3

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Fig 5 Final timing Path 4

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Fig 6 Final Area Report

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Fig 7 Varification of DBC

Fig 7 Verification of DRC

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Fig 8 Timing report

Fig 9 Final layout

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V. CONCLUSION

In this project, we successfully designed and synthesized a 32-bit RISC-V processor core using Register Transfer Level (RTL) Verilog. The design was then implemented at the physical level using Cadence tools and the GPDK 45nm technology node. Each stage of the ASIC design flow — from RTL synthesis, floor planning, placement, clock tree synthesis, to routing was completed and verified. The processor design met the timing requirement of 1 ns, corresponding to a 4 GHz operating frequency, ensuring its suitability for high-speed embedded applications. The visual outputs from each stage confirm the correctness and completeness of the ASIC flow, thus fulfilling the first major objective of our project.

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