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# Design of High-Speed, Low-Leakage CAM for Search-Intensive Applications

Prakash M<sup>1</sup>, Jayabratha S<sup>2</sup>, Anbusri G<sup>3</sup>, Monika R<sup>4</sup>, Sanjay C<sup>5</sup>

Assistant Professor, Department of Electronics and Communication Engineering, Builders Engineering College,  
Kangeyam, Tirupur, Tamil Nadu, India<sup>1,2</sup>

U.G. Students, Department of Electronics and Communication Engineering, Builders Engineering College, Kangeyam,  
Tirupur, Tamil Nadu, India<sup>3,4,5</sup>

**ABSTRACT:** Content Addressable Memory (CAM) is an essential element in rapid search applications like network routers, cache memory, and pattern recognition. However, traditional CAM architectures face the challenge of elevated power usage because of their parallel search functions. The suggested model employs a transmission gate (TG) configuration for the design of CAM cells. The transmission gate type of comparison circuit enhances switching speed and minimizes the voltage drop across the output stage. Therefore, this TG model exhibits a shorter delay compared to standard CAM architectures. A paired match lines each analysis technique is introduced to minimize ML transitions per word while also enhancing density in the comparison units. In contrast to the traditional design, where there is one ML discharge for each one-bit mismatch, the new method results in only one ML discharge for two-bit mismatches and so forth. This results in a reduction of ML dynamic-power consumption. Furthermore, we conduct a comparative study of existing low-power CAM architectures versus our proposed design, assessing factors like power efficiency, search delay, and area overhead. The experimental findings reveal a notable decrease in power consumption while preserving competitive performance. This research offers important insights into energy-efficient CAM architecture, improving their applicability for future computing tasks.

**KEYWORDS:** ContentAddressableMemory(CAM),TransmissionGate(TG),Low-PowerCAMDesign,Matchline(ML) Optimization, Search Efficiency, Dynamic Power Reduction, Energy-Aware Architecture, Pattern Recognition, Routing Applications and Cache Systems.

## I. INTRODUCTION

Memory is utilized to retain data. There are different varieties of computer memories. One type among them is referred to as associative memory. This associative memory is also known as content addressable memory (CAM). CAM functions as a hardware search engine that matches content instead of physical addresses. Associative memories operate at a faster pace than traditional RAM since they execute the entire procedure in a single clock cycle. CAM functions in a way that is different from that of random access memory (RAM).

The address is taken as the input to RAM, whereas the data is produced as the output of RAM. In context-aware computing, a user inputs information in the form of text, and the address linked to the content is provided as output. CAM also incorporates external circuitry like sense amplifiers, decoders, etc. It is widely employed in applications such as ultra-fast computers, space satellite ground station systems, cache memory, pattern matching, and more. CAM carries out the function of bit storage using RAM (preferably SRAM) and can also compare bits. Creating a high-speed CAM that can manage longer text is a challenging task.

Designers had to create low-power cells with top performance to meet the standards of the lower technology node. CAM's design can be split into two parts. The first chip consists of an SRAM circuit. The information is used for storage. The second component of the block is a comparator circuit that verifies whether the input provided corresponds to the SRAM cell's stored data. Figure 1 reveals that the SRAM cell has the input terminal called Bit Line (BL) pointing to the bit to be written (stored) within the cell.



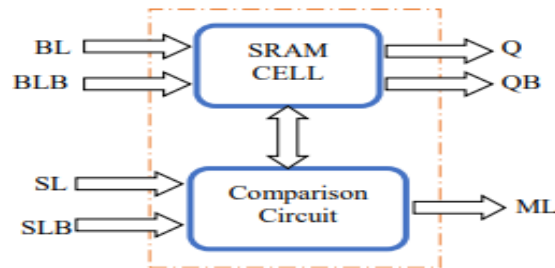


Fig. 1. Basic content addressable memory (CAM)

SRAM bit cell output is Q and Q-bar. Further dividing into the evaluation loop, the input of this search line (SL) bit specifies the data against which BL should be contrasted. The output of the CAM circuit is the match line (ML). If the bit-line and select line differ, the output will be 0; otherwise, the match line (ML) will have a value of 1. Table I. lists several input and output circumstances of CAM. Before we go on forth several notes to mention that, the NMOS transistor is ideal to pass logic "0" and turns ON when its gate voltage is high. PMOS transistor is good for passing logic '1' and turning ON when its gate voltage is low.

TABLE I. CONVENTIONAL CAM OPERATION

BL	BLB	SL	SLB	ML
0	1	0	1	1
0	1	1	0	0
1	0	0	1	0
1	0	1	0	1

**CAM:**Content-addressable memories (CAMs) are hardware search engines that are much faster than algorithmic approaches for search-intensive applications. CAMs are composed of conventional semiconductor memory (usually SRAM) with added comparison circuitry that enables a search operation to complete in a single clock cycle. The two most common search-intensive tasks that use CAMs are packet forwarding and packet classification in Internet routers.

We survey recent developments in the design of large-capacity content-addressable memory (CAM). A CAM is a memory that implements the lookup-table function in a single clock cycle using dedicated comparison circuitry. CAMs are especially popular in network routers for packet forwarding and packet classification, but they are also beneficial in a variety of applications that require high-speed table lookup. The main CAM-design challenge is to reduce power consumption associated with the large amount of parallel active circuitry, without sacrificing speed or memory density. In this paper, we review CAM- design techniques at the circuit level and at the architectural level. At the circuit level, we review low-power match line sensing techniques and search line driving approaches. At the architectural level we review three methods for reducing power consumption.

Content-addressable memory (CAM) is frequently used in applications, such as lookup tables, databases, associative computing, and networking, that require high-speed searches due to its ability to improve application performance by using parallel comparison to reduce search time. Although the use of parallel comparison results in reduced search time, it also significantly increases power consumption.

Content-addressable memory (CAM) is a special type of computer memory used in certain very high speed searching applications. It is also known as associative memory, associative storage, or associative array, although the last term is more often used for a programming data structure.

#### Hardware Associative Array:

Unlike standard computer memory (random access memory or RAM) in which the user supplies a memory address and the RAM returns the data word stored at that address, a CAM is designed such that the user supplies a data word and the

CAM searches its entire memory to see if that data word is stored anywhere in it. If the data word is found, the CAM returns a list of one or more storage addresses where the word was found (and in some architectures, it also returns the data word, or other associated pieces of data). Thus, a CAM is the hardware embodiment of what in software terms would be called an associative array.

#### Standards for Content-Addressable Memories:

A major interface definition for CAMs and other Network Search Elements (NSEs) was specified in an Interoperability Agreement called the Look-Aside Interface (LA-1 and LA-1B) developed by the Network Processing Forum, which later merged with the Optical Internetworking Forum (OIF). Numerous devices have been produced by Integrated Device Technology, Cypress Semiconductor, IBM, and others to the LA interface agreement. On December 11, 2007, the OIF published the serial look aside (SLA) interface agreement.

#### Semiconductor implementations:

Because a CAM is designed to search its entire memory in a single operation, it is much faster than RAM in virtually all search applications. There are cost disadvantages to CAM however. Unlike a RAM chip, which has simple storage cells, each individual memory bit in a fully parallel CAM must have its own associated comparison circuit to detect a match between the stored bit and the input bit. Additionally, match outputs from each cell in the data word must be combined to yield a complete data word match signal. The additional circuitry increases the physical size of the CAM chip which increases manufacturing cost. The extra circuitry also increases power dissipation since every comparison circuit is active on every clock cycle. Consequently, CAM is only used in specialized applications where searching speed cannot be accomplished using a less costly method.

#### Alternative Implementations:

To achieve a different balance between speed, memory size and cost, some implementations emulate the function of CAM by using standard tree search or hashing designs in hardware, using hardware tricks like replication or pipelining to speed up effective performance. These designs are often used in routers.

#### Ternary CAMs:

Binary CAM is the most basic type of CAM; it employs data search words made entirely of 0s and 1s. This adds search flexibility by giving one or more bits in the stored data word a third matching condition of "X" or "Don't Care." A ternary CAM could, for instance, have a stored word of "10XX0," which will match any of the four search words &'10000,' '10010,' '10100,' or &'10110'. Because the internal memory cell must now encode three potential states rather than the two of binary CAM, the increased search flexibility comes at an extra cost over binary CAM. Normally, including a mask bit (a "care" or "don't care" bit) on each memory cell will activate this further state. Using complex valued representations, holographic associative memory offers a mathematical model for "Don't Care" fused associative recall.

#### Example Applications:

In computer networking equipment, content-addressable memory is quite frequently employed. When a network switch gets a Data Frame from one of its ports, for instance, it updates an internal table with the source MAC address of the frame and the port it was received on. Then the table is checked for the destination MAC address to find out which port the frame needs to be moved to; it is forwarded on that port. Normally, the MAC address table uses a binary CAM, so the destination port can be rapidly located and the switch's latency reduced.

Network routers are typical applications of ternary CAMs, where each address has two components: the network address that can change in size depending on the subnet setup, and the host address that takes up the rest bits. A network mask for each subnet tells which bits of the address are the network address and which bits are the host address. Consulting the router's routing table—each known destination network address, its linked network mask and the data needed to route packets to that destination—routing occurs. The router without CAM would match the destination address of the packet to be routed against every entry in the routing table, do a logical AND with the network mask, and compare it with the network address. If they are equal, the appropriate routing data is employed to send the package.

The lookup procedure becomes quite fast if you use a ternary CAM for the routing table. Since the addresses are kept using "don't care" for the host part of the address, a search of the destination address in the CAM immediately finds the appropriate routing entry; the CAM hardware performs both the masking and comparison.

**Other CAM Applications Include:**

- CPU storage controllers and Translation Look aside Buffers
- Database engines
- Data compression hardware
- Artificial neural networks
- Intrusion Prevention System

## II. EXISTING MODELS

### 1) Low Match-Line Voltage Swing Technique For Content Addressable Memory:

Designing a content addressable memory (CAM) with enhanced search efficiency calls for a unique pre-charge approach. By reducing the loading capacitance and ML voltage swing, this method lowers the match line (ML) power dissipation. The integration of this approach with predictive 45-nm CMOS technology has been accomplished in a 256×64-bit NOR-based CAM; post layout simulations are done in SPECTRE on a 1 V supply. This approach lowers the energy dissipation by 38% vis-à-vis the old pre-charging, which improves search speed by 4.7%.

### 2) QUASIFGMOS6T SRAM Cell Design:

#### A Strategy For Low Power Applications:

Low power and high performance based static random access memory (SRAM) has gained paramount interest as they became an indivisible part of microprocessors, portable devices, system-on-chips and modern VLSI systems. As technology scaled down, low voltage and low power operation are becoming the foremost important issue for mixed signal systems. This paper implements various low power strategies for 6T SRAM cell with supply voltage  $V_{DD}=220\text{mV}$  using TSMC 0.18 $\mu\text{m}$  technology in mentor graphics tool while operating in sub-threshold region which is very crucial for lowering power dissipation and achieves higher speed compared to CMOS circuits.

### 3) Single Bit-Line 11T SRAM Cell For Low Power And Improved Stability

This research focuses on a novel 11T static random access memory (SRAM) cell that incorporates power gating transistors and a transmission gate to achieve low leakage and dependable writing functionality. The proposed cell features distinct paths for reading and writing, which significantly enhances both read and write performance.

Additionally, it addresses the issue of row half select disturbance and employs a row-based virtual ground signal to prevent unnecessary bit-line discharge in the unselected row, thus reducing energy usage. The cell also benefits from low power consumption attributed to the stack effect. To demonstrate the effectiveness of the cell, its design parameters are compared with other SRAM cells that have been published, specifically, conventional 6T, 10T, 9T, and power-gated 9T (PG9T).

In standby mode, this cell shows a reduction in leakage power from 6.71 to 7.37% at an operating voltage of 1.2 V, with improvements in write and read power ranging from 29.21 to 58.68% and 32.74 to 71.11% compared to other cells. The proposed cell achieves higher write and read static noise margins with enhancements of 13.54 and 63.28%, respectively, when compared to the conventional 6T SRAM cell. The cell also offers an improvement in write delay of 29.77 to 49.40% and a read delay improvement of 7 to 12% when compared to 9T, 10T, and PG9T, respectively.

#### Existing CAM Designs:

There are primarily two categories of structures: the matching and searching approach. Also referred to as: NAND-CAM and NOR-CAM [9,10]. The main source of power usage in CAM cells is the match line along with the search line pair (SL, SLB).

#### A. NAND-CAM Design:

In NAND-CAM design, a standard 6 transistor SRAM cell is linked to the input bit lines via the two access transistors. Two cross-coupled inverters are connected to the storage nodes Q and QB. Transistors N5, N6, and N7 are utilized for comparing the data that needs to be searched. The output is obtained from the source terminal of N7 through ML, as illustrated in Fig. 2. A pre-charge circuit is attached, which is in turn linked to an inverter to generate the output ML.

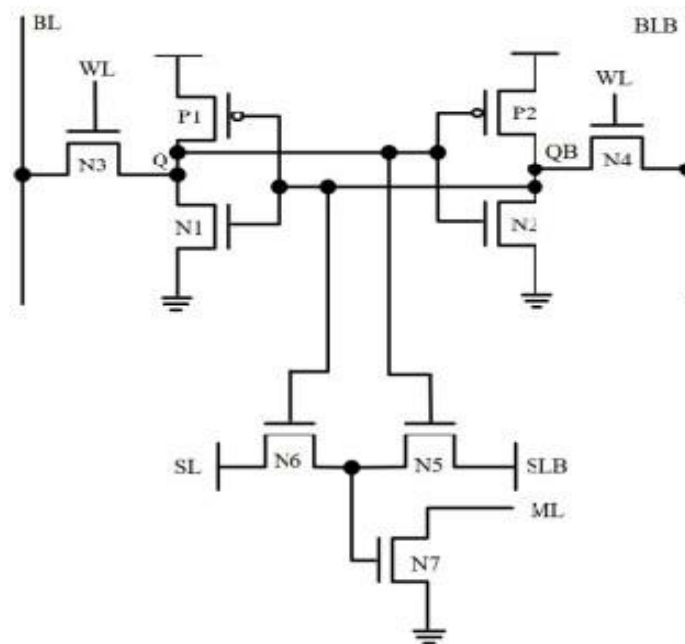


Fig.2. Basic NAND-CAM structure

TABLE II. NAND-CAM OPERATION

BL	BLB	SL	SLB	ML	REMARKS
0	1	0	1	1	N6-ON, N7-OFF. Therefore, ML does not discharge
0	1	1	0	0	N6, N7-ON. ML discharges to ground
1	0	0	1	0	N5, N7-ON. ML discharges to ground
1	0	1	0	1	N5-ON, N7-OFF. Therefore, ML does not discharge

The ML lines start in the pre-charge phase and subsequently discharge to the ground when all CAM cells are matched. A significant disadvantage of NAND CAM is that it causes a voltage drop across the following stage due to the pass transistors N5 and N6 used in the comparison circuit. This results in a heightened delay factor, which in turn decreases the speed of the comparison circuit. Nevertheless, employing pass transistors uses minimal power. To enhance and assess the speed parameter further, we transition to NOR CAM design.

### B. NOR-CAM Design:

NOR-CAM design additionally includes a standard 6T SRAM cell featuring NOR functionality as a reference circuit. As depicted in Fig. 3, transistors N5 and N6 link to the storage nodes QB and Q respectively. The match line (ML) is replenished prior to the searching process. When one or more cells in a CAM do not match, the match-line discharges, signifying that the comparison logic has been established in NOR. The result is returned only after every CAM cell within a single CAM word is matched, meaning the search is completed. The CAM input text can remain unchanged from its original state. In case of a mismatch, the ML is promptly discharged to 0 due to the brief pull-down route. This situation also leads to significant power consumption. Table III. outlines the NOR CAM operation by employing various input scenarios.

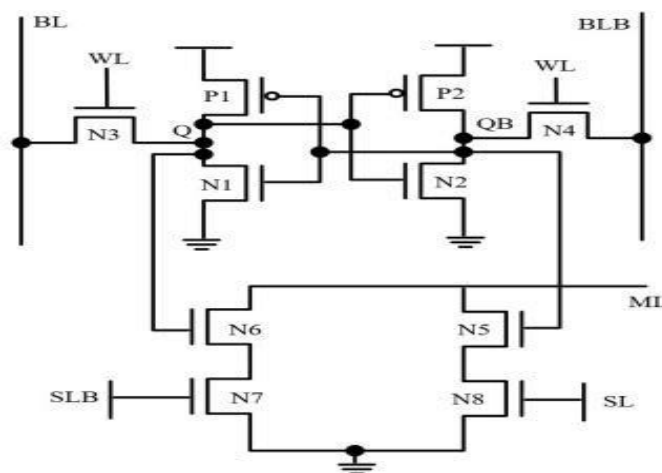


Fig.3. Basic NOR-CAM structure

TABLE III. NOR-CAM OPERATION

BL	BLB	SL	SLB	ML	REMARKS
0	1	0	1	1	N5, N7-ON. No closed path. Therefore, ML does not discharge
0	1	1	0	0	N5, N8-ON. A path exists for discharge. ML discharges to ground
1	0	0	1	0	N6, N7-ON. A path exists for discharge. ML discharges to ground
1	0	1	0	1	N6, N8-ON. No closed path. Therefore, ML does not discharge

### C. Transmission Gate CAM Design:

The transmission gate variant of the comparison circuit enhances the switching speed and minimizes the voltage drop across the output stage. Thus, this TG model experiences a shorter delay compared to traditional CAM architectures. A significant issue with the pass transistor is the threshold voltage drop across the output when the gate terminal is at logic 1. This becomes problematic if the input remains continuously at logic 1. This concern is categorically unacceptable and necessitates an additional circuit at the output to boost voltage. The TG-CAM comprises 10 transistors and is capable of passing both 0 and 1. Another key benefit is the absence of supplementary pre-charge circuitry. This contributes to a decrease in layout area. The TG-CAM design is illustrated in Fig. 4, with the design's functionality summarized in Table IV.



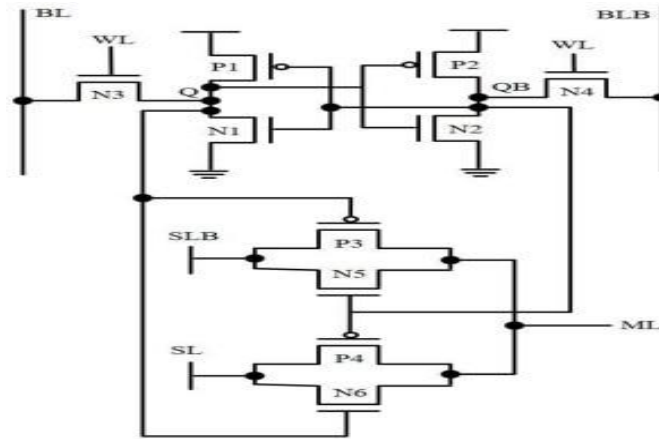


Fig.4. Transmission Gate (TG-CAM) structure

TABLE IV. TG-CAM FUNCTIONALITY

BL	BLB	SL	SLB	ML	REMARKS
0	1	0	1	1	TG1 (P3, N5) ON. SLB (1) passed to output ML
0	1	1	0	0	TG1 (P3, N5) ON. SLB (0) passed to output ML
1	0	0	1	0	TG2 (P4, N6) ON. SL (0) passed to output ML
1	0	1	0	1	TG2 (P4, N6) ON. SL (1) passed to output ML

### III. PROPOSED METHODOLOGY

#### Proposed OML-CAM:

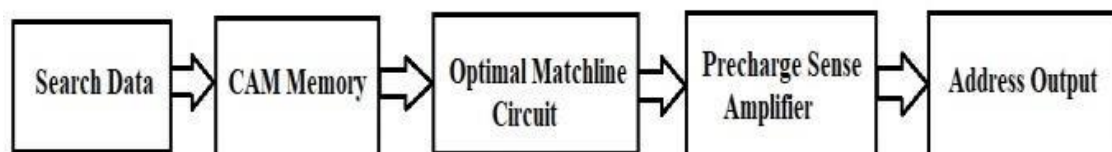


Fig.5. Block diagram of proposed OML-CAM:

The block diagram of the suggested OML CAM is depicted in fig. 5. Considering the high-speed characteristic of TG-CAM, the suggested CAM macro aims to provide the following contributions:

1. A two-bit storage with a comparison-based CAM cell that incorporates OML evaluation is proposed. Because two adjacent cells possess a collective evaluation block, each pair of cells shares a single ML node.
2. Unlike the traditional design, which has one ML discharge for each one-bit mismatch, two ML discharges for two-bit mismatches, and so forth, the proposed OML approach has only one ML discharge for two-bit mismatches. This results in reduced ML dynamic-power consumption.
3. To create an N-bit CAM word,  $N/2$  proposed cells are constructed in TG-type match line so that the match speed (ML delay) aligns with the traditional high-speed match line.



4. The performance (power and delay) of the proposed OML-CAM is evaluated against referenced designs and detailed analyses are included to assess the viability of searching operations across varying process–voltage–temperatures.

Improvements in circuit-level techniques made in the comparison and evaluation section of CAM cells enhanced search speed. During the search, most of the entries in a CAM array result **Proposed Optimized Match-Line Structure** in mismatches. In traditional and existing ML methods, each 1-bit cell is equipped with a specific compare-evaluate circuit. All the mismatched cells generate individual ML state-change (from pre-charged to discharged) pathways in a CAM word or row. The worst-case scenario for discharge occurs when all bits miss in an ML row, at which point the row discharges through ‘N’ equivalent paths for an N-bit data (word). The suggested OML-CAM aims to minimize the number of discharge pathways. A 2-bit (2B) TG-CAM cell is employed, where the storage on the right side and the storage on the left side are compared within a common ML block. Every search scenario is initiated by a default phase (pre-charge) via the pre-charge transistor (PPre) of the sense amplifier shown in Fig. 6.

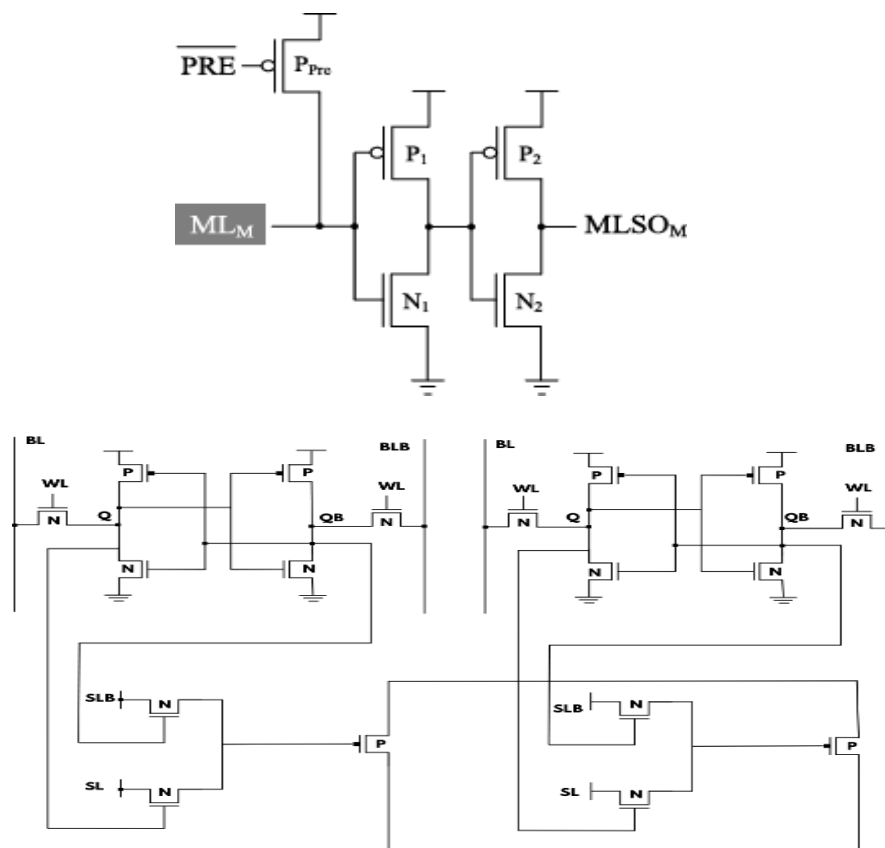


Fig.6. Inverter-based sense amplifier with pre-charge controlled by Signal PRE.

### 1. Pre-Charge Phase:

Pre-charge signal (PRE) is implemented using ‘0’ logic, while SLi and SLi are likewise reset to ‘0’; ML is pre-charged to the supply voltage (VDD).

### 2. Evaluation Phase:

PRE is modified to ‘1’ logic so that the pre-charge transistor (Ppre) is OFF while the input search data is applied to the complementary search-lines (SLi, SLi). When SL corresponds with the bit line (BL), the match line ML stays high; otherwise, during a mismatch condition, ML is discharged to zero.

### 3. Operation of Proposed OML-CAM:

Content Addressable Memory (CAM) is a distinct type of memory intended for rapid data searches and simultaneous comparisons. In contrast to traditional RAM, which accesses data based on a specified address, CAM scans for a specific input pattern throughout all stored entries at once and provides the address of the corresponding match. This capability renders CAM crucial for uses such as high-speed network routing, pattern identification, and cache memory.

A vital component of CAM design is its match line (ML) architecture, which influences power efficiency and operational speed. This paper examines the functioning of CAM with an ideal shared match line for two CAM cells, paired with a pre-charge sense amplifier to improve performance.

**Content Addressable Memory (CAM) Architecture:** CAM is made up of a matrix of CAM cells, with each cell able to store and compare data bits. A CAM cell generally consists of: Storage Element: Often a pair of cross-coupled inverters (SRAM-based) or non-volatile memory elements.

- **Comparison Circuitry:** Consisting of XOR logic to compare archived data with incoming data.
- **Match line (ML):** A signal line utilized to identify a match or mismatch.
- **Pre-charge Sense Amplifier:** Guarantees rapid and energy-efficient detection of match situations.

#### Shared Matchline Structure:

A common match line architecture enhances power and area efficiency by minimizing unnecessary components in the CAM array. In a two-CAM-cell shared ML configuration:

- The match line is common to two neighboring CAM cells, which lowers ML capacitance and power consumption.
- Each CAM cell adds to the ML state depending on the outcome of its comparison task.
- An active pre-charge and evaluation phase guarantees correct operation

#### 1. Precharge Phase:

- Prior to the start of comparison, the ML is charged to a high voltage ( $V_{dd}$ ).
- A pre-charge sense amplifier (PSA) guarantees that the ML is completely charged, minimizing variations and the effects of leakage current.

#### 2. Evaluation Phase:

- The CAM array receives the input data, and each CAM cell executes an XOR operation to compare the stored data with the input data.
- When both cells correspond to the input, the ML stays at a high level; if not, it discharges.
- The PSA identifies the ultimate ML condition and quickly enhances minor voltage discrepancies to signal a match or mismatch status.

#### Pre-charge Sense Amplifier (PSA) in CAM Operation:

A pre-charge sense amplifier is essential for minimizing ML power consumption and enhancing speed. Its roles encompass:

- **Swift Pre-charging:** Rapidly charges the ML to  $V_{dd}$  prior to the comparison cycle.
- **Low-Power Sensing:** Identifies small voltage changes and amplifies them for dependable match detection.
- **Decreased ML Capacitance:** By merging with a shared ML, the PSA boosts power efficiency.

#### Advantages of Shared ML and PSA:

- **Power Decrease:** Sharing ML diminishes switching activity, resulting in decreased dynamic power usage.
- **Space Efficiency:** A reduced number of match line wires results in a more condensed CAM design.
- **Enhanced Speed:** Quicker match line discharge and sensing enhance the speed of search operations.
- **Enhanced Noise Immunity:** PSA enhances minor voltage variations, rendering detection resilient to process fluctuations.

The ideal shared match line design with a pre-charge sense amplifier offers a very effective CAM structure by lowering power usage, increasing speed, and decreasing area overhead. This method is especially advantageous in high-speed scenarios where energy efficiency and performance are essential, like networking devices and AI accelerators. Future developments may concentrate on further minimizing power leakage and improving process scalability for upcoming CAM applications.

#### IV. COMPARISON OF THE PROPOSED OPTIMAL MATCH LINE - BASED CAM WITH THE PREVIOUS EXISTING CAM STRUCTURE

Parameters	Existing	Proposed
Technology	130nm	130nm
WordLine (V)	1.2 V	1.2 V
ArraySize	4X4	4X4
Transistor Count	176	144
Power	27.21mw	13.16mw
Delay	30.32 ns	19.62 ns

#### V. CONCLUSION

In the suggested work, a content addressable memory (CAM) system is constructed utilizing transmission gates (TG) together with optimal match line sensing. The proposed design incorporates a transmission gate (TG) configuration for the CAM cell architecture. The transmission gate comparison circuit enhances the switching speed while minimizing the voltage drop across the output stage. A dual Match-line search analysis approach is introduced to lessen ML transitions per word and enhance density within the comparison units. In contrast to traditional designs, the proposed approach employs only a single ML discharge for every two-bit mismatch. This results in a reduction of ML dynamic power consumption. The proposed CAM structure is designed as a 4X4 array, and metrics such as power dissipation and delay at 130nm have been examined. The findings indicate that the proposed design outperforms existing methodologies concerning power and power delay product. In the future, all high-performance computing applications, including DSP, multimedia, implantable systems, and reconfigurable computing, can be developed using Match-line optimized transmission gate (TG)-CAM to achieve improved delay withstand capabilities even amid temperature fluctuations.

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[www.ijirset.com](http://www.ijirset.com)

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