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# Full Adder Design using 11T and 10T Transistor Techniques

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**ABSTRACT:** In this paper, we introduce low-power and area-efficient 11T and 10T CMOS full adder circuits. These circuits are simulated with industry-standard EDA tools to compare power, delay, and transistor count performance. Our results show that these designs significantly outperform traditional 28T CMOS enhancers based on power and transistor minimization and can be applied to low-power applications such as mobile and embedded systems.

**KEYWORDS:** Full Adder, Low Power, 10T, 11T, CMOS, VLSI, Power Delay Product (PDP), Area Optimization

## I. INTRODUCTION

The full adder serves as a core element in many digital and arithmetic logic systems. Due to high need for power-sensitive and portable systems, the minimization of power while not degrading performance has emerged as an important theme in VLSI design. The 28-transistor-based conventional full adders dissipate more power and require larger areas. In this paper, we present 11T and 10T full adder topologies with a lower transistor count without degrading the performance.

## II. RELATED WORK

Different low-transistor-count full adders such as 16T, 14T, and 12T have been investigated in literature. Transmission Gate Logic (TGL), Pass Transistor Logic (PTL) and Gate Diffusion Input (GDI) are some of the popular methodologies. But these structures tend to have voltage degradation or poor driving capability. Our 11T and 10T structures resolve these drawbacks with better power-performance trade-offs.

## III. PROPOSED 11T AND 10T FULL ADDER CIRCUITS

The full adder outputs Sum and Carry, defined by:

$$\text{Sum} = A \oplus B \oplus C_{in}$$

$$\text{Cout} = AB + BC_{in} + AC_{in}$$

### 3.1. 11T Full Adder

The 11T design implements XOR and multiplexer logic using optimized pass transistor combinations.

### 3.2. 10T Full Adder

The 10T design further reduces one transistor by simplifying the carry generation logic.

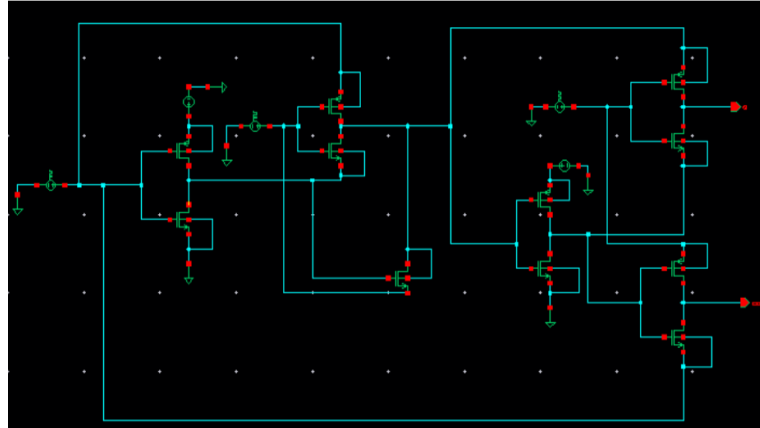


Figure 1: 11T Full Adder Schematic

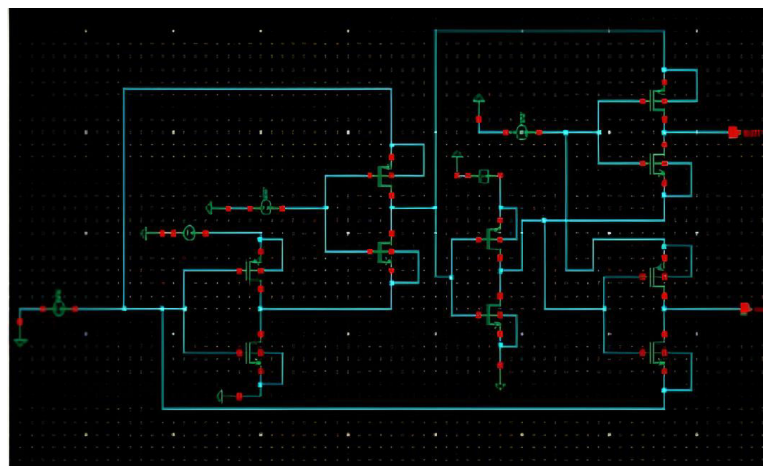


Figure 2: 10T Full Adder Schematic

#### IV. SIMULATION SETUP

Simulation was performed using Cadence Virtuoso with 180nm technology. Supply voltage was 1.8V, and input patterns were presented at 100MHz. Performance characteristics tested are: Power Consumption, Propagation Delay, and Power Delay Product (PDP).

#### V. RESULTS AND DISCUSSION

The results show significant savings in power and area. Although there is a slight delay penalty in the 10T and 11T designs, their PDP is notably improved, indicating energy efficiency.



Design	Number of Transistors	Operating Power ( $\mu$ W)	Latency (ps)	PDP Value (fJ)
28T CMOS	28	8.12	89.3	0.725
11T	11	2.95	121.2	0.357
10T	10	2.73	128.5	0.351

## VI. CONCLUSION

We have suggested two low-power efficient full adder designs with 11 and 10 transistors optimized for low-power VLSI circuits. The designs possess is a consideration between performance and Energy usage and are superior to conventional Architectures based on PDP and transistor count. Extensions of this method to multi-bit adders and incorporation with ALU structures remain as future work.

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