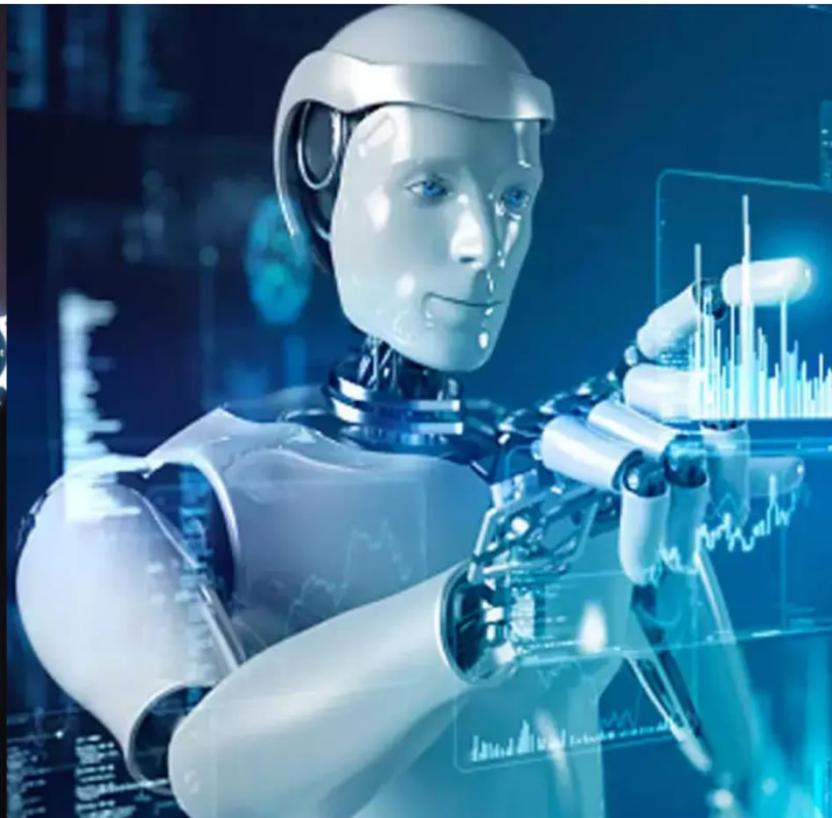




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# **Analysis of Reduced Switch Multi Level Inverter Topologies, Including a Novel Configuration for Enhanced Power Quality & Efficiency**

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**ABSTRACT:** This paper presents a novel multilevel topology for three-phase applications, having three-level modular configurations, enabling low-, medium-, and high- voltage operations. The proposed topology has several attractive features, namely reduced component count, being capacitor-, inductor-, lowering cost, control- complexity, and size, and can operate in a wide range of voltages and powers. Selected simulation and experimental results are presented to verify the performance of the proposed topology. Further, the overall efficiency of the topology and loss distribution in switches are studied. Finally, the key features of the proposed topology in terms of component count, blocking voltage, and DC-link requirements are highlighted via a comparative study.

**KEYWORDS:** DC-AC power converters, low-frequency modulation, multilevel inverters, pulse width modulation.

## **I. INTRODUCTION**

Multilevel inverters (MLIs) have gained significant attention in recent decades as a fundamental component in modern power conversion systems. Their widespread adoption is primarily attributed to their distinctive advantages, including a modular design, high switching redundancy, scalability, low harmonic distortion, and reduced electromagnetic interference (EMI). These characteristics make MLIs highly suitable for various industrial, renewable energy, and transportation applications. The benefits of MLI-based systems include lower total harmonic distortion (THD), minimal filter requirements, enhanced power quality, and the ability to handle high-voltage applications efficiently. Additionally, MLIs enable the use of low-voltage power switches to achieve high-voltage output, improving overall system safety and operational flexibility. Despite their numerous advantages, MLIs also present several challenges that have driven extensive research and innovation. One major drawback is their inherently complex control strategies, which require advanced modulation techniques and computational resources. Furthermore, the high number of semiconductor components in MLI topologies increases system cost, footprint, and thermal management requirements, potentially reducing efficiency and long-term reliability. These challenges have prompted researchers to explore new methods for simplifying control schemes, minimizing the number of components, and improving overall performance. Three conventional MLI topologies—cascaded H-bridge (CHB), neutral point clamped (NPC), and flying capacitor (FC)—have formed the foundation of MLI technology. Each of these topologies has distinct operating principles and advantages. The CHB topology is widely used due to its modularity and ease of expansion, making it well-suited for renewable energy and high- power applications. The NPC topology offers superior voltage balancing and reduced device stress, enhancing system reliability. Meanwhile, the FC topology provides additional voltage levels and better waveform quality but requires complex capacitor voltage balancing techniques. Recent advancements in MLI research have introduced novel configurations and hybrid topologies that aim to overcome traditional limitations. Researchers have focused on reducing component count, simplifying control methodologies, and enhancing efficiency. Some of the latest innovations include asymmetric MLIs, reduced-switch topologies, and artificial intelligence (AI)-based control strategies, which improve performance while maintaining cost-effectiveness. Additionally, advancements in wide-bandgap semiconductors, such as silicon carbide (Si C) and gallium nitride (Ga N) devices, have further improved MLI efficiency, switching speed, and thermal performance. As MLIs continue to evolve, their role in next-generation power

electronics is expected to expand, particularly in electric vehicle (EV) drivetrains, grid-tied renewable energy systems, high-voltage direct current (HVDC) transmission, and industrial motor drives. The ongoing efforts to enhance MLI topologies and control techniques will contribute to more efficient, compact, and reliable power conversion solutions in the future.

## II. EXISTING SOLUTION

Multilevel inverters (MLIs) have revolutionized the field of electrical engineering, offering unparalleled benefits in terms of flexibility, scalability, and efficiency. However, existing MLI designs are not without their limitations. Researchers have been working tirelessly to address these challenges and develop more efficient, compact, and reliable MLIs. One of the earliest attempts to improve MLI design was the introduction of a capacitor-based three-level unit. This design boasted a reduced switch count and medium voltage stress across semiconductor components. However, it required four power diodes and two capacitors per unit, increasing size, cost, and maintenance concerns. To address these issues, researchers proposed a capacitor-free circuit that integrated a conventional half-bridge with a new two-level structure. This design offered a reduced component count and modularity, making it an attractive option for high-voltage applications. However, it required multiple DC sources and high switch counts, leading to increased losses and costs. Hybrid MLIs have also been explored, aiming to balance the benefits of different topologies. For instance, a three-phase hybrid MLI configuration was proposed, featuring a two-level three-phase VSI, three single-phase three-level FHB, and three two-level HB. This design offered modularity and scalability, making it suitable for high-voltage high-power applications. However, it required many isolated DC sources and high switch counts, increasing complexity and costs. To overcome these challenges, researchers have proposed modified circuits that reduce component counts, increase efficiency, and improve reliability. For example, a diode-free T-type MLI was proposed, using only active switches to reduce conduction losses. Another approach involved the use of a hybrid active neutral point (HANPC) topology, generating three voltage levels with a reduced switch count. Despite these advancements, existing MLI designs still have limitations. They are often bulky, restricted to specific voltage levels, and require complex control strategies. To address these challenges, researchers have proposed novel MLI designs, such as the dual-buck MLI (DB-MLI) family. These designs aim to reduce component counts, increase efficiency, and improve reliability.

## III. PROPOSED SOLUTION

The transformer less MLI in Fig. 1's low-voltage configuration is a transformer less topology that operates without the need for a coupled inductor (CI) or flying capacitor (FC), enabling a compact and highly efficient design. In order to create a three-level unit, each phase is made up of just three switches that are uniquely connected. Additionally, the three-phase legs use the same DC-link in order to minimize the number of DC sources. Two symmetrical DC sources of  $E$  are connected in series to create the DC-link. Nevertheless, batteries or AC voltage sources followed by rectifiers can be used in place of these DC sources. To establish distinct routes from the two DC sources to the load, nine power switches,  $S_1$  through  $S_9$ , are utilized. As a result, the DC sources can be set up in various ways to produce the line voltage at the following five levels:  $2E$ ,  $E$ ,  $0$ ,  $-E$ , and  $-2E$ . For instance, the line voltages  $V_{AB}$ ,  $V_{BC}$ , and  $V_{CA}$  are equal to  $2E$ ,  $-2E$ , and  $0$  when  $S_1$ ,  $S_6$ ,  $S_8$ , and  $S_9$  are in the ON state and the other switches are in the OFF state. Figure 2 displays the conduction paths for the forward and reverse currents in the red and blue lines, respectively, as well as the switching modes for the suggested circuit when generating five voltage levels in the line voltage  $V_{AB}$ . These modes of switching have been chosen to avoid the appearance of a positive voltage across the switches' built-in diodes. Consequently, short-circuit faults are prevented from affecting the DC sources. Additionally, some specific switching states are eliminated from the inverter's control algorithms for the same reason. In phase A, for instance,  $(S_1-S_3)$ ,  $(S_1, S_2, S_4)$ , and  $(S_3, S_4)$  cannot all be in the ON-state simultaneously. A new three-phase module is used as a repeated stage in addition to the low-voltage configuration of the suggested inverter, which uses a three-level configuration as a fixed stage. Three basic cells or one cell for each phase are present in each module. Two DC sources and eight switches are needed for each basic cell.

For symmetrical and asymmetrical DC sources, it can generate five and seven voltage levels, respectively. The DC link and either leg A + leg B, leg B + leg C, or leg C + leg A are used to form the basic cell, which is the two-phase version of the fixed stage. The basic cell is designed to be used in the two suggested configurations, which saves time, money, and effort in manufacturing, maintenance, and voltage upgrading. Because of the modularity feature, the voltage levels in the hybrid configuration of the suggested topology can be increased to  $N$  levels without raising the voltage stress across the switches. In terms of voltage levels  $N$ , the numbers of the three-phase modules  $M$ , switches

NSW, and DC sources NDC are shown in (1) through (3). According to the calculation in (1), only one module is required to produce seven levels in the pole voltage. As a result, 36 switches and 8 symmetrical DC sources are needed.

$$M=0.25N-0.75 \quad (1)$$

$$NDC=1.5N-2.5 \quad (2)$$

It is worth mentioning that the switch count for each module can be reduced to eighteen instead of twenty-four switches. This can be obtained by merging the three switches SM5A, SM6A, and SM7A in each basic cell to be one switch and changing the switching algorithm a little bit. For example, in the first module (i.e.  $M = 1$ ), S15A, S16A, and S17A can be merged to be one switching device with a higher blocking voltage ( $2E$  instead of  $E$ ). Accordingly, the total number of required switches could be reduced, as calculated in (4) for symmetrical operation.  $NSW = 4.5N - 1.5$  (4)

**A. Modulation Strategies** Only twelve of the 64 switching states in the low-voltage configuration—which are compiled in Table I—are needed for the switching algorithms of the two modulation techniques. In order to prevent any switching paths from forming a closed loop for the DC sources, these nine switching states were chosen. Additionally, when choosing these switching states, the number of ON-switches in the conducting path for each level was decreased in order to lower the conduction losses. According to Table I, S3 and S4's switching states are designated with the letter "X" in order to produce  $2E$  in pole A. The letter "X" indicates that these switches can be in either the ON or OFF state, but the switching loss is minimized by minimizing the number of switching cycles.

Because of this, the switching algorithms were created to maintain the same prior states of S3 and S4 as their new switching states; that is, if the prior state was ON, the X-state will be ON, and vice versa. For instance, in S4, the new state is chosen to be OFF since the previous switching state was OFF. The three-pole voltage waveforms VA0, VB0, and VC0 are highlighted in Fig. 4, which also displays the LFM's switching patterns. Three rectified sinusoidal waveforms with amplitudes of one are used by the LFM. To create L1-L6, these waveforms are compared to two signals: "Zero-reference" and a suggested modulator signal (referred to as H). The modulator signal H's value can be changed from 0 to 1 to produce a range of voltage.

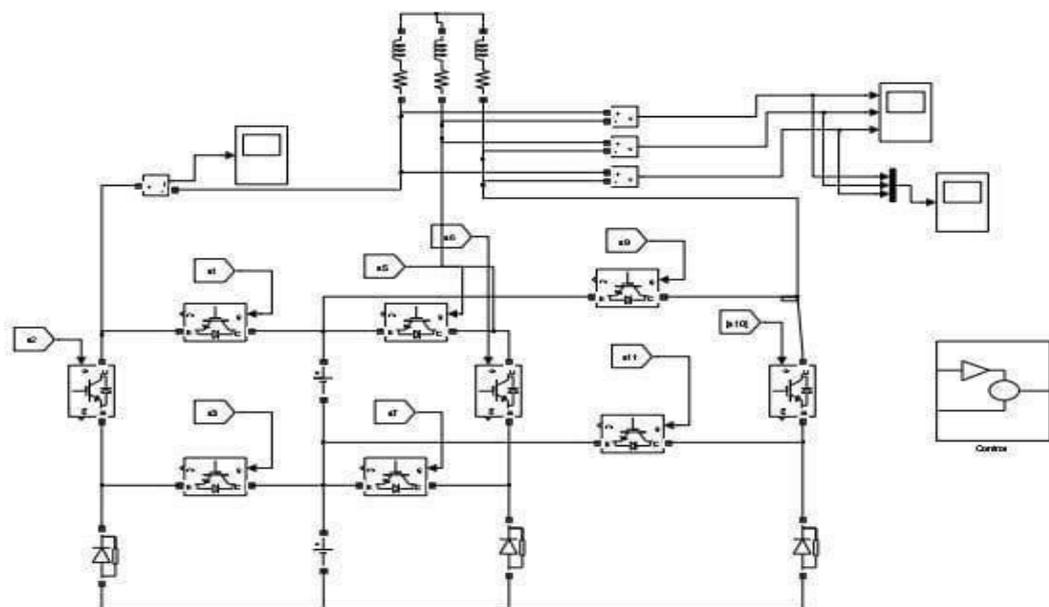


Fig. 1. N-level high-voltage configuration of the proposed topology.

$$NSW = 6N - 6$$

TABLE I

SWITCHING STATES AND THE CORRESPONDING POLE VOLTAGE OF  
PHASE A (X: ON OR OFF)

V <sub>A</sub>	Pole A			
	S <sub>1</sub>	S <sub>2</sub>	S <sub>3</sub>	S <sub>4</sub>
E	OFF	ON	ON	OFF
2E	ON	OFF	X	X
2E	ON	OFF	X	X
2E	ON	OFF	X	X
2E	ON	OFF	X	X
2E	ON	OFF	X	X
E	OFF	ON	ON	OFF
0	OFF	ON	OFF	ON
0	OFF	ON	OFF	ON
0	OFF	ON	OFF	ON
0	OFF	ON	OFF	ON
0	OFF	ON	OFF	ON

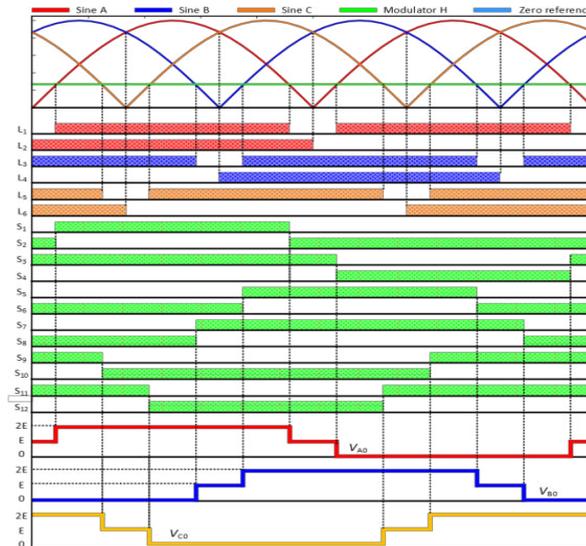


Fig 2: switching scheme of proposed inverter

$$S S L L 3, 4= 1 \times (6)$$

Table II, which lists the complete switching states for generating seven voltage levels, can be used to generate switching signals for the high-voltage configuration. It displays twenty-seven states, including seven primary states (shown in blue) and twenty redundant states. This gives switching algorithms some flexibility, balances switch power losses, and boosts reliability. The seven primary states were chosen in order to minimize the number of ON-switches in conduction paths and lower conduction losses. For instance, a 2E level can be produced using six different switching states; however, the second state, which has three ON-switches, is chosen and designated as the primary state, lowering the conduction losses by at least 40% when producing 2E because the other five states use either five or six ON

switches.

The LS-PWM scheme was used in addition to LFM. The necessary switching pulses for the switches in the low-voltage configuration are produced using three sinusoidal waveforms (SM1, SM2, and SM3) and two carrier signals (CR1 and CR2). With a phase shift of 120°, the signals from SM1 through SM3 are identical in size and shape. The process by which the four switches in phase A generate switching pulses. By comparing the SM1 with the two carrier signals, the Y and Z signals are produced. The correct switching signals are then extracted from Y and Z using various Boolean operators. Similar to this, switching pulses for the high-voltage configuration can be produced, but there are now six carrier signals rather than just two. Consequently the sinusoidal modulation signals are compared with six carrier signals to generate six controlling signals, denoted by X1 through X6 from top to bottom. By applying the Boolean operations to the six controlling signals as summarized, the switching pulses of phase A are produced..

TABLE II  
SWITCHING STATES AND THE CORRESPONDING POLE VOLTAGE FOR SEVEN-LEVEL CONFIGURATION OF THE PROPOSED TOPOLOGY

$V_{A0}$	$S_{A1}$	$S_{A2}$	$S_{A3}$	$S_{A4}$	$S_{11A}$	$S_{12A}$	$S_{13A}$	$S_{14A}$	$S_{15A}$	$S_{16A}$	$S_{17A}$	$S_{18A}$
Phase A, fixed stage				Phase A in the first module								
4E	ON	OFF	OFF	OFF	ON	ON	OFF	ON	OFF	OFF	OFF	OFF
3E	OFF	ON	ON	OFF	ON	ON	OFF	ON	OFF	OFF	OFF	OFF
	ON	OFF	OFF	OFF	ON	ON	OFF	OFF	ON	OFF	ON	OFF
2E	ON	OFF	OFF	ON	OFF	ON	OFF	ON	OFF	OFF	OFF	OFF
	ON	OFF	OFF	OFF	OFF	OFF	ON	ON	OFF	OFF	OFF	OFF
	ON	OFF	OFF	OFF	ON	ON	OFF	OFF	ON	ON	OFF	OFF
	ON	OFF	OFF	OFF	OFF	ON	OFF	OFF	ON	OFF	ON	ON
	OFF	ON	ON	OFF	ON	ON	OFF	OFF	ON	OFF	ON	OFF
E	OFF	ON	ON	OFF	OFF	ON	OFF	ON	OFF	OFF	OFF	ON
	ON	OFF	OFF	OFF	OFF	OFF	ON	OFF	ON	OFF	ON	OFF
	OFF	ON	OFF	ON	OFF	ON	OFF	OFF	ON	OFF	ON	OFF
	OFF	ON	ON	OFF	ON	ON	OFF	OFF	ON	ON	OFF	OFF
	OFF	ON	ON	OFF	OFF	OFF	ON	ON	OFF	OFF	OFF	OFF
0	ON	OFF	OFF	OFF	OFF	OFF	ON	OFF	ON	ON	OFF	OFF
	OFF	ON	ON	OFF	OFF	ON	OFF	OFF	ON	ON	OFF	ON
	OFF	ON	ON	OFF	ON	ON	OFF	OFF	ON	ON	OFF	OFF
	OFF	ON	OFF	ON	OFF	ON	OFF	OFF	ON	OFF	ON	ON
	OFF	ON	OFF	ON	OFF	OFF	ON	ON	OFF	OFF	OFF	OFF
E	OFF	ON	OFF	ON	OFF	ON	OFF	OFF	ON	ON	OFF	ON
	OFF	ON	OFF	ON	OFF	OFF	ON	OFF	ON	OFF	ON	OFF
-2E	OFF	ON	OFF	ON	OFF	OFF	ON	OFF	ON	ON	OFF	OFF

$$SS_{A1}, A2 = X_3 \quad (7)$$

$$S_{A4} = X_4 \quad (8)$$

$$S_{A4} = X_4 \quad (9)$$

$$S_{A4} = X_4 \quad (10)$$

$$S_{12A}, S_{13A} = X_2 \quad (11)$$

$$S_{14A}, S_{15A} = X_5 \quad (12)$$

$$S_{16A} = X_6 \quad (13)$$

$$S_{17A} = X_6 \times 6 \quad (14)$$

$$S_{18A} = X_6 \times 2 \quad (15)$$

TABLE III  
SYSTEM SPECIFICATIONS AND USED COMPONENTS

Description	Value/ Part number	Unit
DC voltage source ( $E$ )	70	V
Load $R, X_L$	30, 31.41	$\Omega$
Carrier frequency ( $F_s$ )	1000	Hz
Modulation signal frequency ( $F$ )	50	Hz
Modulation index ( $M_1$ ), LS-PWM	0.9	-
Modulator signal ( $H$ ), LFM	0.27	-
Sampling time ( $T_s$ )	15	$\mu s$
Switching device	SKM300GA12E4	-
Gate-driver board	SKHI 10/12 R	-
DC voltage source	62024P-100-50	-

### V. SIMULATION AND EXPERIMENTAL RESULTS

The operational principles of the proposed circuit are verified by simulating both switching schemes in Mat lab/Simulink and testing them on a laboratory model. In constructing the low-voltage prototype, two DC voltage sources are added to twelve insulated gate bipolar transistors (IGBT) modules with integrated freewheeling diodes. An complete in-house setup is captured and showed in Fig 6. The switching algorithms for both LFM and LS-PWM are implemented with a digital controller – d SPACE Micro Lab Box. Two primary DC sources are used to energize the three- phase load through 12 IGBT modules SKM300GA12E4. Each IGBT is driven by SKHI 10/12 R gate driver board that is mounted on a heatsink to cool down the IGBT's internal junction temperature. The test setup further includes secondary devices like low-power DC source for driver boards, oscilloscope, voltage- and current-probe. The specifications of the used cases in simulations and experimental tests are presented in Table III.

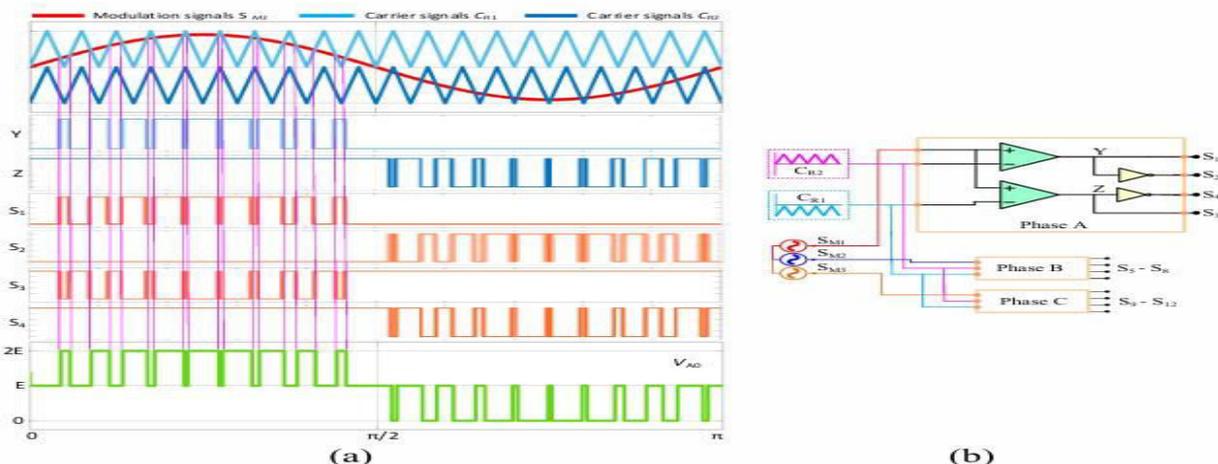


Fig. 5. LS-PWM switching scheme for the low-voltage configuration.

The simulation results for the pole voltages, and under both LFM and LS-PWM control methods are illustrated in Figures 6 and 7. Each waveform exhibits three distinct voltage levels: 0,  $V_{dc}/3$ , and  $2V_{dc}/3$ , with a consistent phase shift of  $120^\circ$  among the three-phase voltages. Experimental verification revealed a strong correlation between the measured waveforms and the simulated results. During the experimental tests, the 'voltage-per-division' setting on the oscilloscope was adjusted dynamically instead of being fixed, allowing the waveforms to be properly displayed on the screen.

The balanced three-phase line voltages, and were measured, showing five distinct voltage levels:  $0$ ,  $V_{dc}/3$ ,  $2V_{dc}/3$ ,  $V_{dc}$ , and  $4V_{dc}/3$ . These levels were derived from the pole voltage waveforms, which maintained three-level behavior with a  $120^\circ$  phase shift. To evaluate the inverter's performance under load conditions, a resistive-inductive (R-L) load was utilized. The test results were obtained for a load with a power factor of 0.7. For the phase-load voltage, the LFM method produced seven voltage levels:  $0$ ,  $V_{dc}/3$ ,  $2V_{dc}/3$ ,  $V_{dc}$ ,  $4V_{dc}/3$ ,  $5V_{dc}/3$ , and  $2V_{dc}$ . In contrast, the LS-PWM method yielded nine distinct voltage levels:  $0$ ,  $V_{dc}/3$ ,  $2V_{dc}/3$ ,  $V_{dc}$ ,  $4V_{dc}/3$ ,  $5V_{dc}/3$ ,  $2V_{dc}$ ,  $7V_{dc}/3$ , and  $3V_{dc}$ . The additional two voltage levels in the LS-PWM scheme result from its unique pole voltage combinations.

Table IV provides a comprehensive list of the different pole voltage combinations utilized in the proposed topology. In the case of the LFM scheme, only seven voltage combinations (A1-A3, A5, and A7-A9) are achievable, whereas the LS-PWM scheme allows for nine combinations (A1-A9). Although the LFM approach employs lower switching frequencies, the LS-PWM method provides greater flexibility. The LS-PWM scheme enables real-time adjustments of output voltage frequency, RMS value, and voltage level count by modifying the frequency and amplitude of the modulation signal. Conversely, in the LFM method, the integrated modulator introduces an additional degree of freedom, allowing variation in output voltage levels and RMS value while maintaining conventional sinusoidal modulation-based frequency control. The simulation and experimental results confirm that modifying  $m$  from 1 to 0 alters the RMS value of the line voltage, reducing it from 100% to 81.6% of the DC-link voltage. Furthermore, the number of line voltage levels changes depending on  $m$ : three levels when  $m=1$ , five levels when  $m=0.5$ , and zero when  $m=0$ . This demonstrates that the proposed inverter topology effectively provides variable magnitude, frequency, and level control for both LS-PWM and LFM modulation techniques.

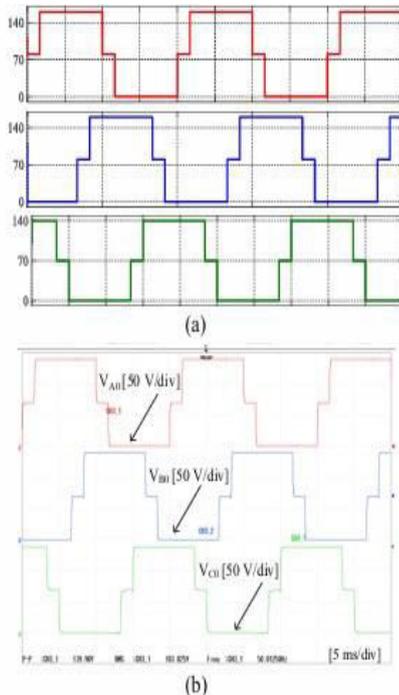


Fig. 7. Pole voltages  $V_{A0}$ ,  $V_{B0}$ , and  $V_{C0}$  for LFM. (a) Simulation. (b) Experimental.

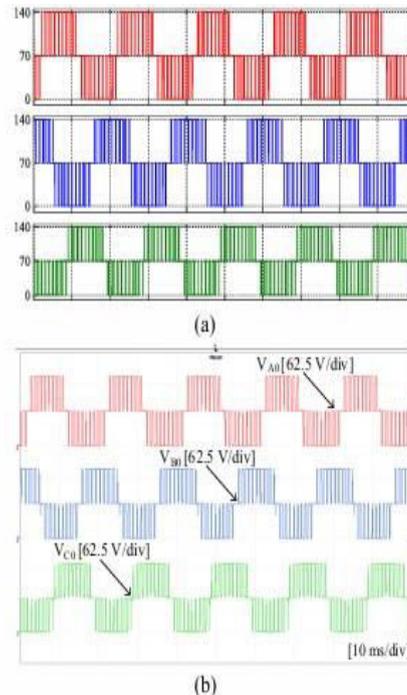


Fig. 8. Pole voltages  $V_{A0}$ ,  $V_{B0}$ , and  $V_{C0}$  for LS-PWM. (a) Simulation. (b) Experimental.

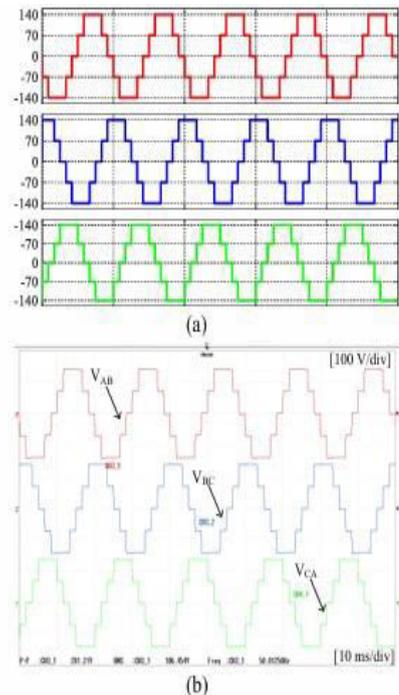


Fig. 9. Line voltages  $V_{AB}$ ,  $V_{BC}$ , and  $V_{CA}$  for LFM. (a) Simulation. (b) Experimental.

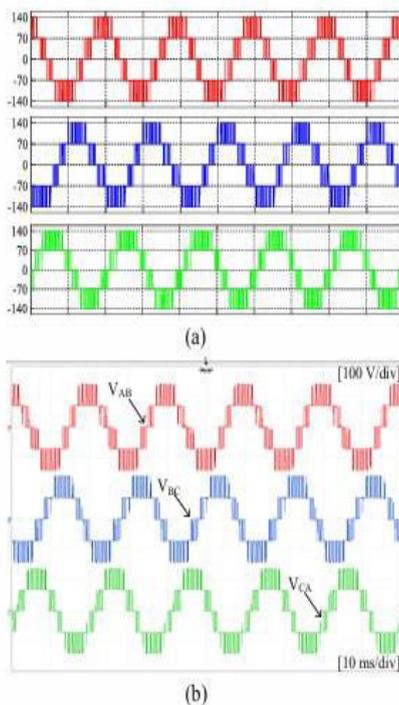


Fig. 10. Line voltages  $V_{AB}$ ,  $V_{BC}$ , and  $V_{CA}$  for LS-PWM. (a) Simulation. (b) Experimental.

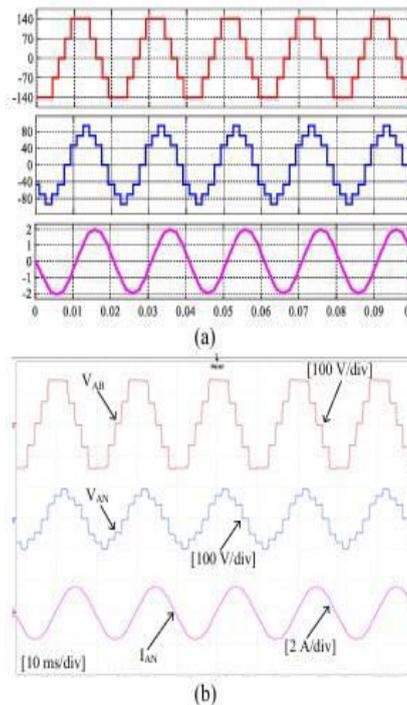


Fig. 11. Obtained  $V_{AB}$ ,  $V_{AN}$ , and  $I_{AN}$  for LFM. (a) Simulation. (b) Experimental.

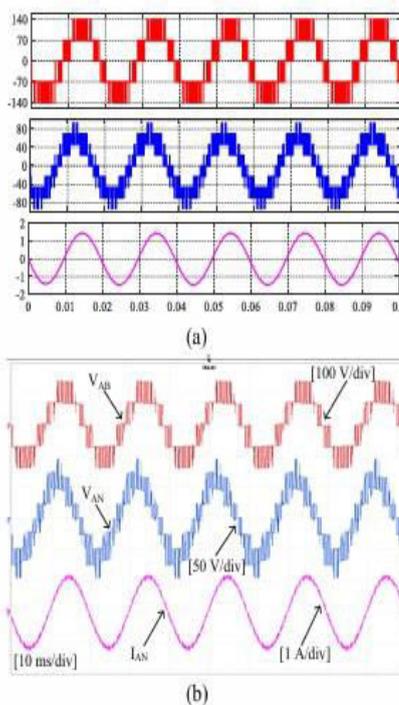
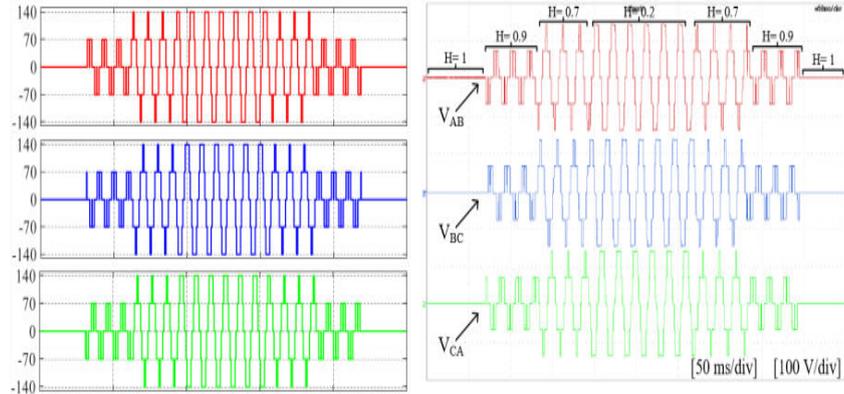


Fig. 12. Obtained  $V_{AB}$ ,  $V_{AN}$ , and  $I_{AN}$  for LS-PWM. (a) Simulation. (b) Experimental.

TABLE IV  
POLE VOLTAGE COMBINATIONS FOR THE USED  
SWITCHING SCHEMES

	LFM			LS-PWM			Phase voltage	
	$V_{A0}$	$V_{B0}$	$V_{C0}$	$V_{A0}$	$V_{B0}$	$V_{C0}$	LFM	LS-PWM
A1	2E	0	0	2E	0	0	4/3E	4/3E
A2	2E	E	0	2E	E	0	E	E
A3	2E	2E	0	2E	2E	0	2/3E	2/3E
A4	-	-	-	E	E	0	-	1/3E
A5	E	2E	0	E	2E	0	0	0
A6	-	-	-	E	2E	E	-	-1/3E
A7	0	2E	0	0	2E	0	-2/3E	-2/3E
A8	0	2E	E	0	2E	E	-E	-E
A9	0	2E	2E	0	2E	2E	-4/3E	-4/3E



Some selected results for the hybrid configuration of the proposed topology and when the fixed stage and one repeated module are used for feeding power to an R-L load ( $R=50 \Omega$ ,  $L=100 \text{ mH}$ ) under LFM and LS-PWM, respectively. By using one module cascaded with the fixed stage, seven levels of  $-2E$ ,  $-E$ ,  $0$ ,  $E$ ,  $2E$ ,  $3E$ , and  $4E$  can be produced in the pole voltage  $V_{A0}$  while thirteen levels of  $-6E$ ,  $-5E$ ,  $-4E$ ,  $-3E$ ,  $-2E$ ,  $-E$ ,  $0$ ,  $E$ ,  $2E$ ,  $3E$ ,  $4E$ ,  $5E$ , and  $6E$  are generated in the line voltage  $V_{AB}$ .

## VI. POWER LOSSES AND EFFICIENCY ANALYSIS

The power losses in semiconductor devices are classified into three categories according to the operating state of the device:

A) OFF-state losses, B) ON-state or conduction losses, and C) changing-state or switching losses [31- 33]. Due to the nonideality characteristics of switches, a leakage current is following through switches during OFF-state, causing OFF-state power losses. The OFF-state losses can be neglected in most cases since leakage currents are insignificant during OFF- state [31]. During the ON-state, the switches have non-zero ON-state voltage ( $V_{on}$ ) and ON-state resistance ( $R_{on}$ ), causing power losses. The ON- state losses depend on  $V_{on}$ ,  $R_{on}$ , load current and the switch duty cycle [33]. The transitions, from OFF- to ON states and vice versa, cannot occur instantaneously. In those transition periods, the flowing current and voltage across the device result in a large instantaneous loss or dissipated energies, which are termed as turn-on energy ( $E_{on}$ ) and turn-off energy ( $E_{off}$ ) for IGBTs, and reverse recovery energy ( $E_{rec}$ ) for diodes. The switching losses are directly proportional to the switching frequency and blocking voltage of the devices [31, 32, 34]. More details on calculating the switching and conduction losses can be found in [31-34].

The efficiency of the proposed topology and the losses distribution in the switches are analysed based on a PSIM software model, considering the actual working condition of the IGBT modules. The required parameters of IGBTs are obtained from data sheets provided by component manufacturers. The IGBT modules are assumed to be working at a junction temperature of  $150^\circ \text{C}$ . Table V shows the system specifications and the parameters of used IGBT modules. The IGBT module has a part number of SKM300GA12E4, which is medium-fast trench.

The loss distribution of different switches, where the losses are divided into conduction losses ( $P_{con}$ ) and switching losses ( $P_{sw}$ ). The conduction period and blocking voltage of the switch have the main effects on the conduction losses and switching losses when the switching frequency and load are kept constant ( $F_s = 5 \text{ kHz}$  and  $P_{out} = 4 \text{ kW}$ ). For example, S1, S5, and S9 have voltage stresses of  $2E$ , so their switching losses are higher than the other switches. On the other hand, S2, S6, and S10 have the highest conduction losses because their conduction durations are the longest among switches. the switching frequency significantly affects switching losses, but it has a small impact on the conduction losses.

**VII. CONCLUSION**

This paper presents and analyses a new three-phase multilevel topology, being applicable for both low-voltage and high-voltage applications. The key features of the proposed topology are numerically verified by simulation results and experimentally validated through an in-house laboratory prototype. The proposed topology is tested using a resistive-inductive load under low- frequency modulation and level- shifted pulse width modulation techniques. Further, the LFM is modified by integrating the proposed modulator H, enabling online control of the output voltage in terms of RMS value, frequency, and level count. Using similar building blocks in both configurations allows for reducing the time and cost of manufacturing, troubleshooting, voltage- level upgrading. A detailed comparison between the proposed topology and other recently developed MLIs in terms of component count and voltage ratings proves that the proposed topology avoids using of inductors, and capacitors, resulting in a more compact design with a higher life-time, efficiency and simpler control algorithms.

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4. Ganesan, Bhaskar, and Narayanan introduced an 11-level multilevel inverter, presented at the IEEE Innovative Smart Grid Technologies Conference in 2018, appearing on pages 1050-1055.
5. Saeidabadi et al. proposed an improved three-phase hybrid multilevel inverter that requires fewer components. This study appeared in IET Power Electronics, Vol. 10, No. 12, pp. 1403-1412, in 2017.
6. Solanki, Ayalani, and Gohil investigated the efficiency of a three-phase T-type multilevel inverter with fewer switches. Their findings were presented at the International Conference on Current Trends in Converging Technologies, 2018, pp. 1-5.
7. Wang and his team designed a diode-free, three-level T-type neutral-point-clamped inverter for renewable energy systems. Their work was published in IEEE Transactions on Industrial Electronics, Vol. 61, No. 11, pp. 6168-6174, in 2014.
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11. pp. 2081-2091, in 2017.



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