



# International Journal of Innovative Research in Science Engineering and Technology (IJIRSET)

*(A Monthly, Peer Reviewed, Refereed, Scholarly Indexed, Open Access Journal)*



**Impact Factor: 8.699**

**Volume 14, Issue 5, May 2025**

# VLSI Design and Analysis of BioInspired Spiking Neural Network using Network-On-Chip Architectures

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**ABSTRACT:** Spiking neural networks (SNNs), with their rich spatially-temporal dynamics, versatile encoding techniques, and event-driven properties that easily align with neuromorphic hardware, have drawn a great deal of attention in the field of brain-inspired intelligence in recent years. With the advent of SNNs, brain-inspired intelligence—an emerging field of study motivated by advances in brain science and geared toward the creation of artificial general intelligence—is gaining popularity. The brain's connectivity is sparse globally and dense locally, generating a small world graph. This pattern of connectivity has been present throughout species evolutionary histories and suggests a common method for effectively routing information. Nevertheless, small-world neural network models are not fully embraced by artificial neural network circuit architectures as they exist today. A ground-breaking method for offering a scalable and high-performance infrastructure for on-chip communication is the 3D Network-on-Chip concept. In the discipline of Neuro Engineering, the most important prerequisite is the construction and optimization of large scale neural systems on reconfigurable hardware that mimic human sensory capabilities. Providing highly dynamic and adjustable neural connectivity is the primary architecture-related difficulty for these reconfigurable Neural Nets (NNs) and their hardware implementation. In order to simulate a third generation (3G) neural network model called the Spiking Neural Network (SNN), this study provides an on-chip connection design and 3D Modular Clustered Neural Tile (3D MCNT) architecture. In comparison to previously published designs for the effective simulation of bio-inspired computer paradigms, a hybrid Network-on-Chip router—a blend of wired and wireless NoC routing paradigms—is built and shown to be a more reliable platform with high speed and low area. This design supports real-time applications in robotics, healthcare, and neuromorphic computing, including prosthetic control and neurodegenerative disease detection. Key advancements include prosthetic arm control and neurodegenerative disease detection, positioning the architecture as a breakthrough in brain-inspired intelligence.

**KEYWORDS:** Silicon on Chip, Wired NoC, Wireless NoC, Router, MCNT, Bio Inspired Computing, Neuromorphic Hardware.

## I. INTRODUCTION

Numerous IP Blocks can now be integrated into a single chip according to Moore's law. Numerous IP cores, including memory blocks and DSP processors, are included into SoCs. These days, high-speed computing systems utilizing chip multiprocessor techniques are emerging, and increasing computation speed only requires a slight increase in power. Every IP block in a symmetric chip multiprocessor has the same characteristics and configuration. There is still a communication bottleneck between these blocks. Network-on-Chip (NoC) technology is capable of the fastest communication. To achieve high speed in NoC, packets are exchanged rather than signals being sent from one tile to the next. NoC facilitates the convergence of applications, but it also opens up completely new possibilities. For example, it is possible to handle several data streams—such as communication channels—in parallel on a chip by utilizing a large number of tiny processors, or SoCs [1-3]. Routers that transfer packets from one processing element (or tile) to another and vice versa are known as network interfaces (NIs), and processing elements, also known as IP cores or tiles, made up the NoC. Neuroscientists are very interested in the structure of connection between brain neurons because it may provide insight into how information is transmitted throughout the brain and processed to create higher order behaviors like pattern recognition [4-6].



With the continuous advancement of computing technologies, Spiking Neural Networks (SNNs) have gained significant attention for their ability to replicate the brain's sparse global and dense local connectivity, enabling energy-efficient and high-speed processing. However, conventional artificial neural network (ANN) architectures struggle with scalability and real-time implementation due to high inter-neuron communication demands. To address these challenges, this project proposes a 3D Network-on-Chip (NoC) architecture incorporating a 3D Modular Clustered Neural Tile (3D MCNT) framework. This design optimizes on-chip communication, reduces router count, and enhances spike packet routing through a hybrid NoC system integrating wired and wireless links. By leveraging NoC technology, the system ensures high-performance, scalable, and reliable processing, making it suitable for applications in robotics, healthcare, and neuromorphic computing. This research aims to bridge the gap between biological neural models and commercial computing architectures, paving the way for innovations such as prosthetic arm control systems and neurodegenerative disease detection while contributing to the future of brain-inspired intelligence. Unlike conventional ANNs, SNNs communicate through discrete spikes, reducing power consumption and computational complexity.

On the other hand, the interconnect is required for the spike transfer between neurons that are assigned to separate processors. Software simulations of conventional SNN network topologies and connection strategies encounter the problem of scalability in biological computing systems, whereas commercial Personal Computers (PC) are built on sequential processing architectures [7, 8]. This makes it challenging to evaluate how well these models perform in solving composite problems. Though there are non-trivial solutions, these constraints can be overcome. Spiking Neural Networks may fully utilize their inherent parallelism and have a computational speed advantage over software simulations when implemented on hardware, making them suitable for real-time applications. Creating effective hardware implementation architectures that can handle large-scale realizations is a major challenge [5]. The exploration of SNN mapping to FPGAs has drawn attention from academics due to its capacity to change logic blocks and interconnect. Generally speaking, the goal of utilizing an FPGA is to improve performance through reconfigurable and dedicated hardware parallelism. On the other hand, the number of logic units on an FPGA chip does not directly correspond to an increase in switching requirements [9-12]. This FPGA interface issue severely restricts the utility of FPGAs for SNN implementation since they are unable to handle the high volumes of inter-neuron communication. Effective, low-area/low-power implementations of synaptic junctions and neuron connections are essential for scalable hardware implementations of SNNs. Scalable connectivity is the primary benefit of NoC. Higher levels of connectivity can be achieved without a significant increase in the interconnect-to-device area ratio.

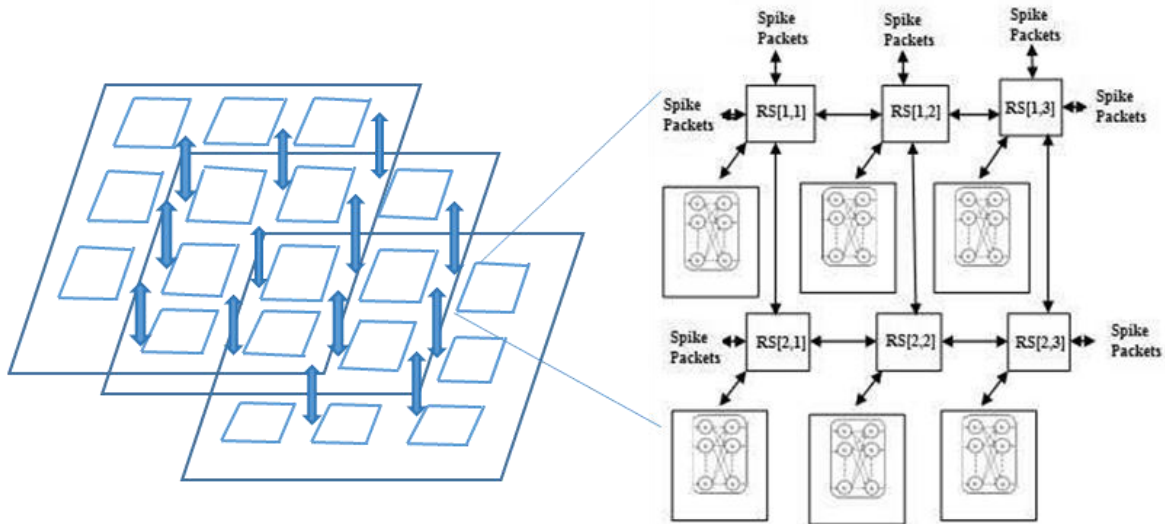
## **II. RELATED WORK**

Several studies have explored the hardware implementation of Spiking Neural Networks (SNNs) to enhance efficiency and scalability. One such approach involves FPGA-based SNNs, which mimic biological neurons using discrete spike-based communication. These implementations significantly reduce computational load and power consumption while enabling parallel processing for faster execution. Another study focused on low-power SoC design for SNNs, utilizing a Current Multiplier Charge Injector (CMCI) synapse to minimize power consumption and chip area usage, making it an energy-efficient alternative for neuromorphic computing. Additionally, research on neuromorphic computing for SNNs has explored Spike-Timing-Dependent Plasticity (STDP) algorithms, which enable adaptive learning and efficient spike-based information processing, further demonstrating the advantages of biological neural emulation in real-world applications. Despite these advancements, existing solutions face scalability issues, particularly in FPGA-based designs that struggle with large-scale inter-neuron communication. Additionally, high power consumption remains a challenge due to the lack of an optimized communication framework for real-time applications. Furthermore, prior studies have not fully utilized 3D Network-on-Chip (NoC) architectures, which could significantly improve on-chip data transfer and routing efficiency. To address these limitations, this project introduces a 3D Modular Clustered Neural Tile (3D MCNT) architecture with a hybrid NoC system that integrates wired and wireless communication links. This novel approach enhances scalability, reduces power consumption, and improves spike packet routing efficiency, making it a highly suitable solution for real-time applications such as prosthetic arm control and neurodegenerative disease detection.

## **III. METHODOLOGY**

The proposed methodology focuses on developing a 3D network-on-chip (NoC) architecture for spiking neural networks (SNNs) using Xilinx Verilog-based simulation rather than physical hardware implementation. The process

begins with a comprehensive literature review to analyze existing SNN architectures, identifying challenges such as scalability, communication bottlenecks, and power efficiency.



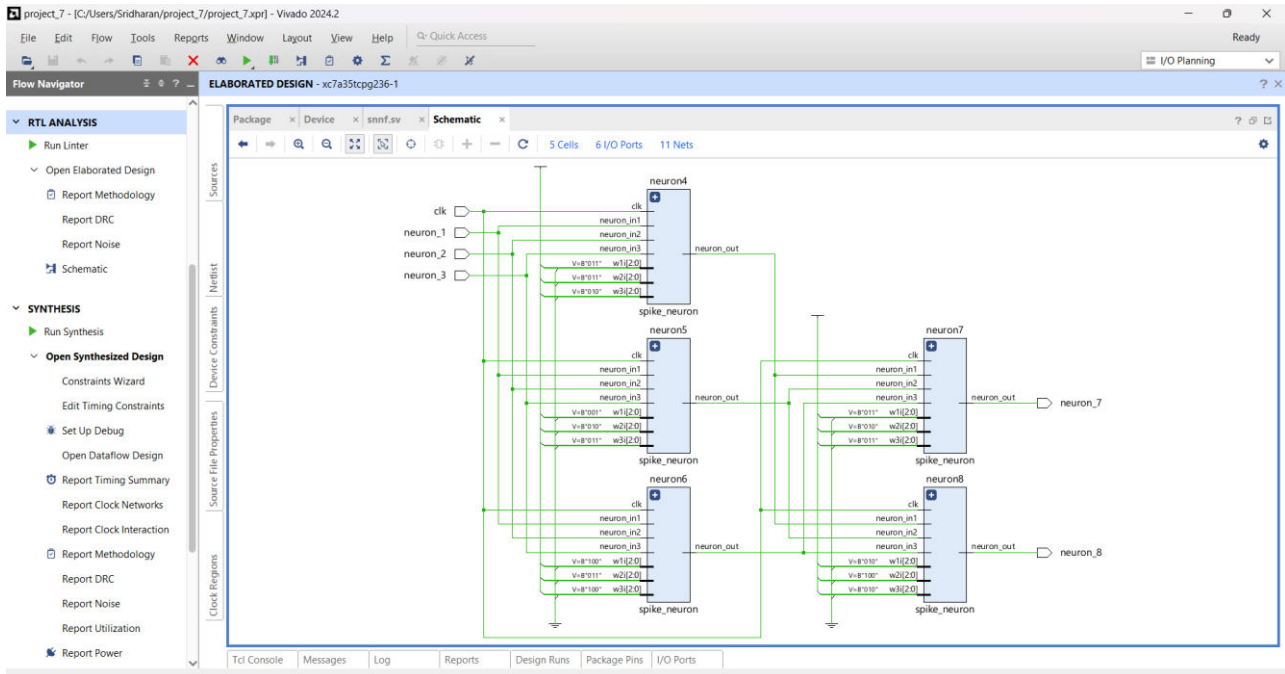
**Fig.1 Proposed 3d NoC Architecture**

Fig.1 depicts the suggested NoC architecture for 3D MCNT. It is composed of a number of Network-on-Chip (NoC) routers and Modular Clustered Neural Tile (MCNT) cores. The on-chip communication in this proposed architecture is based on a particular array of reconfigurable NoC routers. The NoC routers are connected in the North (N), East (E), South (S), and West (W) directions and are arranged in a 3-D Mesh topology array of neural tiles. Spike information contained in spike data packets is transported across the network of routers to allow spike communication between MCNT cores. For the effective emulation of bioinspired platforms, a hybrid NoC system—a combination of wired and wireless links—can offer a more reliable and high-performance platform. Because of this, the design that is being suggested here is hybrid and consists of both wired and wireless NoC routers. These routers are configured so that wired links are used when there is just one hop between MCNT tiles. The wired routers are used to route the spike packets. A wireless link is activated and packet routing via wireless routers takes place when there are more than two hops between MCNT tiles.

Based on these findings, a 3D modular clustered neural tile (3D MCNT) architecture is designed, incorporating a hybrid NoC system with both wired and wireless links to optimize spike packet routing and on-chip communication. The system is implemented and simulated using Verilog on Xilinx tools, focusing on developing an efficient router-based NoC infrastructure with a north-east-south-west (NESW) routing strategy to improve data transfer efficiency. Performance analysis is conducted by evaluating latency, reliability, and power consumption, comparing the results with existing SNN models to validate improvements. The application scope includes real-time neuromorphic computing, particularly in prosthetic arm control and neurodegenerative disease detection using recurrent spiking neural networks (RSNNs). Finally, future research aims to explore scalability in large-scale neural simulations, enhancing AI, robotics, and biomedical applications. This methodology ensures a high-performance, scalable, and energy-efficient NoC-based SNN architecture for real-time computational neuroscience applications.

#### IV. EXPERIMENTAL RESULTS

Figures show the results of Execution of spiking neural network in Xilinx vivado 2024.2 version. Figs. 1 (a) shows the RTL Design of spiking neural network. Fig.(b) is the simulation of spiking neuron. By giving inputs to ports we can detect the spike. Fig.(c) shows the power consumption of chip after it implemented as chip., Total on-chip power consumption is 0.075 Watts. and the junction temperature as 25° C.



Fig(a)

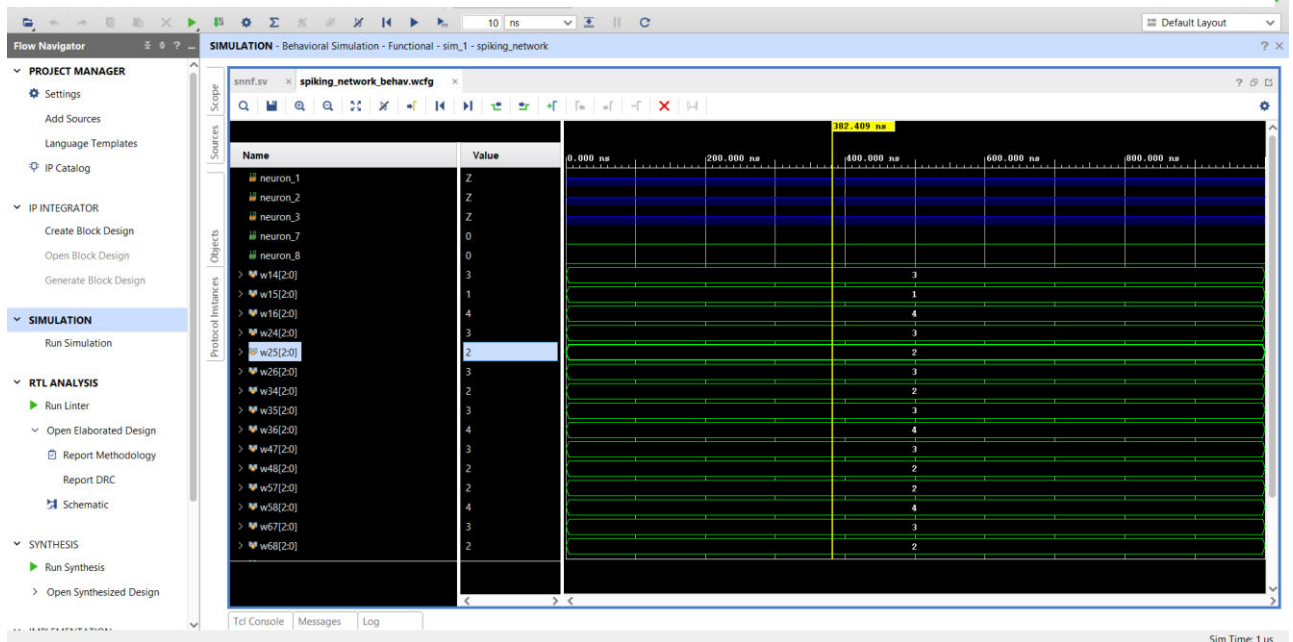


Fig.(b)

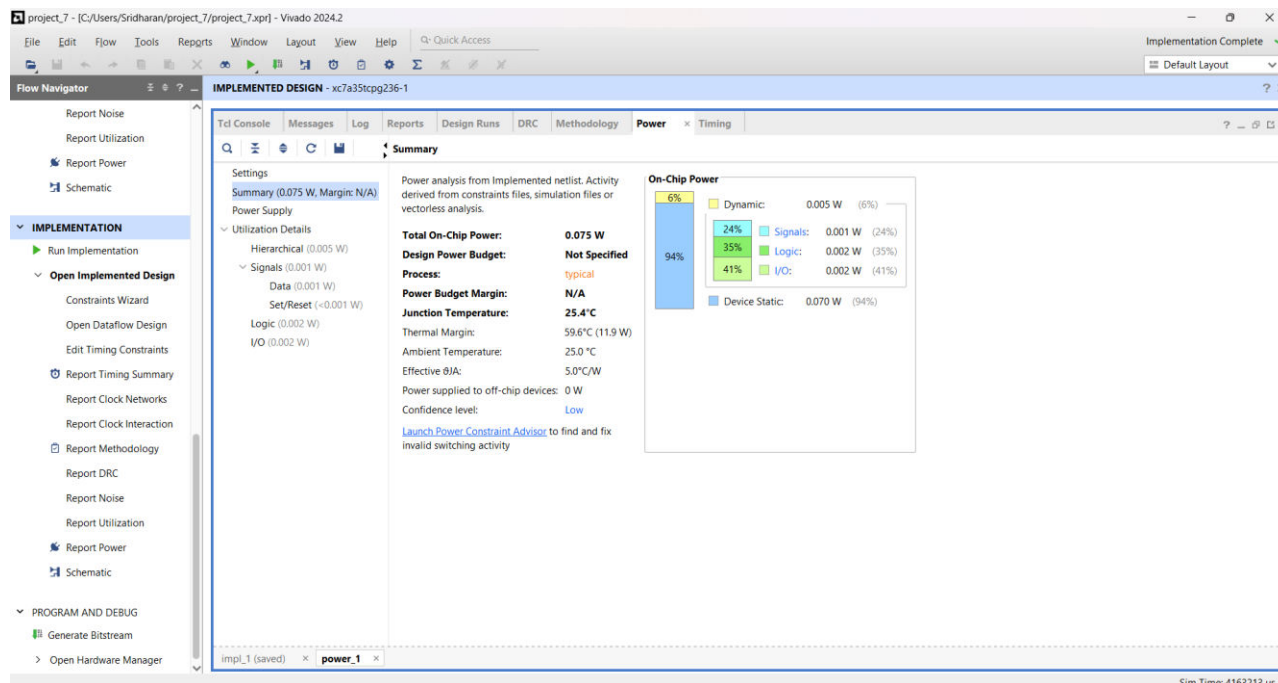


Fig.(c)

## V. CONCLUSION

This project presents a 3D Network-on-Chip (NoC) architecture for efficient Spiking Neural Network (SNN) emulation, focusing on scalability, optimized communication, and energy efficiency. The proposed 3D Modular Clustered Neural Tile (3D MCNT) design reduces router count, enhances spike packet routing, and integrates wired and wireless NoC links for improved data transfer reliability. Implemented and simulated using Xilinx Verilog, the architecture demonstrates low latency, high processing efficiency, and reduced resource utilization compared to existing models. The system's real-time applicability in prosthetic arm control and neurodegenerative disease detection highlights its potential in neuromorphic computing, robotics, and healthcare. Future work will explore silicon realization and large-scale neural simulations, paving the way for advancements in biological computing and artificial intelligence.

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